TCAD Analysis on the Geometry Effects in Three-Independent-Gates Reconfigurable FETs

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***Abstract*—The n-type and p-type operations of 22 nm Fully Depleted Silicon on Insulator (FDSOI) Three-Independent-Gates Reconfigurable Field Effect Transistors (TIG-RFETs) are simulated, incorporating Schottky contacts to the drift-diffusion model. Key-features are selected and adjusted to fit experimental results, like: Schottky barrier height (SBH), direct tunnelling and presence of traps. The inclusion and correct adjustment of these parameters reveals the importance of strong electrostatic control over the energetic barrier at the metal-semiconductor junctions. We extend this analysis with a study of the theoretical impact of the metal-semiconductor interface position under the source-drain gates coupled with the length of the ungated regions.**

***Index Terms*—RFET, TCAD, FDSOI, Schottky contact, DTCO.**

I. Introduction

Reconfigurable FETs are an interesting alternative to the classic CMOS technology that offer more flexibility at the circuit design level [1]–[3]. Keeping the channel intrinsic, and directly contacting it with the source and drain metals, a Schottky Barrier will form. A gate is placed on top of each contact, which is used to electrostatically control the screening length, allowing or blocking the flow of one type of carrier. In addition to this, a third gate can be placed in the middle of the channel to control its conductivity in a more classical way. This flexibility comes with a performance penalty inherent to any Schottky-based transistor [4], [5], and more complexity when designing new logic cells. However, it allows that the same circuit block has various and run-time configurable working modes. The amount of different operation modes [6]–[8], input variables and potential transistors and cells designs is almost unlimited [9], [10]. Here is where accurate TCAD and compact models can offer a great help to explore the working principles and main parameters of the complete family of such devices [11].

In this work, we calibrate a semi-classical TCAD model to fit the experimentally measured transfer characteristics of a TIG-RFET based on the devices described in [12]. The model is used to explore the impact in the performance due to modifications of the geometry. This impact is difficult and expensive to systematically investigate in hardware. Examples of such parameters are the position of the contacts under the source-drain gates and the length of the ungated regions.

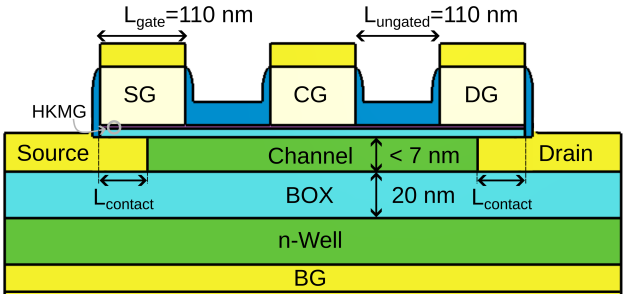

Fig. 1. Device schematic of a TIG-RFET. The key elements analysed in this study are: the ungated length ($L_{ungated}$) and the gate-contact overlap ($L_{contact}$)

II. Device Description and Working Principle

Fig. 1 shows the implemented geometry of the studied TIG-RFET taken from [12]. It is composed of a doping-free Silicon channel over an SiO_2 layer (BOX), a Back Gate (BG) below an n-type doped well, and three top gates, namely Source Gate (SG), Drain Gate (DG) and Central Gate (CG). These gates are subdivided into two groups: Programming Gates and Control Gates. Usually, the Programming Gate is the one used to select the kind of carrier that can flow in the device, whereas the Control Gate regulates the flow. Which one is the Control Gate depends on the operation mode and the number of gates in the RFET [13]. In a TIG-RFET, when the Control Gate is the central one and the Source Gate is biased together with the Drain Gate to program the transport mode, low threshold voltage (V_T) transfer curves are achieved. If, instead, the Source Gate is the one controlling the carrier flow, then a higher V_T is obtained. This is the high-V_T operation mode.

In this analysis, we will work on the numerical characterization of n-type and p-type branches, both under high-V_T and low-V_T operation modes. Optimizing the source/drain (S/D) contact is also crucial for enhancing the performance of these Schottky-barrier based devices. Therefore, the impact of geometry parameters, such as the gate-contact overlap length ($L_{contact}$) and the ungated length ($L_{ungated}$), is investigated.

III. TCAD Model

To account for the effects of quantum confinement, the density gradient model [14] is coupled in a Drift-Diffusion solver [15]. Thermionic emission (TE) at the contacts are evaluated, taking into account the SBH. The permeation model, as proposed by [16], is applied to account for direct tunnelling of both carriers through the SBH, depending on the operation mode. The transmission coefficient calculation is based on the Wentzel-Kramers-Brillouin (WKB) method for linear barriers. In an ideal case, these elements would be enough to describe the behaviour of these Schottky-barrier based devices. However, to better match experimental results, the presence of bulk traps in the channel, close to the contacts, also needs to be considered. The higher number of gates and operation modes compared to a classical MOSFET leads to a large design space. This can also complicate the fitting process to experimental data. Therefore, an optimization flow has been implemented to adjust the key selected parameters of the model, as demonstrated by [17].

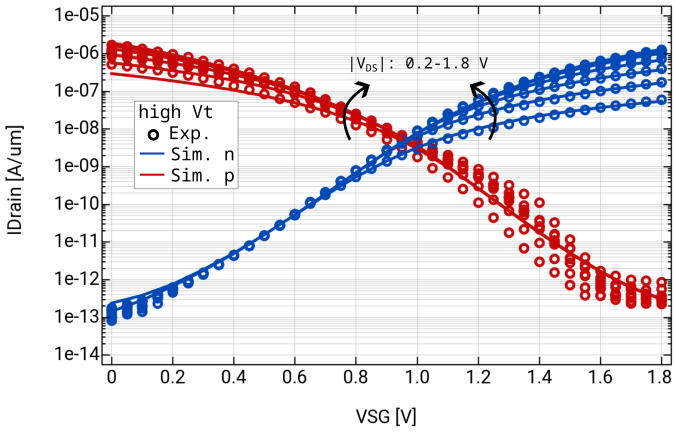

Fig. 2. TCAD simulation fitting to experimental transfer curves at different drain voltages in the high-V_T regime. In this case, the bias of CG and DG gates is fixed, whereas the SG is swept. The impact of the Schottky barrier, direct tunnelling and bulk traps is considered.

The fitted tranfer curves in comparison to the experimentally measured transfer curves for the high-V_T operation modes are depicted in Fig. 2, showing a good agreement with the measurements. The key parameters used in the simulation, including band edge parameters, metal work function of source and drain contacts, and tunneling effective masses, are summarized in Table I. Some interesting conclusions can be extracted from this fitting work. First, the current in this transport mode is mostly dominated by the access resistance at the source-channel interface. This is easier to understand with support of the band diagrams, depicted in Fig. 3. Conduction and valence bands, together with electron and hole quasi-Fermi levels are extracted in a cut in the middle of the channel along the transport direction. To keep the right voltage reference, the n-type branch is biased with $V_D = 1.8$ V and $V_S = 0.0$ V, whereas for the p-branch $V_D = 0.0$ V and $V_S = 1.8$ V. In all this analysis, the BG is kept to 0.0 V. When the SG

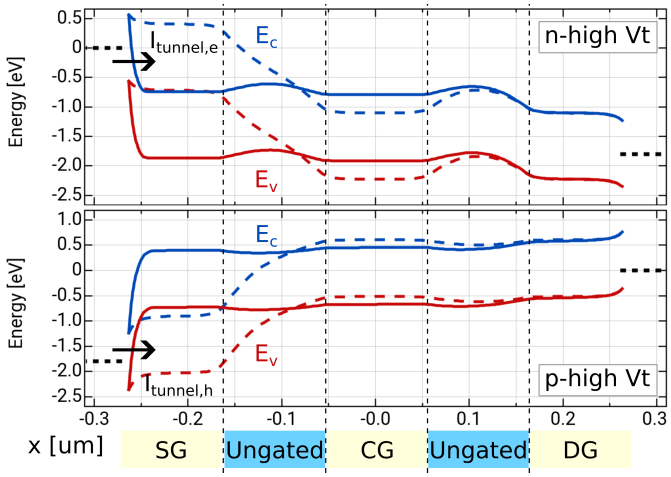

Fig. 3. Band diagrams of the n-type (top) and p-type (bottom) high-V_T transport modes, in on-state (solid) and off-state (dashed)

is activated (low voltage for p-type transport, high positive voltage for n-type), the electrostatic screening length of the mid-gap SBH is reduced for the selected carrier, allowing the tunneling injection through the barrier. As SG is turned off, the screening length is recovered, and the access resistance blocks the tunnelling injection, resulting in a TE-dominated transport. It is noteworthy to mention the impact of the ungated regions. As can be seen, the energy bands bend in those regions, which translates in an insufficient amount of carrier concentration and hence a low conductivity of the channel. Secondly, we can mention that traps close to the source-channel interface have a negative impact on the screening length, decreasing the top gate control. For the n-type transport, this results into a more pronounced dependency of the on-current with the drain bias, and an increase of the off-current. The measurements suggest that p-type transport is significantly influenced by trap dynamics, leading to a noticeable threshold voltage shift in the off-state regime. Moreover, this V_T shift exhibits a clear dependence on the drain-source bias, which may suggest a bias-temperature instability under p-type operation. However, a detailed modeling of this phenomenon is beyond the scope of this work.

The results from the fitting of the transfer characteristics of the device for low-V_T operation mode are depicted in Fig. 4. It is possible to see how the behaviour of the device drastically changes with the configured operation mode. Compared to the previous high-V_T mode, this one has a much smaller subthreshold slope and turn-on voltage, more suitable for logic devices. Again it is possible to visualize in Fig. 5 the band diagrams in on- and off-state for this low-V_T operation mode. Since this configuration fixes the SG and DG bias, to enable the transport of one single carrier, the access resistance is fixed. The conductivity is then controlled by the CG, and the bands resemble more the ones of a regular planar MOSFET. As the device is turned on, the conductivity of the ungated regions changes more drastically compared to the high-V_T case. This

shows how the central gate has a stronger effect on these regions than SG or DG. The use of these tools can be useful in the development of compact models that can be evaluated in SPICE simulations [18]. Alternatively, extended datasets can effectively be generated using the TCAD tool to generate Verilog-A table models. These outputs can be further applied to effectively extract important Key Performance Indicators (KPI) from complex analog and digital circuits [19], [20].

IV. Geometry Exploration

Since this device was purposedly fabricated in a bigger scale to account for the design rule constraints of the underlying baseline technology [21], it is interesting to show in advance some estimates of the performance when certain elements are scaled down to find optimal design choices not yet possible in fabrication.

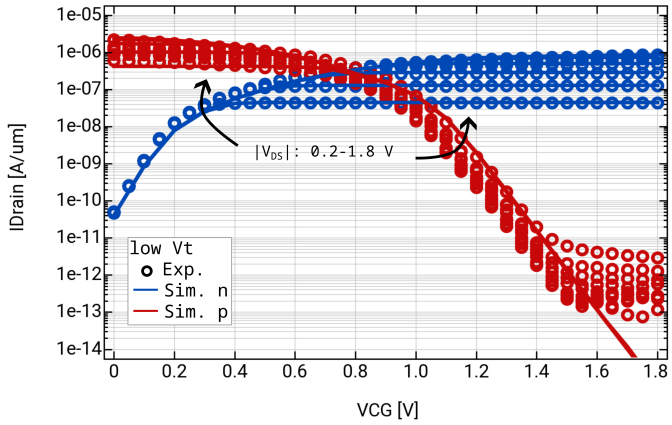

Fig. 4. TCAD simulation fitting to experimental transfer curves at different drain voltages in the low-V_T regime. In this case, the bias of SG and DG gates is fixed, whereas the CG is swept. The impact of the Schottky barrier, direct tunnelling and bulk traps is considered.

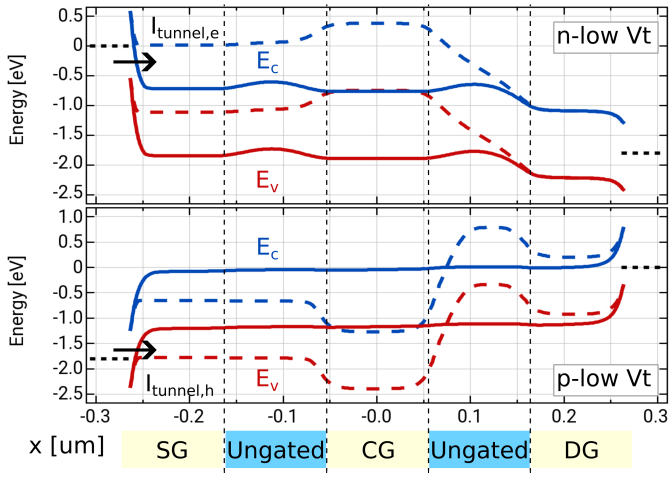

Fig. 5. Band diagrams of the n-type (top) and p-type (bottom) low-V_T transport modes, in on-state (solid) and off-state (dashed). The band profile is more similar to the one of regular planar MOSFETs.

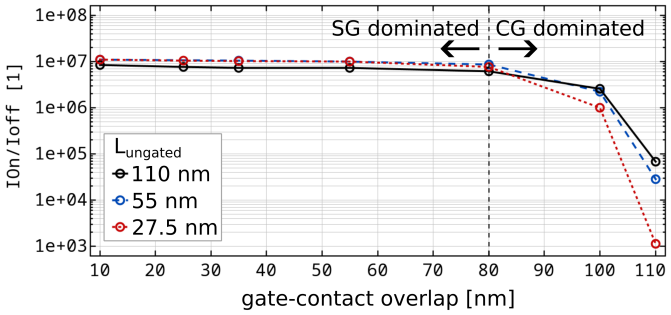

Fig. 6. Ion/Ioff ratio in the nbranch, high-V_T operation mode vs. gate-contact overlap ($L_{contact}$) for different ungated regions lengths ($L_{ungated}$). The dotted line highlight the transition point at which the access resistance control is not dominated any more by the SG.

Here we investigate how the on- and off-current performance are affected by the scaling of the ungated region length ($L_{ungated}$) along with the overlapping of the source/drain contacts with SG/DG ($L_{contact}$). For this analysis, we consider the n-type, high-V_T operation mode. We evaluate the I_{on} current for all gates biased positively to 1.8 V. The I_{off} current is extracted for the case that SG voltage is set to 0.0 V. The results depicted in Fig. 6 show how the I_{on}/I_{off} currents ratio can be improved as the ungated regions are made shorter. When they are short enough, the top gates can generate a high enough electrostatic doping in these regions, minimizing the series resistance and increasing the on-current. Since this is a Schottky-barrier device, the total resistance of the system is still mainly dominated by the access resistance, and hence an improvement in the conductivity of the ungated regions can have only a marginal benefit over the I_{on} current. However, the shortening of the ungated regions can offer other benefits, such as less exposure to oxide-semiconductor interface traps that limit the electrostatic control of the gates over the channel. It also provides a better control of the fringing fields in the ungated region.

At the same time, placing the contacts too deep ($>$ 80 nm) beneath the SG/DG significantly increases the off-current. This is due to lowered electrostatic coupling with the source gate, which reduces the tunnelling distance in the off-state. It can be better appreciated in Fig. 7a, where the conduction band near the source contact is plotted for two different contact overlap distances, 10 and 110 nm. Notice that the bands have been shifted to align with the source contact position, so the differences can be better appreciated. In this case, it is possible to see how SG is effectively suppressing the I_{off} tunnel current when there is a moderate contact-gate overlap. This effect becomes even more pronounced with shorter ungated regions. Similarly, the impact of the contact-gate overlap can be seen by analyzing the conduction band in the on-state, depicted in Fig. 7b. It is shown that there is a slight increase in the screening length, which has an impact in the final I_{on}. This difference in the bands, despite small, made that the I_{on} changed by a factor of 15 for the plotted conditions.

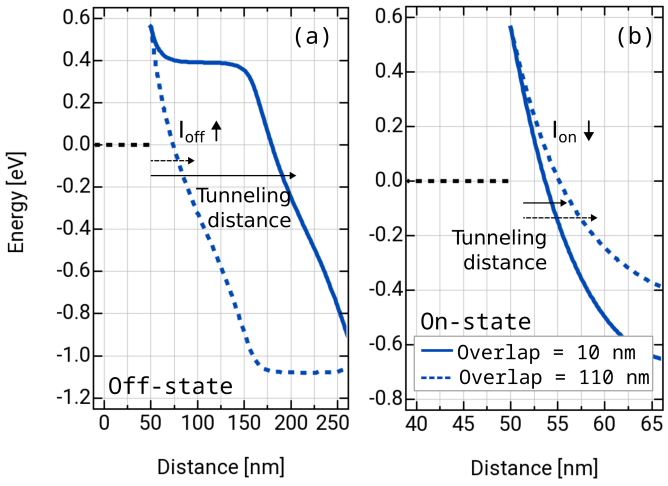

Fig. 7. Band profiles along the channel departing from the source contact position for the n-branch high-V_T operation mode in (a) off-state and (b) on-state. Comparison of the bands for two different contact overlap with the source gate, 10 nm (solid lines) and 110 nm (dashed). Both cases are for the longest (110 nm) ungated regions.

TABLE I
SIMULATION PARAMETERS FOR THE HIGH-V_T TIG-RFET

Parameter	Value
S/D metal work function (eV)	4.61
Si electron affinity (eV)	4.05
Si bandgap energy (eV)	1.12
Tunneling effective mass: m_e / m_h (m_0)	0.1 / 0.08

V. CONCLUSIONS

We have calibrated a semi-classical TCAD simulation flow with experimental measurements of FDSOI TIG-RFET devices for both n- and p-branches in high-V_T and low-V_T operation modes. The simulations show the impact of the Schottky barrier and the ungated regions on the transport, and correctly captures the different behaviour in all the studied transport regimes. This flow can be used to study and optimize key parameters that determine the device performance, such as the gate-contact overlap or the length of the ungated regions.

VI. ACKNOWLEDGEMENT

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