Performance Evaluation of Low Temperature Source/Drain Epitaxy Process Targeting Contact Resistance Scaling for Advanced Gate-All-Around Technology

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***Abstract*—In this work, we evaluate the device and circuit-level performance impact of integrating a novel contact resistivity (ρ_C) scaling scheme for the 2 nm generation of Gate-All-Around technology by deploying our calibrated MSCO^{TM} modeling platform. A sub 10^{-9} Ω.cm^2 ρ_C was reported in [1] by using a low-temperature highly Boron-doped SiliconGermanium (SiGe:B) epitaxial process. Our analysis shows 2% to 3% iso-power circuit performance improvement and 4% iso-performance circuit power reduction as a direct consequence of the Front-End-of-Line (FEOL) transistor drive-strength improvement without penalizing subthreshold performance.**

***Index Terms*—Gate-All-Around, GAA, Contact Resistivity, Epitaxial Growth, Ring Oscillator, DTCO**

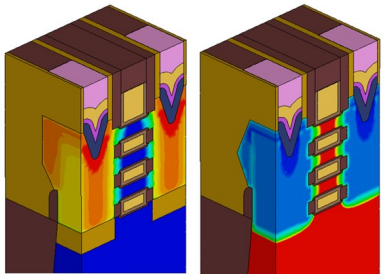
I. Introduction

With the continued scaling of logic technology evolution, the critical dimension (CD) of the source/drain contacts is scaled proportionately resulting in a fast-emerging resistance bottleneck for transistor drive-strength. At the projected Contact CD for the 2 nm GAA technology node (Fig. 1), the Si-Silicide contact interface resistance (indicated as R_C in Fig. 2) is a substantial performance limiting-factor. Effective reduction of the contact interface resistance (typically a Silicon-Silicide interface), either through contact surface-area enlargement and/or through contact resistivity reduction via materials innovation, is critical for scalability of CMOS technology.

Device design innovations to increase Si-Silicide interface area include cavity shaping [1] or employing wrap-around contacts [2]–[4] that maximize the contact Silicide coverage of the Epi facets. Materials innovations thus far have focused on developing and integrating silicides with increasingly lower Schottky barrier heights. Titanium silicide (TiSi) material integration strategies have been deployed and demonstrate contact resistivities near 10^{-9} Ω.cm^2 [2], with further materials such as Scandium Silicide (ScSi) under consideration [5], [6]. However, the integration of new metallic silicide materials faces significant challenges to address thermal stability and process compatibility issues with current CMOS FEOL integration. To further address the contact resistance bottleneck, a selective highly-doped SiGe:B epitaxial process technique, compatible with current state-of-the-art silicides, was developed [1] to enable PMOS contact resistivities below 10^{-9} Ω.cm^2 as shown in Fig. 3(a). The low thermal budget requirements of this epitaxial growth allow for high level of active dopants (2e21 cm^{-3}) without exacerbating dopant diffusion into the channel region, thereby maintaining good subthreshold performance. In this work, we integrate this scheme into the 2 nm GAA node through calibrated process modeling and evaluate the performance impact at the FEOL device and ring-oscillator circuit-level using our comprehensive Materials to Systems Co-Optimization (MSCO^{TM}) [7] framework.

2 nm Gate-All-Around Structure and Dimensions

(a) nMOS (b) pMOS (c) Key dimensions



Parameter	Value
L_{Gate}	12 nm
CPP	45 nm
Nanosheet Width	25 nm
Nanosheet Thickness	5 nm
Spacer Width	5 nm
Contact CD	13.5 nm

Fig. 1. Device structures of (a) nMOS and (b) pMOS GAA transistors at the 2 nm technology node, along with (c) key device dimensions.

II. Modeling Framework

The 3-nanosheet stack GAA transistors (Fig. 1) used in this study are designed with the typical dimensions projected for the 2 nm technology node. The FEOL transistor-level performances are characterized using advanced drift-diffusion transport models calibrated to the self-consistent solution of the Schrodinger, Poisson and subband Boltzmann transport equations [7], [8]. The Contact Epi process is modeled as a selective SiGe (or Silicon, for nMOS) isotropic etch, and low temperature epitaxial regrowth to capture the resultant dopant profiles. Fig. 3 illustrates these key steps and contrasts them with the POR contact-implant process. The interface-doping dependent contact resistivity model (Fig. 4) is calibrated to

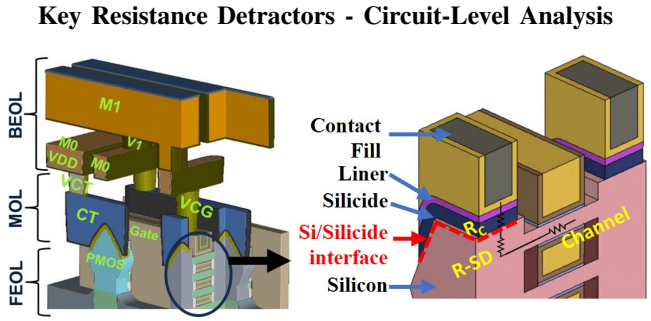


Fig. 2. Key FEOL/MOL/BEOL contributors for 2 nm GAA technology. Silicon-Silicide Interface resistance contributes a considerable portion of the total resistance.

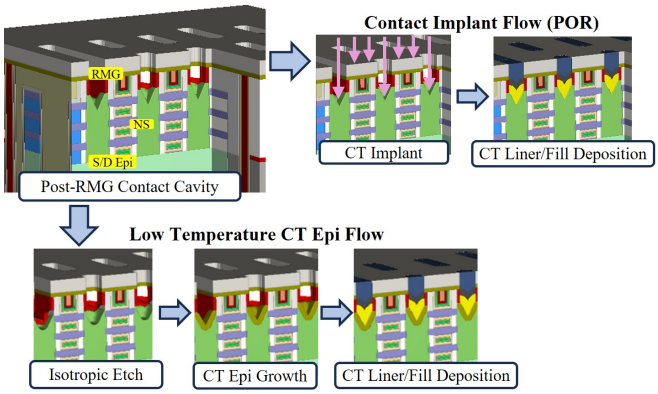


Fig. 3. Comparison of Contact implant process flow vs. Low Temperature Contact Epi process.

in-house experimental data [1]. Finally, we project the performance impact at the circuit level of using the low-temperature contact Epi scheme for both pMOS and nMOS. Compact models calibrated to the aforementioned FEOL characteristics are used, together with detailed MOL/BEOL modeling and

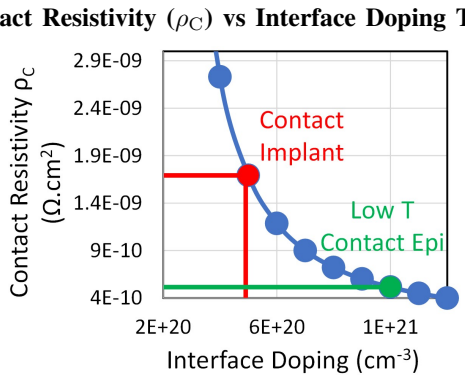


Fig. 4. Contact resistivity scaling trend with interface doping concentration. Conventional contact implant enables ρ_C of 1.5e-9 $\Omega.cm^2$. Low-Temperature Contact Epitaxial process, established in [1], enables sub 1e-9 $\Omega.cm^2$ ρ_C.

parasitic extraction (PEX).

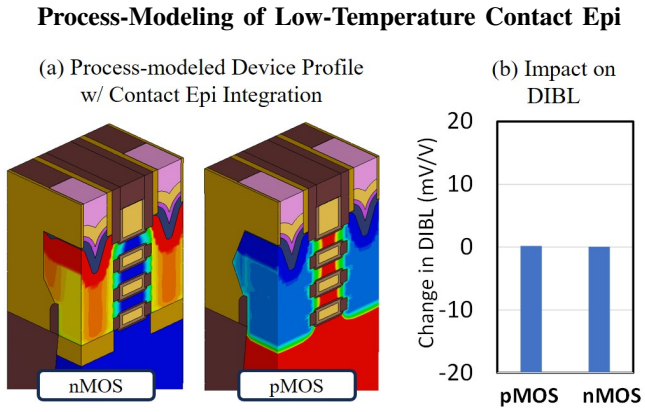


Fig. 5. (a) Process-modeled GAA profiles with low-temperature Contact Epi process integration. (b) Proposed Contact Epi process allows for high dopant activation near Silicon-Silicide interface without penalizing device electrostatics.

III. Results and Discussion

Figure 5 shows the final nMOS and pMOS profiles, following the low-temperature contact epi flow highlighted in Fig. 3. For the pMOS device, the highly doped SiGe:B contact Epi results reduce the Si-Silicide interface resistance (R_C) by 55% compared to the contact implant POR in Fig. 6a. The R_C reduction is primarily an impact of the ρ_C reduction with increase in interface doping. The isotropic etch done prior to contact Epi deposition compensates for any change/reduction in interface area with this process. Moreover, the net higher epi doping also results in a 6% reduction in the Source/Drain (SiGe) resistance. Overall, a 7% improvement is seen in the pMOS FEOL total resistance (R-On).

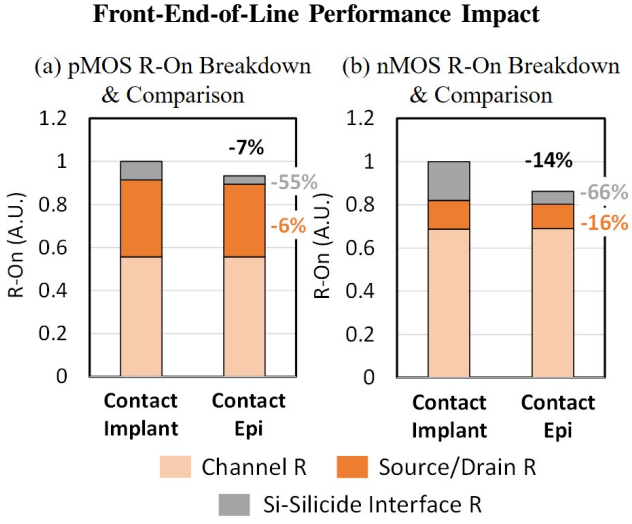


Fig. 6. (a) pMOS R-On breakdown shows 7% R-On improvement with low-temperature Contact Epi due to reduction in Si-Silicide interface resistance (R_C) and S/D bulk resistance. (b) Low temperature Phosphorus-doped contact Epi (Si:P) can lead to 14% improvement in nMOS R-On.

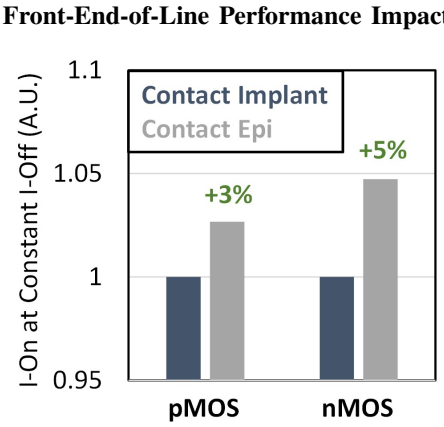


Fig. 7. 3% and 5% improvement in drive-current I-On (measured at fixed target I-Off) for pMOS and nMOS, respectively, with low temperature Contact Epi scheme.

Additionally, we consider the performance impact of using a low-temperature highly-doped Si:P contact epitaxial growth process [9] for nMOS ρ_C scaling. In this case, a 66% R_C reduction was obtained, leading to a more substantial 14% reduction in R-On (Fig. 6b), since R_C makes up a greater proportion of total R-On for nMOS versus pMOS. In both cases, any change to the DIBL or other subthreshold characteristics was negligible (Fig. 5b), highlighting the associated low thermal budget as a critical differentiating factor of the proposed contact Epi scheme. The final enhancements to device drive-current I-On (measured at constant I-off) are 3% for pMOS and 5% for nMOS in Fig. 7.

For a more extensive benchmarking analysis of this combined contact epi scheme, the impact on the inverter ring-oscillator (RO) in Fig. 8a was investigated. To evaluate the circuit-level impact of the contact epi process, Iso-V_{DD} Inverter RO Performance was extracted in Fig. 8b. The integration of this pMOS contact epi process alone was found to result in 1.5% performance enhancement due to the reduced pMOS R-On. An additive 3% enhancement of iso-V_{DD} RO performance was determined with both pMOS and nMOS contact epi processes. Additionally, the combined impact on performance and power was investigated for both the inverter and more complex AOI-based RO circuits. At constant power consumption, a similar 2% increase in performance was seen for the inverter and AOI based RO (Fig. 9). At constant performance, 4% and 5% reductions in power were seen for the inverter and AOI cases, respectively, (Fig. 10) indicating

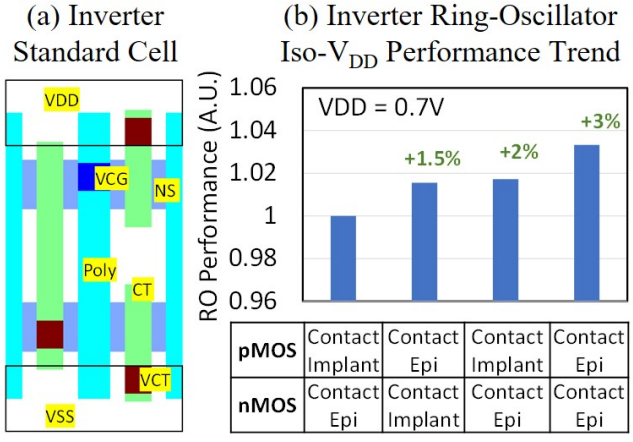


Fig. 8. (a) Inverter standard cell layout used for performance projection. (b) Inverter-based Ring-Oscillator (RO) performance impact of contact implant vs contact Epi schemes. 3% performance improvement is obtained at fixed V_{DD} with Contact Epi scheme integrated in both pMOS and nMOS.

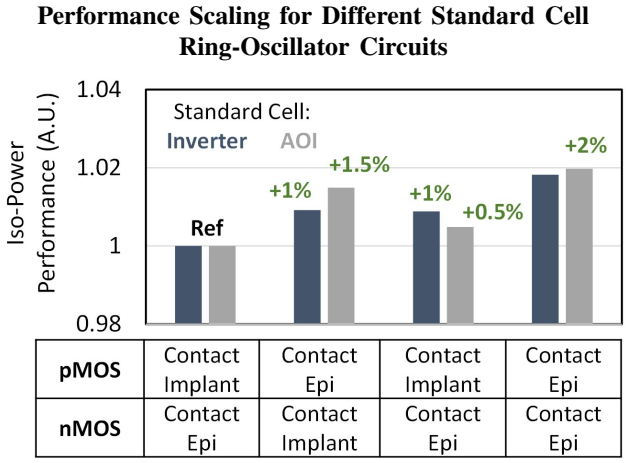


Fig. 9. Iso-Power RO Performance improves with low-temperature contact Epi scheme, showing additive benefits of incorporating it in both nMOS and pMOS and highlighting value for high-performance compute. Similar performance trend for more complex cells like AOI

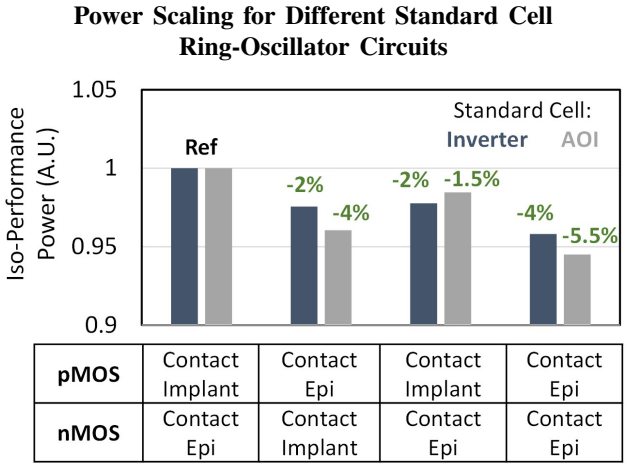


Fig. 10. Iso-performance RO power reduces by upto 4-5% with low-temperature contact Epi integration, highlighting its value for low-power AI applications. Moreover, power efficiency/reduction is further improved with increasing complexity (transistor count) of the standard cell.

that the benefit of the contact epi scheme scales with increasing cell complexity. Fig. 6 also highlights that, for complex circuits like AOI, the contact Epi scheme for pMOS provides relatively more optimized power versus performance scaling benefits compared to the nMOS.

IV. Summary

In summary, we have shown that the proposed low temperature Contact Epitaxy scheme to improve GAA R_C can result in a drive strength improvement of over 3% at the transistor-level and up to 2% performance improvement (at same power) and 4-5% power reduction (at same performance) at the ring-oscillator circuit-level. The study demonstrates that the low-temperature contact epitaxial growth process can significantly improve Source/Drain contact resistance and is a useful knob for enabling power-efficient performance scaling of advanced GAA technology nodes.

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