Novel Block-Level DTCO Solution for Advanced Logic Technology Path-Finding

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***Abstract*—We introduce the novel Block-level DTCO solution which can resolve the difficulty of block-level PPA estimation in path-finding stage. Four remarkable newly developed technologies have been integrated to enable TCAD-based evaluations with a short turn-around-time, even in the absence of a PDK. In addition, it is applied to sub-3nm logic technology development for the first time, and we have identified that differences in cell types and BEOL assumptions used in cell-level evaluation induce a performance gap between block-level and cell-level. Finally, our novel solution has improved block-level PPA through DTCO in the early stages of product development.**

Keywords— Block-level DTCO(Design-Technology-Co-Optimization), Path-Finding, PPA(Performance-Power-Area), TCAD(Technology-Computer-Aided-Design)

I. Introduction

Since device performance has not directly been linked to product performance due to parasitic RC impact increase in sub-14nm technology, standard cell Performance-Power-Area (PPA) evaluation and its cell-level Design-Technology-Co-Optimization (DTCO) was an inevitable technique for product PPA targeting. However, cell-level PPA has not been able to represent a product in sub-3nm technology because of Back-end-of-Line (BEOL) wire impact increase, and design scheme complexity. In order to develop competitive product in such Angstrom technology era, block-level PPA evaluation and optimization range expansion from device to further larger circuit/block/system, so-called Block-level DTCO, is an essential solution to initiate a future path-finding [1-3].

Although conventional Electronic Design Automation (EDA) tool based block-level PPA evaluation is a common flow, its application for advanced technology is unavailable because EDA tools cannot support the disruptive structures that are the principal DTCO objectives for sub-3nm nodes. There are numerous technology paths to be studied, such as backside contacts [4] and three dimensional stacked devices [5]; therefore, an innovative solution to flexibly evaluate the block-level PPA of these disruptive technologies has been eagerly awaited. In this paper, we introduce the Block-level DTCO solution to deal with the advanced technology node even in the absence of Process-Design Kit (PDK). Technology Computer-Aided Design (TCAD) is extensively utilized for physical and various types of scheme evaluations in pathfinding for advanced technology nodes.

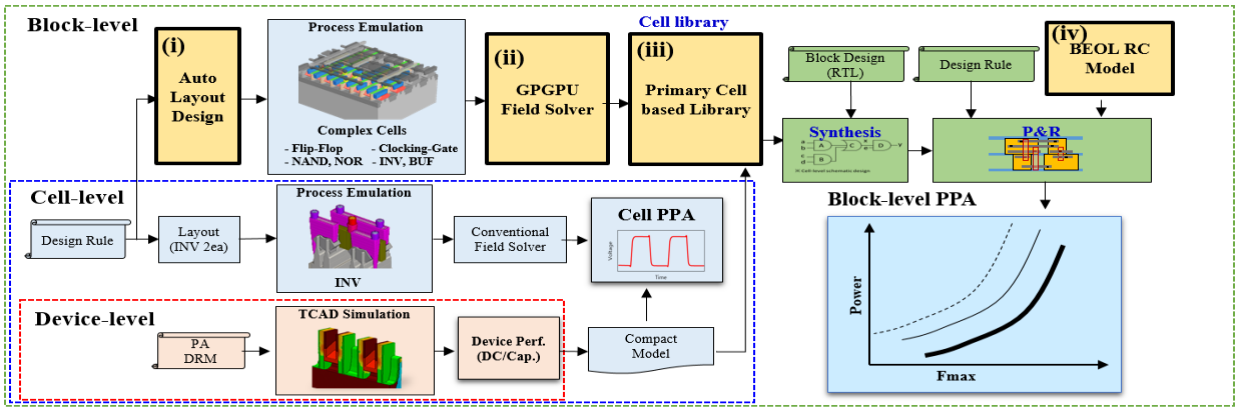


Fig. 1. The Flow diagram of Block-level iDTCO.

II. Solution Development

Figure 1 shows novel block-level DTCO flow diagram, named as "Block-level iDTCO". In addition to conventional cell-level iDTCO [6], three major steps, Cell library creation Logic Synthesis / P&R (Placement and Routing), have been successfully established to obtain block-level PPA. 3D-Emulation and parasitic RC extraction with the field solver are applied to all standard cells, and generated parasitic resistance and capacitance netlists of each standard cell are used for cell-level performance and power simulation through SPICE in order to obtain the cell library. The cell library is Look-up-Table style delay and power library and integrates all of standard cell. It is turned into input data of block performance evaluation.

Figure 2 describes metric differences between cell and block-level evaluation. While cell-level evaluation is only limited standard cell type with typically routed loading metal assumption, block-level evaluation involves up to 1K cells and actual routed metal, which can have a significant impact on the final product. Furthermore, four remarkable technologies are newly developed and integrated for use in the initial development stage: (i) Automated cell layout design, (ii) GPGPU based field solver, (iii) Primary cell sampling, (iv) TCAD based BEOL model for P&R.

A. Automated Cell Layout Design

Figure 3(a) illustrates the automated cell layout generation process, a critical step in the design process. The input includes the cell netlist, design rules, device architecture, and Power Delivery Network (PDN) scheme, providing necessary information for the tool to create optimized standard cell layouts. Through automatic transistor placement and metal routing techniques [7], the tool generates standard cell layouts that meet specified design requirements. The automated transistor placement and metal routing algorithms optimize transistor placement and connections. The resulting standard cell layouts are compiled, providing a foundation for further design and optimization, and enabling efficient creation.

B. GP-GPU Based Field Solver

Cell-level performance relies on device performance and parasitic RC. TCAD device simulation informs the compact model, and parasitic RC is extracted using a field solver that solves the Poisson equation for 3D structures. Although accurate, this method has a longer Turn-Around-Time (TAT) due to 3D matrix solving. To address this, we've developed PFS, a new field solver with a GP-GPU based matrix solving engine and agile discretization algorithm [8]. PFS achieves a 12.6x TAT reduction compared to conventional CPU-based field solvers, as shown in Fig. 3(b), while maintaining accuracy.

C. Primary Sampling

The third feature is a primary cell sampling technique to optimize the number of standard cell with keeping the accuracy and run time for DTCO purpose. A lager number of core cell can improve the block-level PPA, however cell library development time, such as cell layout development netlist generation library creation, would increase and disturb quick DTCO. So we carefully evaluated and minimized the number of standard cells which is able to maintain the PPA accuracy compared to the product library (~1K cells), as shown in Fig. 4(a). It shows clearly that increasing the cell number can result in better PPA. Through cell sampling techniques, we have determined 40 cells which can maintain a PPA accuracy over 95% with product-level library.

D. TCAD Based BEOL Model

The final new solution is the generation of a TCAD Emulated 3-dimensional structure based BEOL RC model for P&R. The advantage of TCAD based BEOL RC model is its ability to simulate realistic corner-rounding and sloped metal/via structures, as well as dimension dependent resistivity models. Scaling a metal dimension in advanced technology can induce additional grain boundary scattering, which makes larger resistance. Therefore, including its impact on block-level evaluation is inevitable. Figure 4(b),(c) shows wire area dependent resistance trend for various metal materials. Since each material has a different resistance dependency on wire area, the optimum material needs to be considered in conjunction with design rules and block-level PPA through DTCO.

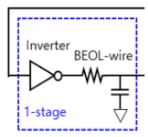
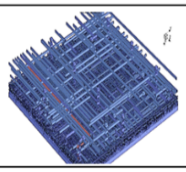
	Cell-level	Block-level
Circuit	Ring Oscillator	Blocks in CPU/GPU Core
FEOL/MOL	INV	Cell Library
BEOL	Pre-defined Portion of Metal Usage	Actual Routed Metal
		

Fig. 2. Comparison between Cell-level and Block-level evaluation metric.

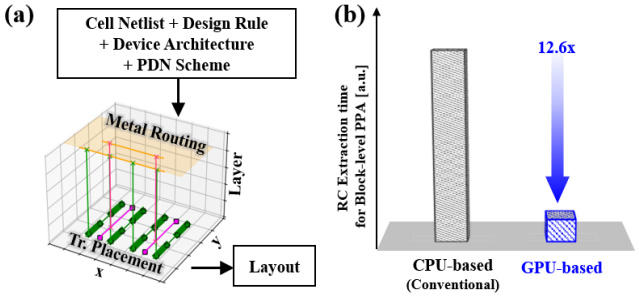


Fig. 3. (a) Automated standard cell layout generation flow. (b) TAT reduction for parasitic RC extraction.

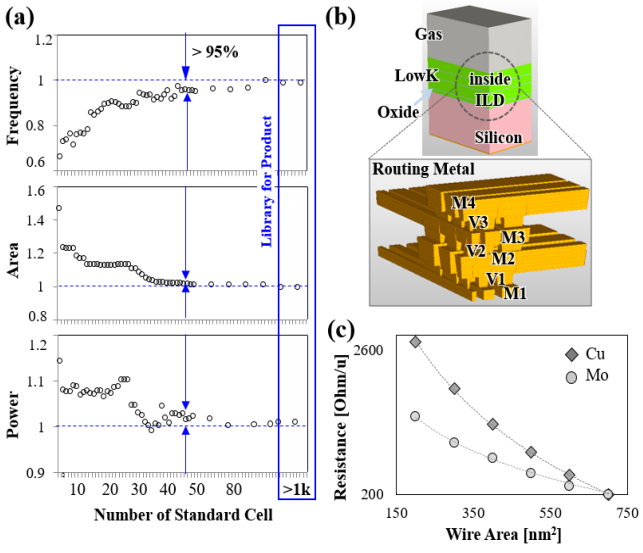


Fig. 4. (a) Primary core cell sampling methodology, (b) TCAD Emulation structure and (c) BEOL wire model for Block-level DTCO.

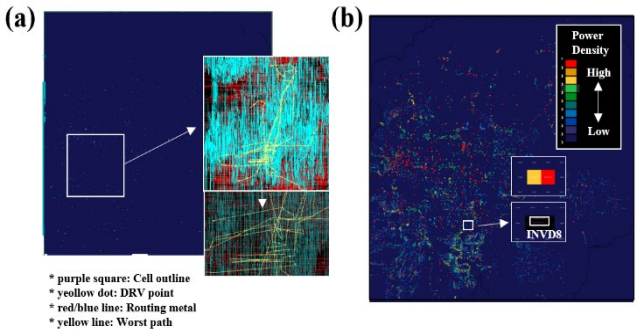


Fig. 5. A block designed for the evaluation of (a) Fmax and (b) Power at the block-level.

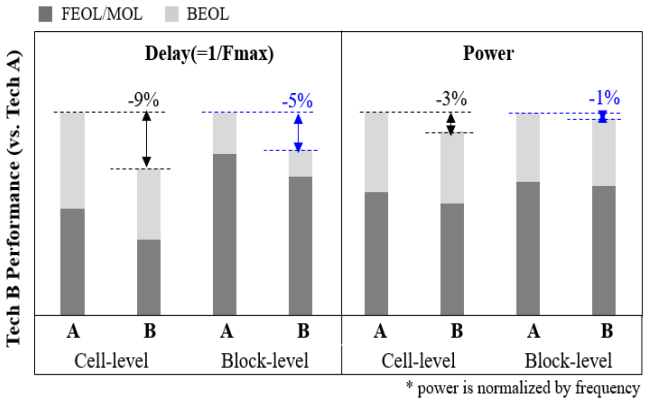


Fig. 6. Delay & Power evaluation of Tech A and B at both the Cell-level and Block-level, respectively.

III. Results & Discussion

A. Block-level vs Cell-level Performance Comparison

Utilizing the new solution, we conducted a comprehensive evaluation of the cell-level and block-level performance and power of two distinct technologies. To assess cell-level performance, we measured the oscillation frequency of a 17-stage Ring Oscillator (RO) comprising Inverter cells. The oscillation frequency served as a key metric for evaluating the intrinsic performance capabilities of the individual cells.

For block-level performance evaluation, we used the maximum achieved frequency, Fmax, as a metric. Fmax was determined by adjusting the clock period to achieve zero slack across the worst 300 paths, with the inverse yielding the achieved frequency. A Floating Point Unit (FPU) block was used to evaluate Fmax due to its complexity. The block-level power consumption was evaluated at Fmax, as shown in Fig. 5, providing a realistic representation of power requirements. This evaluation enabled a thorough understanding of the performance and power consumption characteristics of the technologies under consideration.

Both Technology A and Technology B employ a Gate-All-Around (GAA) architecture, with differences in Front-End-Of-Line (FEOL) and Middle-Of-Line (MOL) related technologies. As illustrated in Fig. 6, the block-level performance and power improvement in Technology B is substantially less pronounced compared to its cell-level improvement. This disparity can be attributed to two primary factors: the types of cells utilized and the Back-End-Of-Line (BEOL) routing metal characteristics, as depicted in Fig. 2. To understand the underlying causes, we analyzed the FEOL/MOL and BEOL components of the total delay. The analysis revealed that Technology B's subpar block performance was due to limitations in both FEOL/MOL and BEOL. Both components contributed to the degradation in block-level performance, highlighting the need for a comprehensive evaluation of the technology's capabilities. This finding emphasizes the importance of considering both cell-level and block-level performance when assessing a technology's overall efficacy.

B. Analysis and Block-level DTCO

Figure 7(a) shows that NAND and NOR cells are predominantly used in the worst path group, whereas Inverter (INV) cells are less frequent, highlighting a potential mismatch between cell-level and block-level evaluation. Technology B exhibits weaker NAND and NOR cell performance compared to Technology A. To address this, a Vth adjustment strategy was implemented, enhancing NAND cell performance (Fig. 8) and yielding a 2% block-level performance gain (Fig. 7(b)).

To investigate BEOL's impact on block-level performance and power, we analyzed the contribution of each BEOL layer. Near BEOL layers significantly affect performance, while mid BEOL layers impact power consumption (Fig. 9(a)). A sensitivity analysis to wire R/C of each BEOL layer (Fig. 9(b)) identifies key layers for optimization, enabling additional performance gains through metal and via height optimization based on Fmax sensitivity.

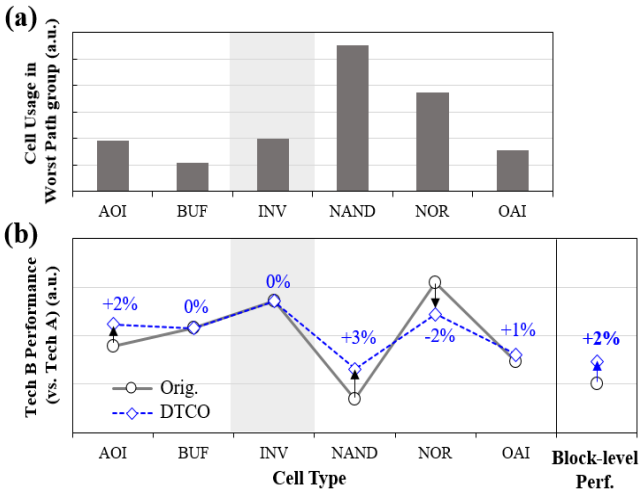


Fig. 7. (a) Cell usage in Block, (b) cell-by-cell performance comparison of Tech B vs. Tech A, and DTCO performance booster by N/P re-balancing and Idlin enhancement.

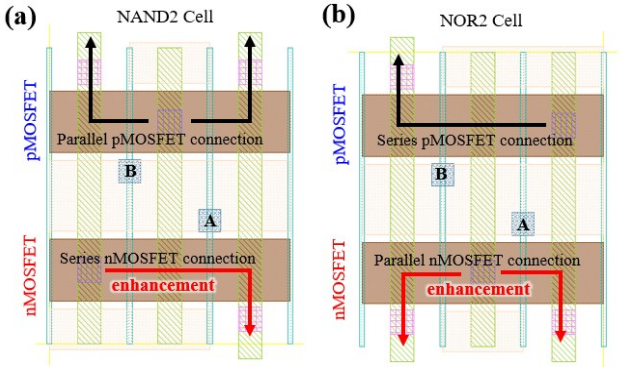


Fig. 8. Layout and the circuit topology of the minimum drive strength for the (a) 2-input NAND cell and (b) 2-input NOR cell.

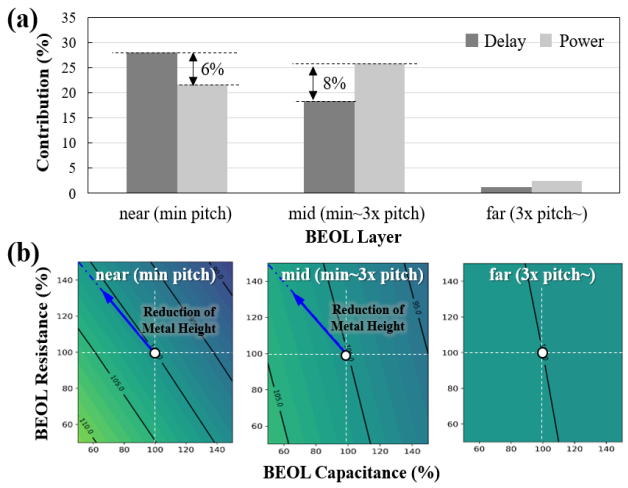


Fig. 9. (a) Contribution of BEOL Layer in Delay and Power in Block. (b) Fmax sensitivity with respect to the BEOL RC change.

IV. Conclusion

For the first time, a block-level DTCO solution was developed and introduced during the early stages of technology definition. This pioneering approach enabled the evaluation of block-level performance and power based on TCAD simulations, even during the initial logic technology development phase. By leveraging this capability, we were able to assess the impact of various cell types and BEOL routing on block-level performance, which was not feasible with traditional cell-level evaluations. Through the application of block-level DTCO using our solution, we successfully achieved a significant improvement in block-level performance by optimizing both cell and BEOL performance. This accomplishment demonstrates the effectiveness of our approach in maximizing the potential of emerging technologies. In the context of Angstrom dimension pathfinding, our block-level DTCO solution is poised to play a crucial role in enabling the development of competitive technologies. By providing a comprehensive and accurate assessment of block-level performance and power, our solution can help guide the development of next-generation technologies, ultimately paving the way for innovative applications and advancements in the field.

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