Process-Performance Variability Modeling of Inner Spacer Etch in GAA FETs

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***Abstract*—This work presents a robust machine learning (ML) framework for modeling the inner spacer etch process and its impact on electrical behavior in gate-all-around (GAA) FETs. Leveraging an in-house Process Monte Carlo (PMC) simulator, the etch front evolution under diverse process conditions is simulated. Gaussian Process Regression (GPR) demonstrates superior accuracy (98.5%) in modeling inner spacer etch process. Artificial Neural Networks (ANNs) are employed to map inner spacer etch geometric variations to device current characteristics with 98.2% accuracy. The proposed ML pipeline establishes a direct process-to-device link, enabling accurate assessment of electrical performance variations, and paving the way for data-driven process-performance co-optimization in advanced transistor technologies.**

***Index Terms*—gate all around FETs, inner spacer etch, particle monte-carlo, GPR, ANN, process variation, NSFET**

I. Introduction

Gate-All-Around (GAA) Field-Effect Transistors (FETs) have emerged as a leading architecture to extend CMOS scaling beyond the 3nm technology node [1], [2]. Their enhanced electrostatic gate control offers improved device performance and energy efficiency compared to FinFETs. A critical ad challenging step in the GAA FET fabrication is the inner spacer etch process, which involves the selective partial removal of SiGe to form nanoscale indents between stacked silicon nanosheets [3]. The highly selective chemical etch [4], [5] used in inner spacer etch is sensitive to interdependent process conditions like temperature, pressure, flux, and time, making predictive modeling challenging. Variations in this step directly affects key geometrical parameters such as gate length (L), spacer thickness (t_{sp}), and gate-to-source/drain isolation, which ultimately impacts both static and dynamic electrical performance. A representative GAA nanosheet FET (NsFET) structure is shown in Fig. 1.

Despite the clear connection between these etch-induced variations and their impact on device performance, current research often remains siloed between isolated process study and device analysis. The process side, focused on etch outcomes, operates largely independently from device simulations, which assess electrical performance. This disconnection makes it difficult to establish a clear, direct route from process parameters to device-level electrical outcomes, leading to resource intensive, costly, slow and cumbersome optimization cycles. To address this, we propose a ML-based framework that captures the complex inner spacer etch process dynamics and links process variations directly to device-level electrical behaviour, enabling accurate process-to-device variation modeling.

This work was supported in part by the Ministry of Education (Government of India) through Prime Minister's Research Fellowship (1701656).

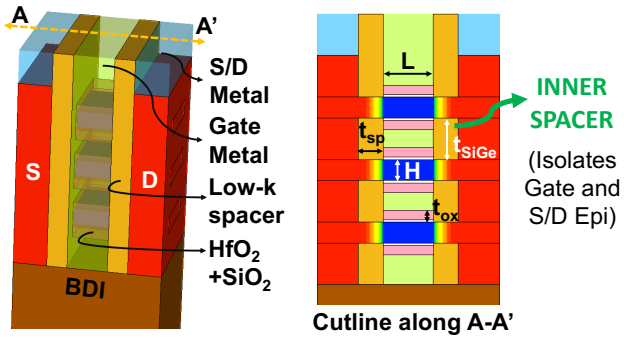

Fig. 1: The schematic diagram of the three-sheet-stacked NsFET. Cross-section across A-A' of NsFET shows the inner spacer with thickness t_{sp}, gate length L, gate oxide thickness t_{OX}, sheet thickness H and sheet-to-sheet spacing of t_{SiGe}.

II. Simulation Setup

A calibrated in-house voxel-based Particle Monte Carlo (*nanoPMC*) simulator is used to model the inner spacer etch process, incorporating incident particle energy, angular distributions, and surface reaction probabilities (Fig. 2). The simulator is calibrated using experimentally reported etch rates and spacer profiles from [4], [5], with calibration details provided in [6]. The key process parameters considered include neutral particle flux (F), temperature (T), etch time (ET), and Ge diffusion (D) during prior STI annealing [5]. The inner spacer etch profile from the nanoPMC simulator is exported into Synopsys TCAD suite for electrical analysis (Fig. 3). The NsFET structure with the imported spacer profile is generated for electrical simulation, with calibrated electrostatic, quantum confinement and transport models [7]. To reduce the dimensionality of the training dataset, the 3D etch front is projected to a representative 2D profile. A design of experiments is used to generate 428 etch profiles per SiGe

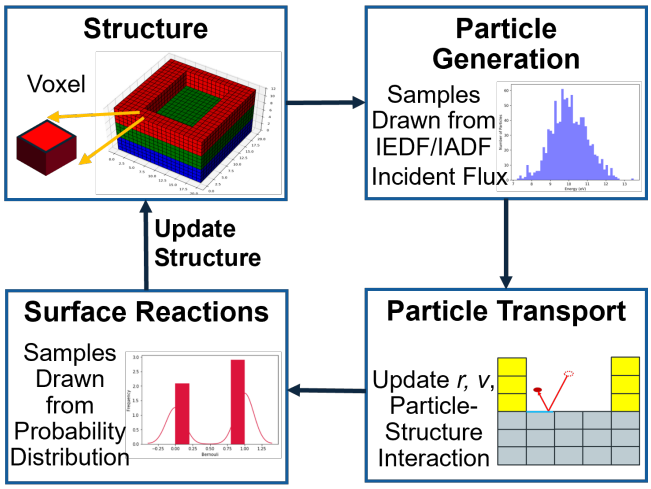

Fig. 2: In-house voxel-based 3D Particle Monte Carlo (*nanoPMC*) simulator workflow. Samples are drawn from energy (IEDF) and angular (IADF) distributions during initialization of particles. Surface reactions are executed based on reaction probabilities, sampled with Monte Carlo algorithm.

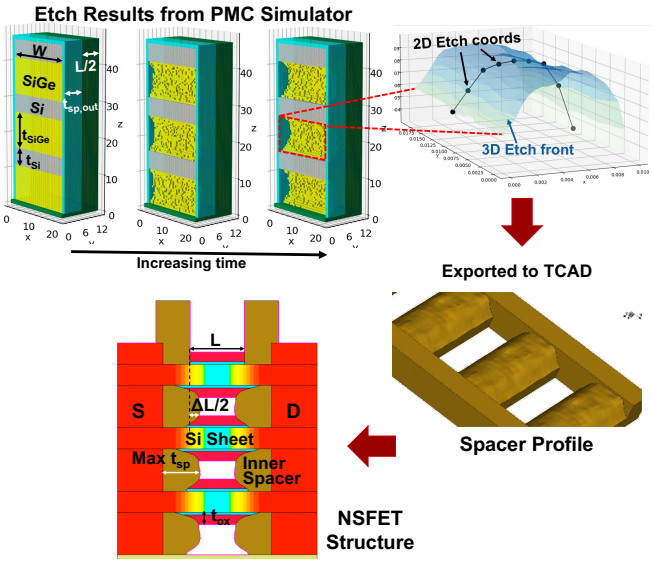

Fig. 3: Simulation flow for generating process-device training data. NsFET inner spacer etch process results from PMC simulator are extracted in form of a 3D etch front. The etch front is exported to Synopsys TCAD, to create the spacer profile in the 3 sheet NsFET device, which is used for electrical simulation. The 3D etch front is reduced to a mean 2D etch profile for ML process model.

thickness (t_{SiGe}), covering variations in process parameters as listed in Table I. From this dataset, 100 etch profiles are selected for current–voltage simulation in TCAD.

TABLE I: Variation in the process parameters

Parameter	Variation
Flux (F)	$\pm 50\%$
Temperature (T)	$\pm 10\%$
Etch Time (ET)	$\pm 50\%$
Diffusion (D)	$\pm 20\%$
SiGe Thickness (t_{SiGe})	8nm, 10nm, 12nm

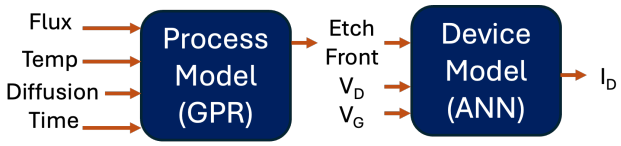

Fig. 4: Process-Performance modeling framework. Process parameters are input to the GPR process model which generated the 2D etch front. ANN device model takes the etch front along with gate (V_G) and drain voltages (V_D) to predict the drain current (I_D).

III. Methodology

A ML based process-device pipeline is setup consisting of separate etch process model and a device electrical model, cascaded to link etch process parameters with device-level electrical behaviour as shown in Fig. 4.

A. Process Model

Modeling the inner spacer etch profile is critical for understanding its impact on GAA FET performance. However, detailed physics-based simulations, such as PMC, are computationally intensive and not viable for rapid process exploration. To address this, we adopt a data-driven approach using Gaussian Process Regression (GPR) to model the inner spacer etch profiles. GPR is a non-parametric, Bayesian regression method, which predicts etch profiles while also quantifying uncertainty, making it well-suited for process variability analysis. Its kernel-based structure captures the complex nonlinear relationship between process conditions and etch front shape, even with limited training data. In this work, we used the Radial Basis Function (RBF) kernel to calculate the covariance (k) between input data points (x).

$$k(x_i, x_j) = \sigma^2 \exp\left(-\frac{||x_i - x_j||^2}{2l^2}\right) \quad (1)$$

where σ^2 is the signal variance, and l is the length scale controlling smoothness. These are optimized by maximizing the log marginal likelihood using the L-BFGS-B algorithm [8]. The resulting GPR model enables fast, accurate, and data-efficient prediction of inner spacer etch profiles across diverse process conditions.

B. Device Model

The drain current (I_D) of the NsFET is modeled using an Artificial Neural Network (ANN), which takes the 2D inner spacer etch front, gate voltage (V_G), and drain voltage (V_D) as inputs. Due to the wide dynamic range of I_D, ranging from nA in the subthreshold region to mA in strong inversion, the

output is transformed into logarithmic scale to reduce variance and improve prediction accuracy in the subthreshold region. However, a small error in logarithmic output would translate to large error on linear scale. Therefore, the loss function which minimizes the relative Root Mean Square (RMS) error on the exponent of the outputs is used [7]. This is given as:

$$Loss = RMS(\frac{e^{y_{true}} - e^{y_{pred}}}{e^{y_{true}}}) \quad (2)$$

This approach ensures robust prediction performance across both subthreshold and above-threshold operating regimes.

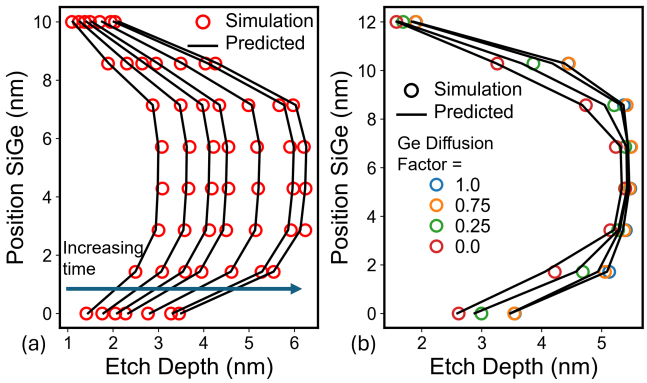

Fig. 5: Simulated and predicted etch front of inner spacer etch for (a) time and (b) Ge diffusion variation. The GPR model can accurately track the etch profile progression. Diffusion variation affects curvature of spacer.

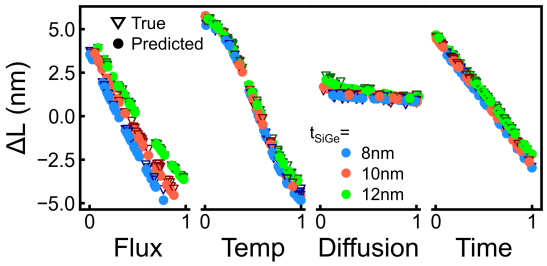

Fig. 6: True and predicted distribution of ΔL for varying process parameters. The GPR model can accurately predict derived geometrical parameters.

IV. Results and Discussion

The GPR model predicts the evolution of etch front with respect to ET and D as seen in Fig. 5. With increasing ET, the entire etch front propogates and maximum etch depth increases, while change in D only affects the curvature of the etch front. Fig. 6 illustrates how change in gate length (ΔL) varies with individual process parameters, aligning closely with ground truth data with an average relative error of 1.5%. ΔL decreases with increase in F, T and ET, due to increase in t_{spr}, which results in shorter L. D does not significantly affect ΔL and shows very slight decreasing behaviour due to

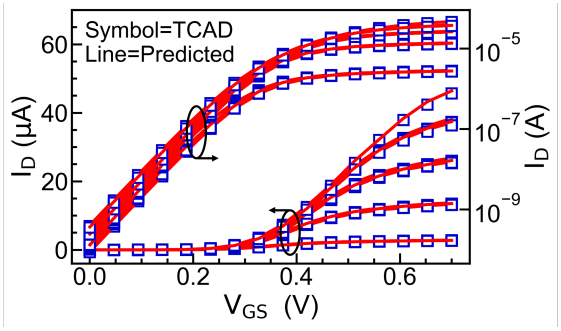

Fig. 7: Validation of transfer characteristics predicted from the ANN device model, with TCAD, across varying inner spacer profiles and terminal voltages. Model is accurate with average relative error of 1.8%.

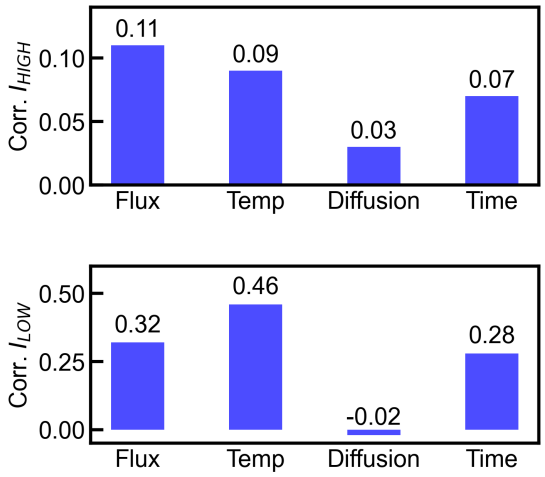

Fig. 8: Correlation of the high current (I_{HIGH}) and low current (I_{LOW}) with the process parameters. I_{LOW} has a stronger correlation with flux temperature and time compared to I_{HIGH}. Diffusion has weak correlation.

the increasing curvature of the etch front. These results confirm the effectiveness of GPR in modeling the inner spacer etch process and its impact on key device dimensions, ensuring robust predictions under diverse parameter variations. The ANN-based device model predicts the I_D for the different bias conditions and various input inner spacer etch profiles generated from the process model. The predicted transfer characteristics ($I_D - V_{GS}$) is validated against TCAD simulations for different etch fronts (Fig. 7), achieving an average relative error of 1.8%. Cascading the process and device models reveals the impact of process variations on NsFET's current characteristics. As shown in Fig. 8, I_{LOW} (I_D at V_G = 0 V and V_D = 0.01 V) shows a strong positive correlation with F, T, and ET, while I_{HIGH} (I_D at V_G = 0.7 V and V_D = 0.01 V) exhibits a comparatively weaker dependence. Fig. 9 validates this correlation by showing the variation of V_{th}, I_{HIGH}, and I_{LOW} with respect to different process

parameters. I_{LOW} exhibits strong sensitivity, varying by up to 85% with etch time and as much as 150% with flux and temperature. In contrast, I_{HIGH} shows limited variation, with a maximum change of 8% across the same process window. V_{th} is extracted using constant current method, with I_{th} computed for a 3 sheet NsFET having a sheet width of 20 nm and sheet thickness of 5 nm, at L = 12 nm. V_{th} decreases with increase in F, T and ET, which is in line with ΔL variation. Ge diffusion has minimal influence on device performance, with variations limited to 5%. Overall, the GPR-ANN-based ML framework accurately captures the impact of inner spacer etch process variations on NsFET electrical characteristics, enabling reliable process–performance variability analysis.

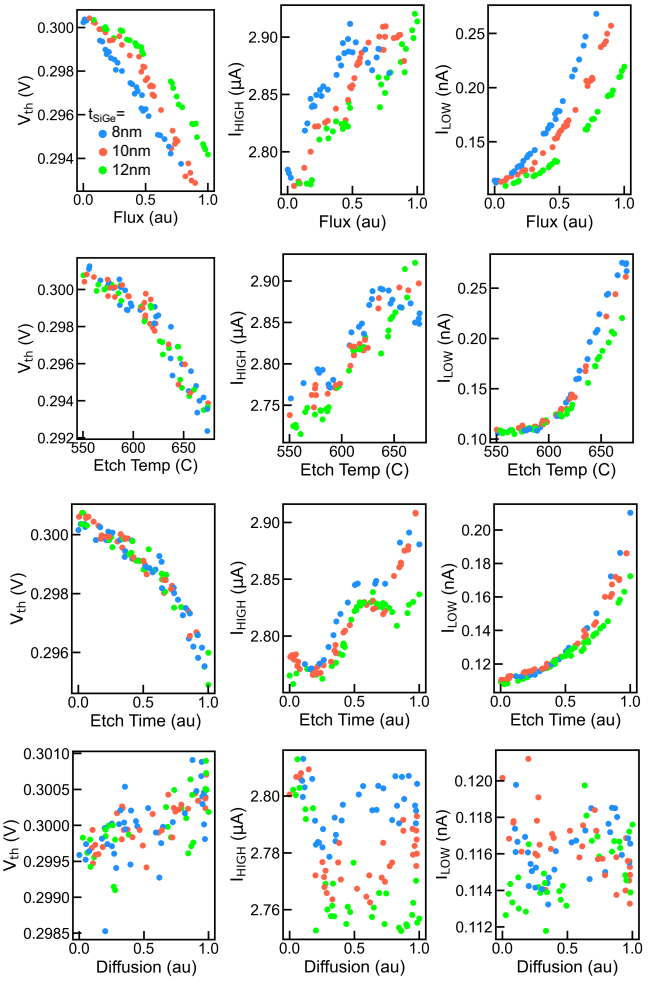

Fig. 9: Variation in I_{HIGH} and I_{LOW} with flux, etch temperature, diffusion factor and etch time. V_{th} and I_{HIGH} have a maximum of 4% and 8% variation respectively across variation in flux, temperature and time. I_{LOW} varies 100-150% with variation in process parameters with a positive correlation. Diffusion factor has less impact on the current variation due to inner spacer etch process.

V. Conclusion

This work presents a machine learning framework that effectively bridges the inner spacer etch process and electrical behavior in GAA FETs. A calibrated PMC simulator is used to generate etch profiles under varying process conditions, which are accurately modeled using GPR. The resulting etch geometries are mapped to device currents through an ANN-based model, enabling direct prediction of I_D characteristics from process parameters. The proposed GPR–ANN pipeline captures the impact of process variations on device geometry (ΔL) and critical electrical metrics such as I_{HIGH}, I_{LOW}, and V_{th}, demonstrating its potential for efficient process-device co-optimization. This framework enables rapid and accurate variability analysis, providing a valuable tool for advanced technology development.

Acknowledgment

The authors thank Dr. Pardeep Kumar and Dr. Samit Barai from Applied Materials India for their technical support in a part of this work.

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