Transport characterization and quantum dot coupling in commercial 22FDX®

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***Abstract*—Different groups worldwide have been working with the GlobalFoundries™ 22nm platform (22FDX®) with the hopes of industrializing the fabrication of Si spin qubits. To guide this effort, we have performed a systematic study of six of the foundry's processes of reference (POR). Using effective mobility as a figure of merit, we study the impact of gate stack, channel type and back bias as a function of temperature. This screening process selected qubit devices that allowed us to couple quantum dots along both the length and width of the Si channel. Simulations provide insights into potential technology optimizations and the advantages of leveraging forward body bias within an FDSOI qubit platform.**

Keywords—FDSOI, forward back biasing, TCAD, quantum dot.

I. Introduction

Significant advances have been made in the field of quantum computing, with the largest test platforms now surpassing a thousand physical qubits [1]. Many of these experimental platforms however are based on technologies that suffer from poor scalability. Leveraging CMOS manufacturing would enable the rapid scale-up of quantum computing hardware. As such, there has been considerable effort in the last 12 years [2] to develop the Si spin qubit and bring it to the 300mm scale. Among the commonly explored Si-based technologies, Fully Depleted Silicon-On-Insulator (FDSOI) has proven to be a promising forerunner [3]. FDSOI has a unique local back gate which offers very strong control over the transistor threshold voltage (V_{TH}). In qubits, this back gate can also control the vertical position along the Si channel in which a quantum dot (QD) is formed, drawing it away from inherent defects at the front-gate Si/SiO_2 interface and reducing the charge-noise associated with interface traps [4]. While some progress has been made to bring FDSOI spin qubits to the commercial scale [5-7], the deep cryogenic temperatures and long measurement protocols necessary to fully characterize qubits can be prohibitive in determining the efficacy and variability of a new process split. Rigorous characterization routines must be developed to screen potential qubit technologies and aid process development. Effective electron mobility is sensitive to many variables within the process flow and can shed light on both material and interface defects [8].

In this work, we present a detailed study on the effective mobility of six process splits from the GlobalFoundries™ 22nm platform (22FDX®), varying channel type, front-gate stack and front-gate equivalent oxide thickness (EOT). We use both temperature and back gate bias along with TCAD simulations to inform our understanding of the process splits and choose the best split and back bias conditions for forming QDs within the integrated qubit structures. Together, our data supports the selection of a thicker gate oxide in NMOS qubit arrays, which displays improved QD coupling relative to what has been reported for thinner gate oxides in 22nm FDSOI [6].

II. Devices and Methodology

All devices were fabricated using the commercially available 22FDX® platform from GlobalFoundries™ with their processes of reference (POR). The buried oxide and silicon channel in this technology are 20nm and 6nm thick, respectively. The commissioned wafers were designed with a wide range of in-wafer and in-die process splits as well as integrated test structures which allowed us to screen several potential front and back gate stacks. The process splits discussed in this study are outlined in Table I. The first is focused on gate stack materials (GS-1 *vs.* GS-2), the second between thin (EOT-1 = 1.25 nm) and thick (EOT-2 = 3.4 nm) gate oxides. These were then tested on both n-type and p-type Si channels. Split C-V test structures were 9µm x 10µm transistors with a local back gate. Two styles of qubit devices were measured in this study: one which contains several gates in series (SR), with a similar design as in [9], and a second 2xN array of split gates in series, often called face-to-face (FF) gates [10].

TABLE I. In die Process Splits

Split	Gate Stack (GS)	Oxide (EOT)	Carrier type
A	GS-1	Thin (EOT-1)	PMOS
B	GS-2		
C		Thick (EOT-2)	
D	GS-1	Thin (EOT-1)	NMOS
E	GS-2		
F		Thick (EOT-2)	

Variable temperature I-V and C-V measurements were collected in a cryogenic Probe Station, using a commercial Semiconductor Device Parameter Analyzer and LCR-meter. QD experiments were carried out in a dilution refrigerator at 100mK. Simulations were carried out by Sentaurus TCAD from Synopsys Inc. Metal gate work functions and gate oxide dielectric constants were calibrated on experimental CV measurements. Density correction based on a quantum correction model was employed with the values calibrated in [11].

III. Qubit Process-Split Pre-Screening

Carrier mobility is an important indicator for high-quality materials and therefore qubits. Using split C-V we screen the six potential process splits by studying the behavior of 22FDX® MOSFETs with lowering temperatures and back bias. Figure 1 plots the effective carrier mobility, μ_{eff} as a function of temperature at zero body bias (ZBB, $V_{BG} = 0$). As expected, the mobility of each device increases with decreasing temperature. However, some differences between PMOS and NMOS emerge. If we first compare gate stacks, this has a negligible effect on NMOS, while in PMOS the first gate stack (GS-1), consistently shows ~50% lower mobility than GS-2. If instead we compare the effects of equivalent oxide thickness, NMOS proves itself to be more sensitive. While PMOS EOT-2 does benefit from slight improvements in mobility (ex. – 334 vs. 401 cm^2/Vs maximum at 4.2K), NMOS mobilities for EOT-2 are significantly larger than EOT-1 at every temperature, increasing from 1.7x to 3.6x greater at 300K and 4.2K respectively. This is in line with published results showing that mobility reduces with decreasing EOT for high-*k* gate oxides due to increased optical phonon scattering, whereas the quality of the high-*k* gate oxide determines the amount of remote charge scattering [12].

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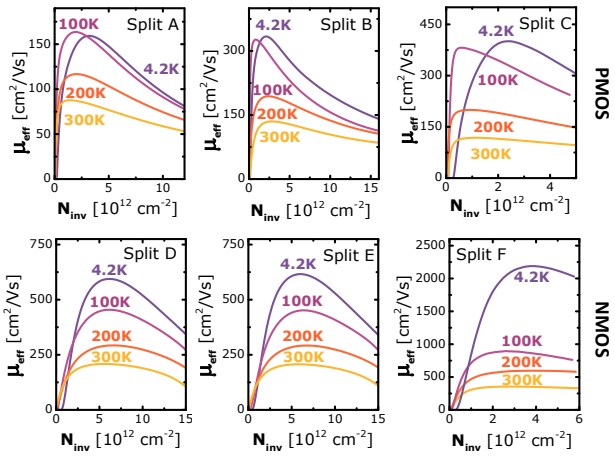

Fig. 1. Effective carrier mobility (μ_{eff}) *vs.* the inversion charge density (N_{inv}) as a function of temperature for both front gate stacks and equivalent oxide thicknesses when V_{BG} = 0V (ZBB).

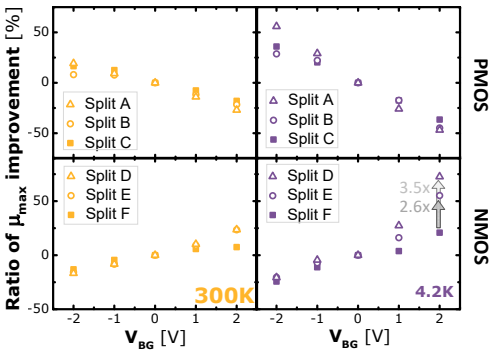

Fig. 2. Ratio of maximum effective mobility (μ_{max}) improvement w.r.t. V_{BG} = 0 *vs.* the back gate voltage (V_{BG}) at (left) 300K and at (right) 4.2K for the six process splits: GS-1 (triangle) and GS-2 (circle, square), EOT-1 (open markers) and EOT-2 (closed markers).

Irrespective of temperature, the back gate has a significant impact on the maximum μ_{eff} (μ_{max}). In Fig. 2 we plot the relative change in μ_{max} with applied back bias of ±1, ±2V as compared to ZBB and look at how this difference is modified with temperature. To consistently compare NMOS and PMOS, we refer to these values as forward body biasing (FBB) and reverse body biasing (RBB), as the back bias polarity is inverted for the two channel types. In all cases, FBB (RBB) improves (decreases) the μ_{max} but the FBB effect is notably strong at 4.2K for Splits D and E (EOT-1.) To take a closer look at the back-bias dependence at 4.2K, we plot μ_{eff} *vs.* the effective electric field, E_{eff}, and V_{BG} in Fig. 3. The NMOS EOT-2 reaches a μ_{max} of 2645cm^2/Vs under FBB, at 4.2K. This maximum is on par with comparable FDSOI transistors with thicker gate oxides (EOT = 6nm) and no high-*k* [13]. This is significant because high-*k* materials are a known source of defects which degrade mobility by introducing more scattering centers when compared to SiO_2. Moreover, the mobility for all NMOS under a FBB = 2V displays a change in slope at $E_{eff} \approx$ 0MV/cm to 0.2MV/cm, which is indicative of two-channel conduction and suggests the presence of intersubband scattering (ISS) [14].

To confirm this, we performed TCAD simulations on NMOS EOT-1 and EOT-2. Fig. 4 and 5 show the relative electron density (n_e) as a function of position within the height of the channel ranging from a depth of 0 nm (front gate) to 6 nm (back gate), for both EOTs. In Fig. 4 we show the low temperature (low T) evolution of this density as a function of applied V_{GS}, starting from V_{GT} = 0V and increasing to V_{GT} = 1V while in Fig. 5a, we show the densities calculated at the applied-V_{GS} where μ_{max} occurs in the two devices at 300K and low T. In Fig. 5b we plot the mean

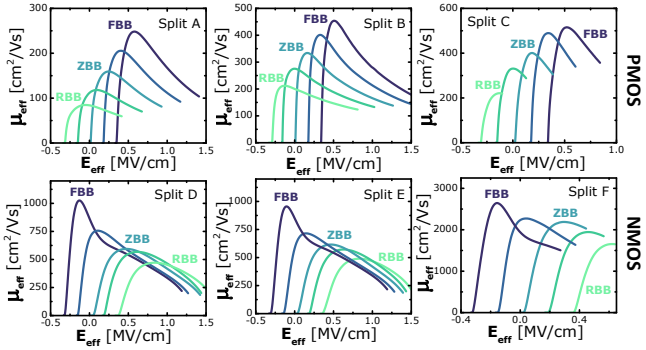

Fig. 3. Effective carrier mobility (μ_{eff}) *vs.* the effective electric field (E_{eff}), as a function of applied back gate voltage (V_{BG}) at intervals of 1V (max = ±2V) for both front gate stacks and equivalent oxide thicknesses at 4.2K.

location of the normalized electron (e^-) density within the channel ($\bar{z}$) at low T as a function of V_{GS}.

From Fig. 5a we see that at ZBB the e^- density is more evenly distributed within the channel for EOT-2; at μ_{max} EOT-2 displays 9% and 5.5% more e^- density than EOT-1 in the bottom half of the channel at 300K and low T, respectively. In agreement with experimental results, this decreases significantly for RBB (V_{BG} = -2V), where 88-95% of the e^- density is centered in the first 3nm of the channel in both device types. In comparison, more than half of the e^- density can be found at the back interface (> 3nm) at μ_{max} for FBB (V_{BG} = 2V) at both temperatures and EOTs. In Fig. 4, we see that EOT-2 maintains a large e^- density at the back interface under FBB and high V_{GT}. In fact, 40% of the e^- density can be found at z > 3nm when V_{GT} = 1. This is in contrast to EOT-1 which only has 16% e^- density at its back interface at V_{GT} = 1. As seen in Fig. 5b, the average e^- position ($\bar{z}$) for EOT-2 does not decrease below 3nm and move towards the front gate conduction channel until V_{GS} > 0.9V (*i.e.* V_{GT} > 0.7V).

To fully understand the implications of these results, we return to the experimental data in Fig. 6 and plot μ_{max} *vs.* temperature on a log-log scale as a function of gate stack and back gate bias (V_{BG}). All devices above 100K display a power law $T^{-\gamma}$, which has been shown to be primarily correlated with the mechanism for phonon scattering (μ_{ph}) within the device [15]. Combining these results with simulation, the differences observed in γ with back bias paint a clear picture. In EOT-1, the gate oxide is thin and the carriers thus experience more Coulomb scattering from the high-*k* above

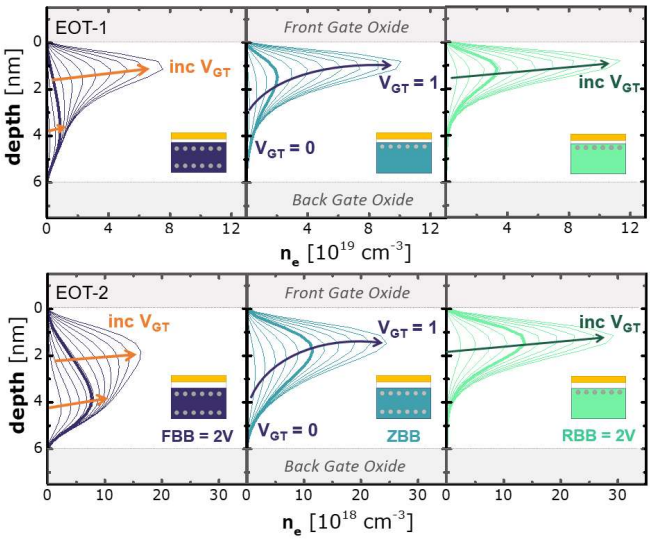

Fig. 4. Low temperature simulation of electron density as a function of depth within the Si channel for NMOS EOT-1 (top) and EOT-2 (bottom) with V_{GT} = V_{GS} – V_{TH} ranging 0V to 1V (intervals of 100mV). V_{GT} corresponding to μ_{max} is shown in bold. Results are plotted for V_{BG} = 0V and ±2V, at 20K.

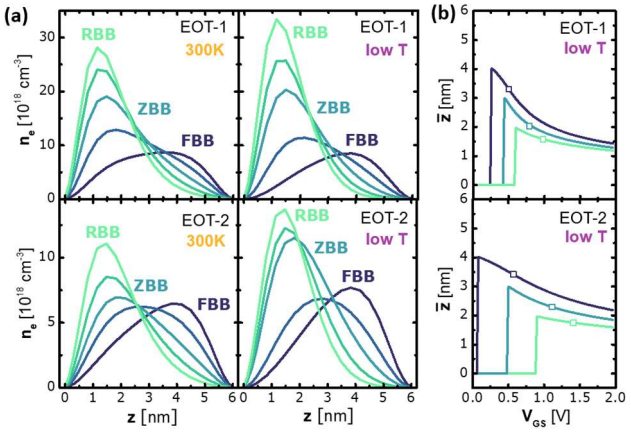

Fig. 5. (a) TCAD simulations of electron density (n_e) vs. Si channel depth (z) at μ_{max} for EOT-1 and EOT-2 at 300K and low temperature prior to any ISS as a function of applied back bias (intervals of 1V). (b) mean location of n_e ($\bar{z}$) as a function of V_{GS} for forward (dark purple), zero (blue) and reverse (light green) body bias (V_{BG} = 0, ±2V). Open square marker corresponds to μ_{max}.

when traveling near the top surface, as occurs with ZBB and RBB. The effect of this scattering is reduced under FBB, as the carriers are pulled down towards the back gate and μ_{max} corresponds to an e^- distribution primarily in the middle of the Si channel, particularly at warmer temperatures, leading to an increase in γ. In this regime, the quality of the BOX interface starts to have a stronger influence. In comparison, the thicker oxide of EOT-2 shifts the baseline conduction pathway of the carriers such that, under both ZBB and FBB, most of the carriers are found in the middle and back half of the channel respectively when μ_{max} occurs, leading to γ~0.9 in EOT-2 under FBB. However, under RBB, while most of the carriers are drawn to the front interface for all V_{GS}, EOT-2 has much less Coulomb scattering, as the oxide used is thick enough to shield the carriers from the high-*k* above it, leading to an observed γ~1 for both carrier types.

Meanwhile, at carrier densities higher than that of μ_{max}, the oscillations observed in electron carrier mobility under FBB along with the strong evidence for two-channel conduction suggest that the electron mobility in both EOT-1 and EOT-2 is degraded by ISS when operated at high inversion densities. The mobility improvements observed under FBB could therefore be limited by the interaction between front and back channels in ultrathin silicon films. This interaction, and subsequent ISS, may be ameliorated in thicker Si films, where the two conduction channels would be better physically separated, and should be considered for future quantum technologies.

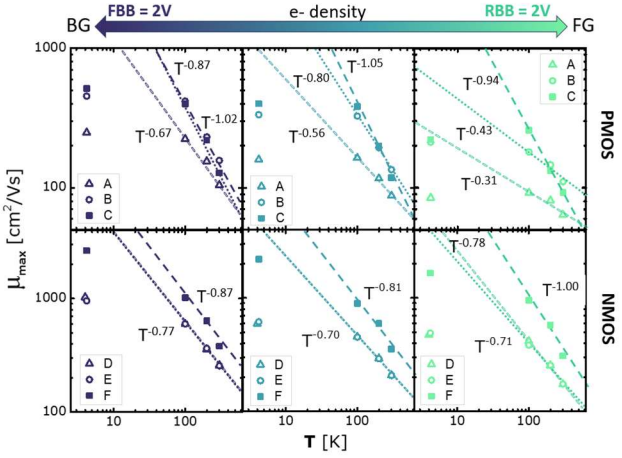

Fig. 6. Maximum effective carrier mobility (μ_{max}) *vs.* temperature on log-log scale for GS-1 (triangle) and GS-2 (circle, square), EOT-1 (open markers) and EOT-2 (closed markers) for three V_{BG} values (0V, ±2V). A power law with temperature is shown for each case.

IV. Split F Qubit Linear and Bilinear Arrays

With the insights from Section III, we selected Split F (NMOS, GS-2, EOT-2) operated under FBB as the best candidate for qubits. Schematics of our qubit devices can be found in Fig. 7. In SR devices (1xN arrays), QDs are coupled along the direction of the Si channel length (y-axis), as shown in Fig. 7c. In FF devices (2xN arrays), the coupling is opened to two dimensions and lateral coupling across the width of the Si channel (x-axis) is now feasible (Fig. 7d). The two-dimensional nature of this coupling makes our arrays compatible with the two most prevalent readout techniques for Si spin qubits today: RF-reflectometry [8] and nearby SET charge detection [15].

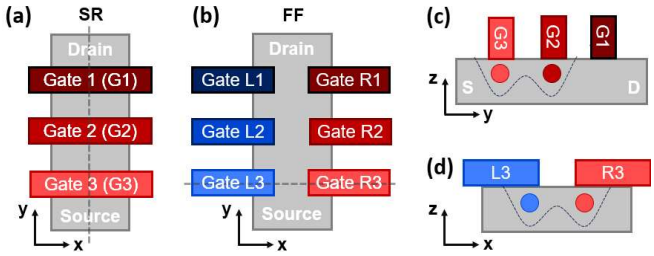

Fig. 7. (a) – (b) Top-down schematic of our qubit designs consisting of (a) three gates in series (SR device) and (b) three face-to-face or split gates (FF device). Gate pitch: 90nm, width: (a) 40nm (b) 70nm. (c) – (d) Cross-section schematic of two adjacent QDs coupled in (c) an SR device, along the y-axis and (d) an FF device, along the x-axis.

A. SR devices: QDs coupled along the y-axis

Operation in the SET regime requires a V_{DS} significantly smaller than the energy separation between subbands. The spaces between gates then act as barriers and promote 3D confinement. We therefore used V_{DS} = 1mV and swept individual gates while operating the remaining front gates in the strong inversion regime. This configuration forms a single QD under the swept gate, while the other gates operate as extensions of the "reservoirs" (*i.e.*, source and drain). Fig. 8a shows the results from one such set of sweeps as a function of G3 at V_{BG} = 2V. The resulting I_{DS}-V_{GS} displays many well-defined Coulomb peaks, with each peak corresponding to the addition of a single electron to the QD. The many equally spaced peaks indicate that a "true QD" has been created within our qubit device and the signal is not due to a dopant or other defect displaying quantum confinement-like behavior.

Next, we repeat this experiment varying V_{DS}, and present the data in Fig. 8b. As expected for a QD SET, a diamond-like pattern is observed, (referred to as Coulomb diamonds), where a given diamond represents a stable N-electron configuration; within a diamond, no additional electrons can tunnel into the QD due to Coulomb blockade. From the heights and widths of the Coulomb diamonds, we can extract two important parameters for the QD: the charging energy, E_C, and the lever arm, α. For G3, we calculate a range of charging energies, with E_C varying between 2.0 and 4.5meV. This range stems from the irregularity of the Coulomb diamond heights and reveals some variability in the size of the QD. The source of this variability is likely due to a localized defect which is exerting unwanted electrostatic force on the QD. The lever arm (α) is a measure of the electrostatic capacitive control the gate exerts on the QD and was found to range from 0.2 and 0.4 eV/V for the many Coulomb diamonds in Fig. 8b, which is on par with other CMOS-based QDs [16].

To couple multiple QDs, we repeat the I_{DS}-V_{GS} under FBB (2V) at very low V_{DS} (1 mV) but as a function of two front gates rather than one (with the other front gate(s) still operated in the strong inversion regime.) In this case, two QDs are formed, one under each swept gate, as shown schematically in Fig. 8c. For two

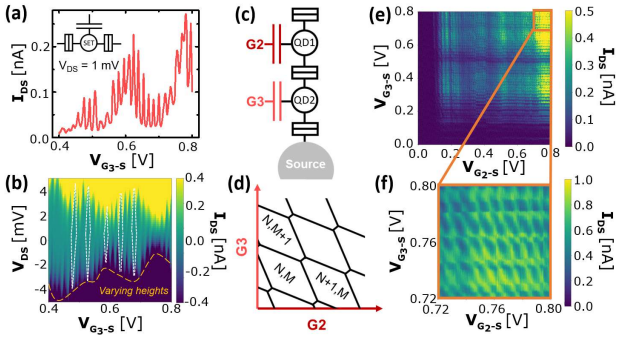

Fig. 8. Process split F 1x3 (SR) qubit device operated under FBB in (a) – (b) the SET regime displaying characteristic (a) Coulomb peaks (b) Coulomb diamonds while sweeping G3. Several Coulomb diamonds are outlined in white to guide the eye. (c) Electronic schematic of two adjacent QDs coupled along the length of the Si channel (y-direction). (d) Theoretical stability diagram with the honeycomb pattern predicted for two coupled QDs. (e) and (f) Stability diagrams of two coupled quantum dots under FBB, located underneath gates G2 and G3, in an SR qubit device.

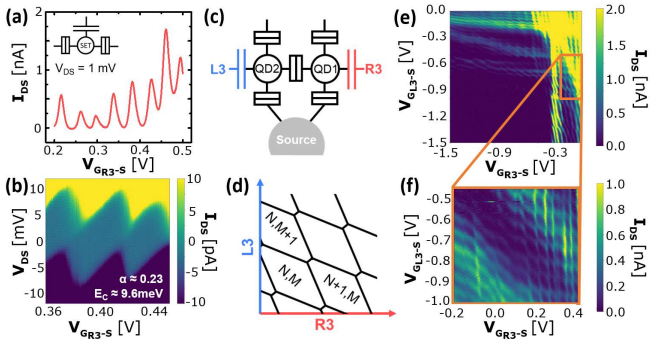

Fig. 9. Process split F 2x3 (FF) qubit device operated under FBB in (a) – (b) the SET regime displaying characteristic (a) Coulomb peaks (b) Coulomb diamonds while sweeping R3. (c) Electronic schematic of two adjacent QDs coupled along the x-direction in an FF qubit device. (d) Theoretical stability diagram with the honeycomb pattern predicted for two laterally coupled QDs. (e) and (f) Stability diagrams of two coupled QDs under FBB, located underneath gates L3 and R3, in an FF qubit device.

quantum dots capacitively and tunnel coupled, the 2D I_{DS}-V_{GS} map of the two swept gates (*i.e.*, the stability diagram) should display a "honeycomb" pattern as depicted in Fig. 8d, which represents the equilibrium charge states of the coupled QDs. An angled slope of the vertical and horizonal lines indicates that the dots are capacitively coupled [17].

In Fig. 8e and 8f we show this stability diagram for our SR qubit device with two QDs formed under gates G2 and G3. In the many-electron regime, we see a clear honeycomb pattern in Fig. 8f, indicating that the two adjacent QDs are indeed capacitively and tunnel coupled. The barrier between the two QDs defines their coupling and is primarily determined by the gate pitch and V_{BG}. A gate spacing of 60nm is therefore large enough to form barriers within 22FDX® and define the quantum wells. To further fine tune this coupling and have individual control over this barrier, a second level of gates could be integrated. Alternatively, as demonstrated in [7], control over the barrier can be reached in linear arrays if the QDs are formed between the gates.

B. FF devices: QDs coupled along the x-axis

Many Si spin qubit devices rely on having a 2xN array-like structure such that one side of the array can be used to sense the other and read-out its state. Moreover, in this type of array, each qubit can have more closest "neighbors" (*i.e.*, more entangled qubits). Therefore, it is also important to be able to couple QDs in the *x*-direction. We use our FF qubit device to probe this functionality in 22FDX®. As in the SR device, we observe many characteristic Coulomb peaks (Fig. 9a) and Coulomb diamonds (Fig. 9b), shown here for the bottom-right gate, R3. From the Coulomb diamonds we extract charging energy of 9.6meV and a lever arm of 0.23 eV/V. The larger E_C measured for the QD under gate R3 in this device implies that this quantum dot is smaller than the one measured in the SR qubit device. This is consistent with the difference in the gate areas between the two device styles, which changes from 1200nm² to 300nm² for SR and FF, respectively. The modification of the QD size with changing gate size is a good confirmation that the QDs that we are measuring are electrostatically defined underneath the front gates as desired.

To couple QDs in a face-to-face configuration, we again repeat the I_{DS}-V_{GS} under FBB with very low V_{DS} but as a function of two parallel front gates. The resulting stability diagrams can be seen in Fig. 9e and 9f, where the quintessential angled honeycomb pattern is again observed, this time for the bottom left and right gates (L3 and R3).

Recent work in 22FDX® has been published on similar qubit layouts with the same reported gate stack as Split E: GS-2 and EOT-1 [6]. Under similar FBB values, the stability diagrams of these devices seem noisier and no clean double QD feature is observed. Comparison with these results further supports the selection of EOT-2 for 22FDX® qubits and suggests that our screening process is indeed working as advertised.

V. Conclusion

Using effective carrier mobility as a figure of merit, we screened six potential processes of reference from GlobalFoundries™ and identified Split F (NMOS, GS-2, EOT-2) and FBB as the best conditions for 22FDX® qubits. Our commercially fabricated qubits formed capacitively- and tunnel-coupled QDs both along the Si channel as well as across it. This is evidenced by the characteristic honeycomb pattern clearly observed in the presented stability diagrams.

Our mobility results show that FBB is highly effective at reducing the scattering associated with the front gate, irrespective of EOT and gate stack materials. TCAD simulations confirm that this is due to the location within the channel that the carriers sit under bias. Moreover, the oxide in EOT-2 is more effective at shielding carriers from high-*k* defects, and with FBB allows one to achieve the same maximum effective mobility as similar devices with a thicker SiO_2 gate oxide. These improvements with FBB however may be limited by intersubband scattering, suggesting that even greater mobility improvements could be seen with FBB of thicker Si channel devices. Overall, this MOSFET screening process represents a viable characterization protocol that can be applied to future qubit nodes.

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