Virtual Twins for Semiconductor Design and Manufacturing Processes

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***Abstract*—In the semiconductor industry, precision in design, and control in manufacturing are among critical points for innovation and yield. Virtual Twins offer a powerful approach by integrating multi-physics, multi-scale modeling and simulations (MODSIM) across key design and manufacturing steps. This article highlights some of Dassault Systèmes solutions' capabilities, including 3D electromagnetic layout simulation to evaluate circuit performance, plasma simulations for etching and deposition to optimize material processing during fabrication, deformation analysis during wafer cleaning, and chemical mechanical planarization simulations to minimize defects and ensure surface uniformity. Powered by the 3D**EXPERIENCE® **platform, these solutions provide an end-to-end virtual environment to reduce variability, improve yield and performance, while uniquely close the design-manufacturing loop by enabling continuous, data-driven feedback and rapid process optimization.**

Keywords—semiconductors, wafer cleaning, etching, deposition, electromagnetic analysis, fluid structure interaction, chemical mechanical planarization, simulations

I. INTRODUCTION

Morteza Mohseni, Emmanuel Leroux: The semiconductor industry is at the heart of technological progress, driving innovations across almost all industries, namely, computing, communications, healthcare, energy, automotive sectors [1-2]. As design complexity increases and device sizes shrink to atomic scales, traditional approaches to process control and optimization face growing limitations. Therefore, challenges in both design and manufacturing have become more pronounced. Indeed, nowadays, maintaining performance, reliability, and high yields while accelerating time-to-market is a growing concern for fabs, equipment suppliers, and design houses.

High complexity of these issues generates strong dependencies between semiconductor design and manufacturing processes. For example, minor variations in plasma etching, deposition conditions, or wafer cleaning steps can significantly affect circuit performance or reliability [3]. Additionally, the transition to heterogeneous integration, 3D architectures, and advanced materials has introduced new sources of variability that are difficult to predict and control using conventional methods.

Virtual (a.k.a digital) twins (VT), the digital replicas of physical systems enriched with real-world data and multi-physics multi-scale simulations, are emerging as a transformative solution to address such challenges [4, 5]. In this context, VTs provide an integrated, simulation-driven environment to understand, predict, and optimize the behavior of materials, devices, and processes across the semiconductor value chain. They enable engineers and scientists to experiment, iterate, and optimize semiconductor technologies in silico, long before physical wafers are processed.

VTs though should rely on a unified data environment to integrate simulation models, manufacturing workflows, and design revisions. This allows them to function as dynamic, cross-domain systems, enabling seamless data exchange between feature scale and process simulation, equipment modeling, and metrology data. This will ensure traceability and consistency across the semiconductor lifecycle leveraging a single and unified environment for data governance, which could be enhanced with artificial intelligence and machine learning [6-8].

Here, we cover a few aspects of semiconductor design and manufacturing process, in which MODSIM technologies are used to improve performance and minimize defects. Taking advantage of the **3D**EXPERIENCE® platform, these solutions provide an end-to-end virtual environment to potentially create a full VT of semiconductors. From validating circuit layouts with 3D electromagnetic field solvers to simulating ion beam etching, and modelling chemical mechanical planarization and stress analysis during wafer cleaning, such VTs enable engineers to make informed decisions before committing to costly physical prototypes. By capturing the underlying physics, electromagnetic, plasma dynamics, mechanics, fluid mechanics, and surface physics, these models offer deep insight into interactions that could govern performance and reliability of semiconductors.

II. 3D SIMULATION OF SEMICONDUCTORS LAYOUT

Longfei Bai: Simulating integrated circuits (ICs) as full 3D geometries is highly challenging due to the large number of transistors or logic gates involved, each requiring ports for full-wave analysis. These ports enable signal transmission through the 3D structure and help characterize its electromagnetic behavior. Thus, a robust and efficient 3D full-wave simulation technique is crucial to handle complex routing and numerous ports in modern ICs.

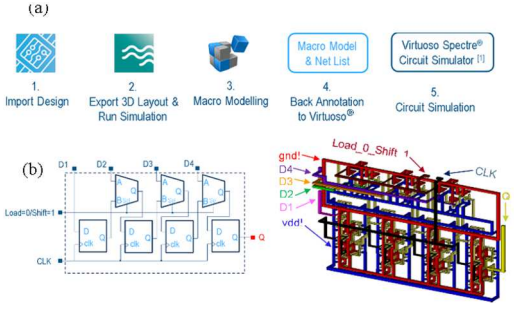

Figure1. (a) IC layout simulation workflow. (b) circuit of a piso shift register and its 3D layout

The proposed workflow is shown in Fig. 1a. The workflow is explained step-by-step using a piso shift register as an example. A piso shift register can be used as a serializer to convert parallel data into serial data in a Serializer/Deserializer (SerDes) channel. Its equivalent circuit is presented in Fig. 1b.

The 2D layout pattern and stackup are first imported into the SIMULIA CST Studio Suite® Chip Interface solution, followed by exporting the model to a 3D environment for full-wave frequency domain (FEM solver based) simulation. In the 3D view, each net is displayed in a unique color, with ports automatically created for every logic gate, such as NAND gates and inverters. Device and pin information is embedded in the port labels. The resulting S-parameters from the simulation are then imported into IdEM® solution, where the generated macro model is verified to be passive and causal—an essential requirement for accurate time-domain circuit simulation. This model is back-annotated into Cadence Virtuoso®, where a symbol is automatically generated using the device and pin information from the port labels, and includes all relevant 3D simulation data as shown in Fig. 2a.

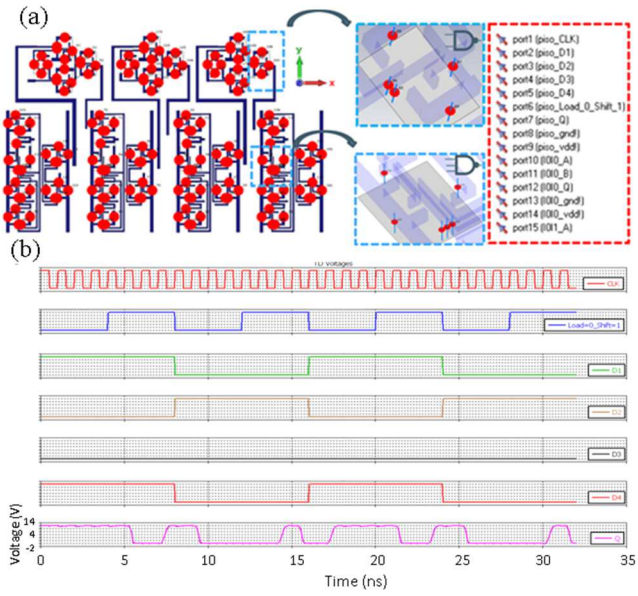

Figure 2. (a) Ports are created for every logic gate. In this example there are 36 logic gates and 191 ports. (b) Timing relationship between input and output

Finally, as displayed in Fig. 2b, circuit simulation is performed in Cadence's Virtuoso Spectre®, with timing results confirming expected behavior: during load time, the shift register holds data with Q equal to D4, and during shift time, it serially outputs data on the rising clock edge.

In summary, seamless workflow for simulating semiconductor layout in 3D is presented. A digital IC example is used but the workflow is also applicable to analog IC and RFIC. The simulations at each step show excellent performance since the entire task takes less than 100 minutes to complete on a workstation with 256 GB DDR4 memory and a CPU @3.4 GHz.

III. PLASMA SIMULATIONS FOR DEPOSITION AND DRY ETCHING PROCESSES

Richard Cousin: Fab equipment vendors have to address many challenges to deliver cost-effective devices optimized for semiconductor mass production. One of these challenges is the design of the so-called plasma reactor currently used for deposition or dry etching. There are different types of dry etching processes that broadly fall into the IBE (Ion Beam Etching) and RIE (Reactive Ion Etching) categories. Thus, to optimize the ion beam responsible for the etching process, it is necessary to control the plasma characteristics such as the plasma density and its homogeneity. The simulation is key to predict the plasma behavior to design an etching machine, especially when no diagnostics are available. This allows estimating the physical parameters, such as the gas pressure and the input power which need to be adjusted in the experimental setup.

Numerical Method: The plasma simulation for the design of semiconductor plasma reactors is performed in 3D with SIMULIA CST Studio Suite® Particle Studio, the charged particle simulation tool of the SIMULIA brand within Dassault Systèmes. The technique is a microscopic approach which uses a time-domain kinetic method with a Poisson based Particle-In-Cell algorithm Fig. 3. First, an electrostatic calculation is performed within the potential applied to push the initial particles. The position and the momentum of each macro-particle is updated at each time step which defines a space charge dynamic. The charge distribution defines an updated solution, superimposed to the external electric field, to compute a new Poisson equation.

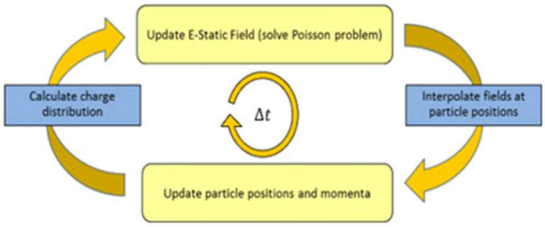

Figure 3. Electrostatic Particle-In-Cell algorithm

Any external magnetic field could also be taken into account as a Lorentz force contribution to the particle movements. In this particular approach, the defined Electrostatic Particle-In-Cell code is not self-consistent. This means that the time step used is a constant, independent of the mesh grid which allows calculating large time scale problems dealing with charged particle species with a different mass ratio such as the interaction between electrons and ions. There is no self-magnetic field generated, therefore no RF-signal emitted. The neutral gas environment is defined by its pressure, temperature and density. The media where the plasma is created is defined by the neutral gas ionization cross-section, excitation and elastic collisions. A statistical model of the Monte-Carlo type is applied according to [9]. The collision cross section depends on the energy of the colliding particles. When considering an electron as an incident particle, it is assumed that this electron is much faster than the neutral atom. Therefore, the neutral velocity and energy contribution is neglected. The energy dependance of the cross-sections is defined by tabulated data for a specific neutral gas and are entered as ascii files.

The Ion Beam Etching (IBE) Process: The numerical method described previously is illustrated in an IBE application demonstrated in Fig. 4a in a full 3D simulation. The device is a cylindrical geometry of 225 mm height and a 95 mm radius. A plasma chamber, characterized by a smaller cylindrical cavity is placed on top of the structure, terminated by two grids at the bottom of the cavity. One grid, connected

to the main cylinder, is grounded to trap the electrons into the plasma chamber to maintain the ionization process. The other grid, the extractor, is defined at a potential of -400V to extract the ions in order to guide them to the substrate to etch. On top of the plasma chamber there is an electron gun to produce electrons to ionize the neutral argon gas under a pressure of 0.2 mTorr. A maximum emitted current of 7.9 mA is extracted out of the electron gun to ionize the argon neutral gas. A static magnetic field, defined by a circular coil is applied to maintain the plasma confined into the plasma chamber.

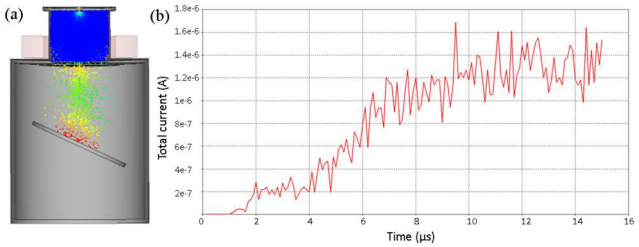

Figure 4. (a) Geometry of the IBE process showing the plasma chamber on top of a larger cylinder containing the material to etch. The picture shows the ions extracted from the plasma chamber and guided to the wafer. (b) maximum ion beam current extracted out of the plasma chamber showing a steady state regime reached after a pulse duration of roughly 10 µs.

The argon ion beam extracted from the plasma is shown on Fig. 4a, A 2D-plane is located at 35 mm from the bottom of the plasma chamber to monitor the maximum ion beam current. An average current of roughly 1.3 µA is extracted, as shown on Fig. 4b. A steady-state regime is reached in approximately 10 µs, validating the time-domain kinetic approach of such analysis.

IV. NUMERICAL FLUID-STRUCTURE INTERACTION WORKFLOW FOR PATTERN COLLAPSE PREDICTION DURING SEMICONDUCTOR FABRICATION

Gabriel Pichon: Isopropyl Alcohol (IPA) is commonly used in microchip fabrication to keep surface clean and remove watermarks after the wet cleaning process. During the IPA drying process, nanoscale silicon patterns can bend and collapse due to capillary forces, a phenomenon known as "stack bending" or "pattern collapse." This issue is critical as chip sizes continue to decrease, making stacks more prone to collapse.

Accurate prediction of this manufacturing use case requires to analyze the IPA distribution-displacement process and its structural impact on the silicon nanostructures. This study presents a numerical fluid-structure interaction workflow using multiphase lattice Boltzmann Method (LBM) [10] for fluids and finite element analysis (FEA) for structures. Unlike previous research that focused only on structural analysis with constant capillary pressure [11], this workflow addresses both transient multiphase fluid flow and its capillary impact on pattern collapse for the first time.

The Numerical Method: The workflow starts with re-constructing 3D CAD from Transmission Electron Microscopy (TEM) images. Two images orthogonal to each other are captured as shown in Fig. 5a-b. Note that the TEM images show etch distortion and edge rounding of the stack. These imperfections are also retained in the reconstructed 3D CAD model as shown in Fig. 5c.

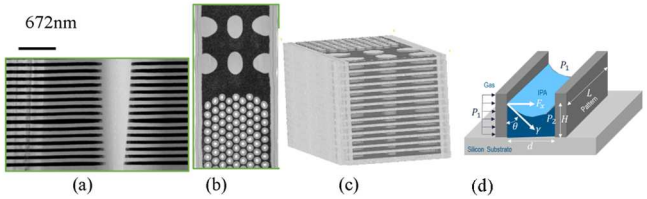

Figure 5. (a-b) Transmission Electron Microscopy Images. (c) 3D reconstructed microchip from these images. (d) Schematic of nanopattern on top of a silicon substrate in presence of IPA and gas phase. Capillary forces acting on the pattern are shown.

In the third step, capillary forces from the Lattice Boltzmann Method (LBM) simulation are calculated. The Laplace pressure and relevant forces are due to the bulk fluid pressure difference between non-wetting (gas) and wetting (IPA) fluid, expressed as:

$$P_1 - P_2 = \Delta P = \frac{2\gamma \cos\theta}{d} \quad (1)$$

$$F_{laplace} = \Delta P L H = \frac{2LH\gamma \cos\theta}{d} \quad (2)$$

where $P_1, P_2, \gamma, \theta, L, H, d$ *and* $F_{laplace}$ represent gas pressure, IPA pressure, surface tension, contact angle, length, height and gap of the pattern and force due to the Laplace pressure, respectively. The transient Laplace pressure in eq. (1) is obtained from the LBM simulation at different time steps and provided as 3d pressure boundary condition input for the FEA analysis.

In the fourth step, an implicit dynamic FEA simulation is performed where the bottom part of the micro-chip is kept fixed to the silicon substrate while applying transient pressure load from the LBM simulation.

Results from the LBM and FEA simulations in Fig. 6 show the 3D IPA/gas distribution, the deformation, and stress fields. The deformation is strongly influenced by fluid distribution: stacks exposed to IPA on one side and air on the other side show significant deformation due to capillary forces, whereas stacks surrounded by IPA show little to no deformation. This contrasts with workflows using only FEA analysis. Fig. 7 demonstrates this by applying uniform capillary pressure without using multiphase fluid simulations, resulting in an overestimated deformation across all stack layers, unlike the more selective deformation seen in Fig 6. Also, note that a transient history of 3D fluid distribution enables to have a transient deformation and stress field history.

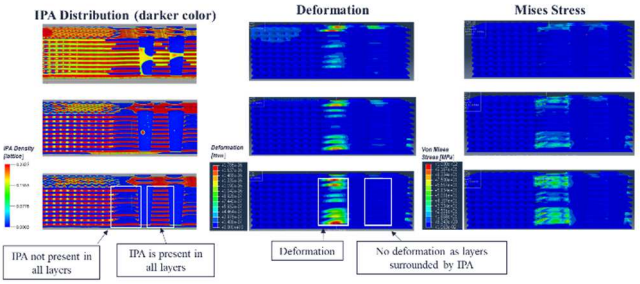

Figure 6: 3D IPA distribution and corresponding deformation and mises stress.

The workflow results demonstrated above can be leveraged to check for multiple gas injection location, rotation speed during cleaning, alternatives of rinsing liquids

which in turn can improve success rate in semiconductor fabrication process.

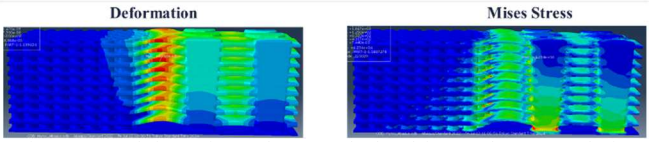

Figure 7. 3D deformation and stress calculated from only FEA analysis.

V. CHEMICAL MECHANICAL PLANARIZATION

Romil Tanov: Chemical-mechanical planarization (CMP) is a process in semiconductor manufacturing that uses a combination of chemical and mechanical forces to create a smooth, flat surface on silicon wafers [12]. The basis for modeling CMP in SIMULIA Abaqus® is the Contact Wear modeling capability within the Abaqus® contact interaction scheme in Abaqus®/Standard and Abaqus®/Explicit.

Wear is a microscale phenomenon triggered by mechanical contact resulting in cumulative loss of surface material. In Abaqus® surface wear modeling is implemented within the contact interaction modeling scheme. Material wear is handled by treating accumulated wear distances as nodal offsets for contact penetration calculations without affecting underlying element calculations. This approach uses Archard's wear model, which relates the wear distance rate on individual contact surfaces to contact pressure and slip rates:

$$\dot{W} \approx \phi_{wear} \cdot \mu_{fric} \cdot \sigma_{p.|\dot{\gamma}|} \qquad (3)$$

in which, ϕ_{wear} is the wear coefficient; μ_{fric} is the friction coefficient; σ_p- is the contact pressure; and $|\dot{\gamma}|$ is contact slip rate, respectively.

Contact wear accounts for local surface wear distances in contact penetration calculations but not in underlying element calculations. It can be used together with ALE adaptive meshing in Abaqus®/Explicit to modify the mesh based on the accumulated wear distance from the contact wear. Furthermore, it can be implemented together with step cycling in Abaqus®/Standard to efficiently predict accumulated wear from a large number of wear cycles. Moreover, it is possible to simulate wear accumulation in steady-state transport analyses.

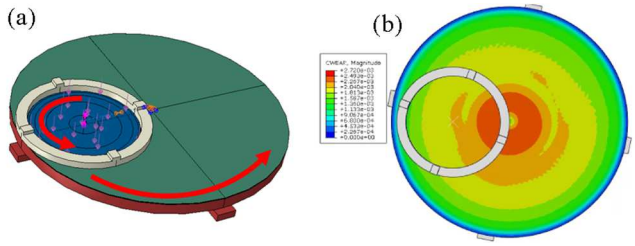

Figure 8. (a) Simplified example of the CMP Abaqus® model. (b) Abaqus® CMP models accumulated wear results.

VI. CONCLUSIONS

Leveraging the multi-scale, multi-physics modeling and simulation technologies of Dassault Systèmes, we developed several innovative use cases to verify and analyze semiconductors throughout the design and manufacturing processes. We introduced 3D electromagnetic solvers to evaluate the performance of a phase shift register layout, demonstrating that robust, efficient 3D full-wave simulations can provide valuable insights into the electromagnetic behavior of semiconductors. Additionally, we presented novel workflows using advanced physics solvers to i) predict physical dynamics in plasma reactors, ii) assess Fluid-Structure Interaction (FSI) for pattern collapse during wafer cleaning, and, iii) simulate Chemical-Mechanical Planarization processes. By integrating such simulation technologies and Design of Experiments (DoE) solutions with real-world manufacturing data into the 3DEXPERIENCE® platform, we move closer to enabling an end-to-end Virtual + Real (V+R) environment that connects the entire semiconductor value chain from design to manufacturing.

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