Wafer Edge and Backside Profile Integration with 3-D Process Emulation

2024 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD) | 979-8-3315-1635-2/24/$31.00 ©2024 IEEE | DOI: 10.1109/SISPAD62626.2024.10733209

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***Abstract*—Attention has been drawn on wafer front surface's patterning area while developing next-generation semiconductor products. Unfortunately, to enhance device performance, the number of process steps and integration schemes are diversified inducing complex patterns over whole surfaces including wafer edge and back-side (WEB) in final. Thus, focusing on those regions is required beyond the front, as defects and process risks are increased on the regions. So far, post-processes are executed to reduce defects after their occurrence at the edges and back-side, but it is important to understand defect generation mechanism to suppress them effectively. In this paper, we utilized 3-D process emulation on WEB profile integration to estimate defect risk in early stage of product development before defect occurs. In final, WEB profile has been integrated and consistent with real-wafer's cross-section microscopy images with typical defect sources.**

Keywords—3-D, Process, Emulation, Wafer, Edge, Back-side, Bevel, Defect.

I. INTRODUCTION

Recently, importance of process control in wafer edge and back-side (WEB) regions has been continuously increased for fast development and yield improvement on next-generation devices. In particular, with the recent advancement of wafer bonding technology, the importance of process control in the WEB domain is increasing even more [1]. However, risk analysis and its hedge in the regions usually rely on experience-based approaches from previous generations. The reason is that there are limitations on inspection technology for those area, compared to the front-side, and it is difficult to detect in-fab defects and discover risk before front-side attack by defects from WEB [2].

To overcome the limitations, we introduced 3-D process-emulation which is widely used for device characterization and process integration due to its fast calculation algorithm. On the emulator, we developed novel process models covering WEB regions of unique features as its shape and dimension up to micrometer, such as bevel. Each models were verified as actual unit processes. This has an advantage of being able to create and utilize back-end profiles, especially when wafer supplies are concentrated in the front-end process at early stage of device development period.

Moreover, preemptive risk identification has been done on WEB induced by cumulative process. Defects can be prevented even in the early phase of product development under extremely frequent changes from scheme design to unit processes. It can be also used for the profile variation of the middle of back-side and along edge lines in the same way. Through this methodology, it is expected not only to make resources which are invested in the development of WEB area more efficient but also to contribute to the timely development of device.

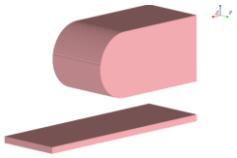

Fig. 1. Initial structure of wafer edge and back-side for 3-D process emulation.

II. Unit Process Models

In-house topography simulator, developed for modeling wide range of 3-D structures based on unit process models, was utilized [3]. Since conventional topography models are focusing on front-side processes as experiments, WEB-specified models were newly developed for accurate structure generation. Since it has both simulation and emulation algorithm, we can choose a proper model depending on trade-offs between real process similarity and calculation cost. In this work, emulation models were mainly used to calculate millimeter scale structure in fast (Fig. 1).

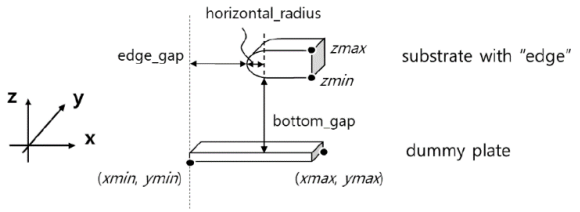

Fig. 2. Definition of initial WEB structure.

To define initial structure with high degree-of-freedom, essential parameters were defined (Fig. 2). First, x_{min}, x_{max}, y_{min}, y_{max}, z_{min}, z_{max} were defined for overall dimension of wafer's length, width, and thickness. Also, *horizontal_radius* was also defined to determine bevel's convexity, which is about 0.25 mm at actual wafers. Additionally, *bottom_gap* and *edge_gap* were defined to control WEB structure's 3-D offset inside the domain. Throughout optimization of the parameters, computational structure can be set up similar to real wafer's cross-section observed in scanning electron microscope (SEM) images.

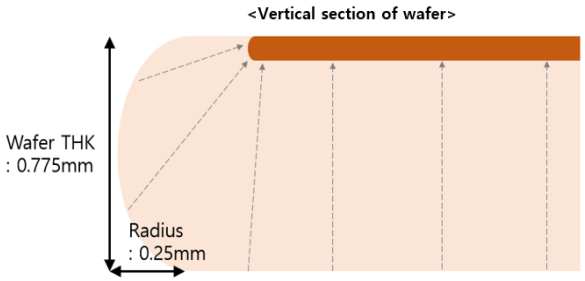

Fig. 3. Structure scaling method for calculation cost reduction.

Also, scaling method was used for efficient calculation to achieve both reality and high resolution in nanometer. When we define parameters as actual wafer, it is hard to use nanometer resolution under typical high-power-computing (HPC) servers due to memory overflow issues. Thus, we scaled initial structure by 1/100 of the actual size to reduce calculation cost (Fig. 3).

We defined unit process models for WEB region. Based on 8 major process category, 14 unit process models were established and implemented into our simulator (Fig. 4). Most of the models are linear with process parameters such as process time. For example, 'Diffusion-General' category model which assumes general boat type chamber, the deposition thickness over whole structure is directly proportional to deposition time of equipment recipe. Also, there are non-linear processes which generates non-conformal results by position due to its original mechanism. For example, edge bead removal (EBR) and plasma etch strip (PES) process use source materials and make them react locally. The models were developed and verified with experimental results as below.

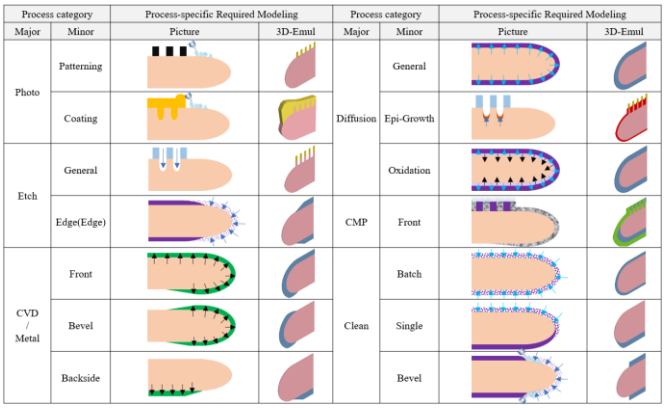

Fig. 4. Unit process models based on major process category.

A. Edge Bead Removal (subprocess of Photo-Coating)

After SOH coating, edge bead removal (EBR) process is performed to remove unnecessary region by shooting liquid etchant along the edge while the wafer spins. After EBR, hump is generated on the edge line where SOH and etchant are in contact, which results non-linear shape such as width and height of the hump. We prepared a sample of SOH coating process having hump on 0.7 mm from the edge, which was a target location of EBR process. With cross-section analysis, it was identified that hump was formed with 5 μm tails for inward and outward from the peak height location (Fig. 5). We also found that the maximum height of the hump (377 nm) was about 6 times thicker than front-side's target thickness (68 nm) and reproduced the whole profile by the emulation (Fig. 6).

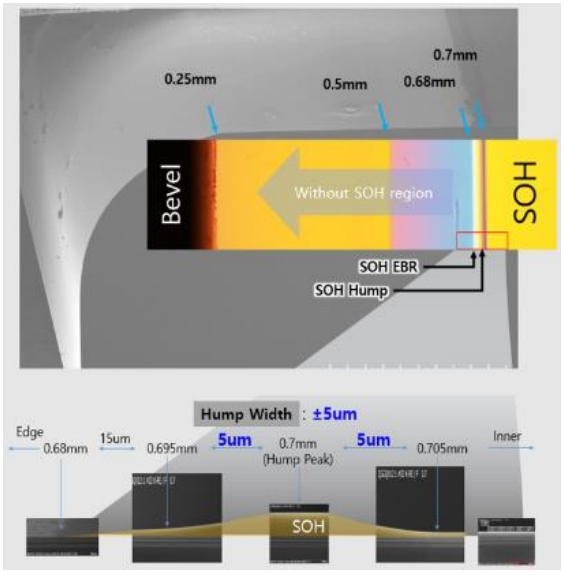

Fig. 5. Cross-section SEM image of SOH coating sample's near edge line.

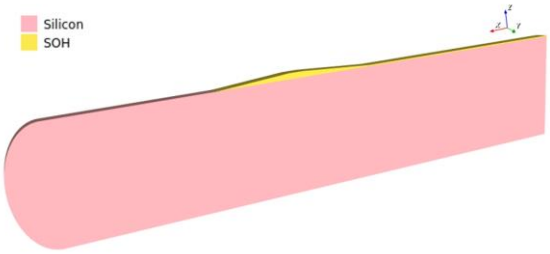

Fig. 6. Emulation result of coating process calibrated on cross-section image.

B. *Plasma Edge Strip (subprocess of Etch-Edge)*

Similarly, after ACL deposition, plasma etching is executed to remove unnecessary region by screening front and back side and exposing edge region only. However, the plasma can penetrate into the gap between wafer and screens which results ACL's unwanted etching profile toward wafer center. In final, incline, also a non-linear result, is generated starting from screen edge. We also prepared a sample of ACL's PES process. With cross-section analysis, ACL was completely removed from wafer edge to 0.75 mm distance and slope was found from 0.8 to 1.5 mm (Fig. 7). Based on the result, we generated PES profile by the emulation (Fig. 8).

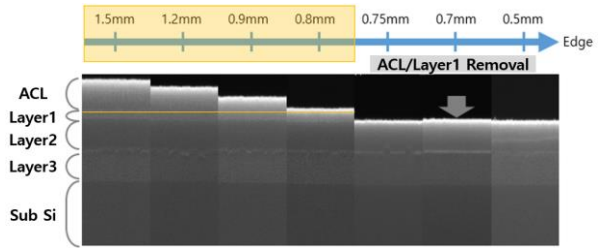

Fig. 7. Cross-section SEM image of ACL layer remaining profile after PES.

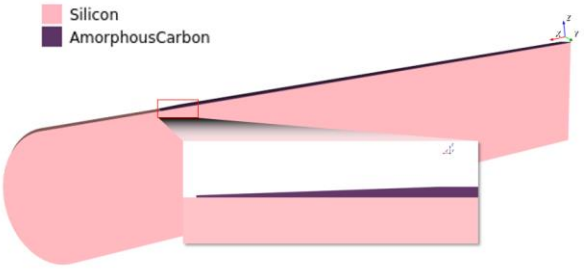

Fig. 8. Emulation result of PES process calibrated on cross-section image.

III. Integration Process and Discussions

After unit process verification, we expanded our work to complicated structures from real integration process. Two representative steps were investigated focusing on wafer front edge (flat region) and bevel (convex region), respectively.

A. *Wafer Front Edge*

The first example is coating process followed by etching and deposition post-processes. As we discussed in the previous section, hump was generated on flattened SiN layer, right next to EBR line expected to be in ring shape along wafer edge. Cross-section image was analyzed as what we expected while wiggling exists due to variation of liquid etchant shooting and interaction with SOH in reality (Fig. 9). After that, front-side SOH etch process and oxide deposition processes was executed sequentially to generate integrated structure. Among them, it was found that the height of hump decreased faster than the width of it during SOH etch process which left stand-alone hump in final. The emulation result was highly similar to cross-section SEM images (Fig. 10).

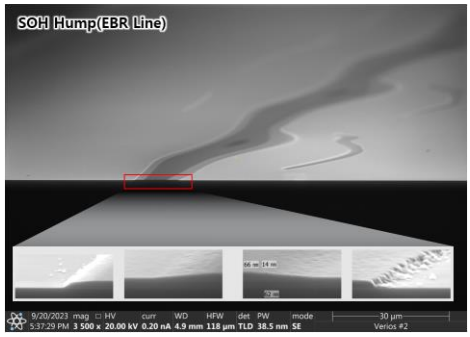

Fig. 9. SOH hump on actual wafer of arbitrary process

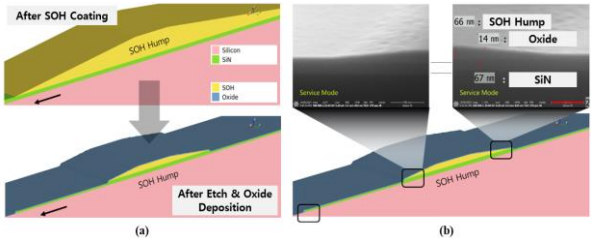

Fig. 10. (a) Change of SOH bump profile after etch and deposition process on emulator (b) Comparison of actual wafer profile and emulator on edge.

B. *Bevel*

The second example is integrating tens of process steps. The upper part of bevel region is highly affected by front-side etch processes because of accumulated residual layers after them. Also, in clean processes, the front/back-side can be selectively etched by controlling chemical discharge direction which induces bevel region's stacked shape more complicated. Compared to experimental cross-section images, it was well integrated even though the structure was composed of multiple layers throughout multiple processes (Fig. 11).

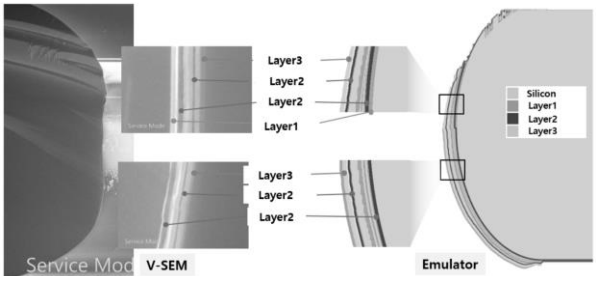

Fig. 11. Cross-section comparison of emulation and SEM image of bevel area.

To be more specific, it is possible to compare the bevel's front and back-side with layer1 material's presence which was formed at the beginning of whole integration process. Right after the layer1's deposition, back-side layer1 strip was performed (Clean-Single), and there is no layer1 film left in the back-side bevel region. Also, it is confirmed that layer1, layer2, and layer3 were also formed quite similarly.

In final, a process risk was found with unexpected structure as a defect source with the high-accuracy integration results. On top of bevel region in the emulated structure, sharp-cornered silicon pillars were observed, which is a one of representative cases to be controlled in defect engineering, called "cone defect" [4]. The defect arises when high amount silicon etching processes are involved in the integration process because they induce patterns on wafer edges, like inner region of the wafer. They are highly possible to be broken by lots of mechanical stress sources and become particles attacking main patterns of wafer front-side. It was easily found in other samples under similar mechanism, although Fig. 11 does not show due to the low resolution (Fig. 12). Moreover, those structures alive through multiple processes if they are passivated due to edge line variation of photoresist determined by EBR process, which makes itself more hazardous to following steps. Since we can control the line's position and shape via emulation parameters, it is possible to advance our work toward optimization of the parameters to reduce various kinds of defects on process scheme designing.

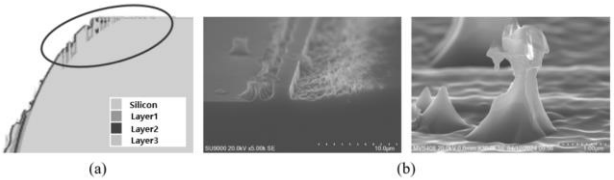

Fig. 12. Wafer bevel area cumulative stack comparison.(a) Emulator (b) Actual wafer.

We constructed a prototype of emulation-based defect analysis workflow in high accuracy, while it needs more improvements. For example, the upper part of bevel is slightly different from the actual one due to imperfection of selectivity. In reality, most of processes have selectivity for each material, but it was not completely reflected to this work. Also, there are internal sequences for a single recipe which was not completely implemented on the emulator. However, as calibration work accumulates, the consistency with real processes will continue to rise.

IV. Conclusion

Our study developed and utilized 3-D process emulation models for predicting risks on WEB area, unlikely to conventional product researches and developments methods focused only on the front-sides. In order to simulate the actual semiconductor processes, 14 models were developed and organized for 8 major semiconductor process except ion implantation, and consequently, we made the foundation for step by step processes. Along the way, we found that there are some non-linear factors in the models, such as SOH hump and ACL slope from EBR and PES processes, respectively. Those models were fitted consistently based on destructive testing/analysis of actual wafers. In final, a process risk has been found with unexpected patterns on edge as a possible defect sources.

Still, there are several cases of inconsistency which results from the difference of etch selectivity used in the process of wet/dry etch recipe with theory, so these kinds of issues need to be investigated. We expect to create a more consistent model by securing more experimental data and accurate selectivity. When we implement the process flow by utilizing the model, it can be considered as a great tool that can analyze risks quickly before execution of wafer processes and suggest modification points for the process schemes. Therefore, we expect improvements such as reducing defects on wafers from the early stage of device development which can be helpful toward mass-production phase.

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