2024 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD) | 979-8-3315-1635-2/24/$31.00 ©2024 IEEE | DOI: 10.1109/SISPAD62626.2024.10733046

STEM Image Based Structure Generation for Advanced CMOS Devices

Felix Widauer, Xaver Klemenschits *, Cedrik Balla, Gerhard Rzepa,
Jose Maria Gonzalez-Medina, Bonny Dongre, Georg Strof, Zlatan Stanojevic, Markus Karner
Global TCAD Solutions GmbH, Vienna, Austria
* Corresponding Author: x.klemenschits@globaltcad.com

***Abstract*—Process technology computer aided design (TCAD) has become an indispensable tool to characterize proposed future technologies. However, current solutions often require tedious manual calibrations of process flows. Here, we present the automatic processing of electron microscopy (EM) images to 2D and 3D device representations. Parts of the device which are not present in the EM image are emulated to create a structure ready for device simulation. The feasibility of this approach is shown by extracting the fin shape from the EM image of a 7nm FinFET, as well as studying the impact of fin shape on device characteristics in an exemplary variability study. Additionally, the inner spacers and gate shape of a nanosheet (NS) FET are reproduced, showcasing the applicability of the presented approach to different device technologies.**

***Index Terms*—EM, TEM, STEM, FinFET, Nanosheet, TCAD, Image Recognition**

I. Introduction

Continued scaling and optimization of semiconductor devices requires detailed insight into processing and device performance. Typical modeling via manual extraction from electron microscopy (EM) images or process emulation strategies to mimic the shapes visible in the EM images are both time consuming and prone to inaccuracies. The proposed STEM image recognition library (STIR) aims to automate the systematic extraction of device structures from EM images, thereby grounding the device simulation in real measurement data, as opposed to purely emulated device structures. The targeted speed and efficiency gains enable more economical modeling of real structures and thereby large scale studies which are currently only feasible with large amounts of manual effort.

II. Methods

STIR, as part of the ProEmu [1] software, is a computer vision library based on OpenCV [2] and is used to identify material interfaces in EM images. Several image processing techniques, such as bilateral filtering [3], adaptive thresholding [4], morphological operations [5], and connected component labeling [6], are used to identify the boundaries of all materials according to multiple criteria. EM images often exhibit low resolution, low contrast, and high degrees of noise. Identifying the two-dimensional (2D) material surfaces is therefore dependent on the ability to robustly distinguish among materials. This is achieved by performing the following steps for each material visible in the EM image, thus allowing these image processing algorithms to be fine-tuned for any given material with a set of specific input parameters. The order of application of the image processing steps to reach conformal material descriptions is shown in Fig. 1.

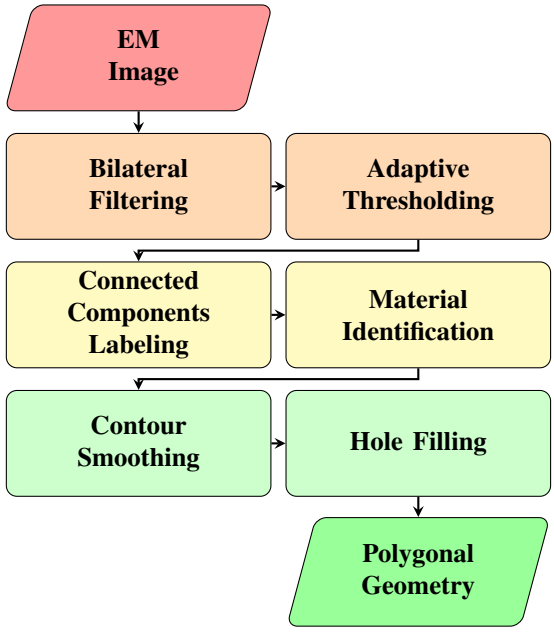

Fig. 1: STIR: From EM Image to Polygonal Geometry

First, bilateral filtering is applied to the input image to reduce noise while preserving contrast between the materials. Next, an adaptive threshold is used to separate each material from the background, thus creating a binary image for each of the materials. The subsequent operation require each material, which is represented by an area of the foreground in the binary image, to have no connection to any other region of the foreground. This is achieved by first applying morphological operations to the binary image.

Now the individual regions within the binary image are detected using connected component labeling. One or multiple regions are assigned to a given material based on its expected position in the image, its average gray scale value and its expected area. It is also possible to define materials as one or a union of multiple remaining areas, which are located at specific points in the EM image. This is particularly relevant for layered structures and materials which are fully enclosed

within another. This flexible approach to material identification allows for straight forward adaptation to new device technologies while retaining robustness due to redundant assignment conditions.

The obtained material candidates may exhibit holes and imperfections along the contour which do not correspond to the material shape visible in the EM image. These imperfections arise due to noise in the EM image which can not be suppressed sufficiently by the pre-processing steps. A custom hole filling algorithm based on connected components labeling and morphological operations is applied to remove these imperfections.

After all materials have been detected and placed in the simulation, parts of the device which were not present in the EM image are generated to form a full structure. Thereby, a fully automated tool chain from EM image to electrical device characterization is formed. To investigate the viability of STIR for advanced node technologies, a FinFET of the $7\,\mathrm{nm}$ node and a nanosheet (NS) FET proposed for the $3\,\mathrm{nm}$ node were characterized using this approach.

A. 7 nm FinFET

The robustness of the STIR library is shown by detecting the materials perpendicular to the channel of a $7\,\mathrm{nm}$ FinFET [7]. First, the oxide is found, as it is expected to be identified most robustly due to the well-defined boundary with neighboring materials. Substrate has to be the region directly below oxide and can be identified redundantly by position and gray scale value. Next, the interface between the high-k dielectric and the gate metal is found. The high-k dielectric is then defined as the area above oxide and below this interface. The area above the interface and in this case up to the edge of the EM image is identified as gate metal. The material is confirmed with a gray scale value comparison. The input parameters used for the detection of materials via their gray scale value are listed in Tables I to III. The presented method implements one of various possible approaches to recreate the full FinFET cross-section with the STIR library.

Parameter	Value
Bilateral Filter Diameter	7
Bilateral Filter Sigma Color	30
Bilateral Filter Sigma Space	30
Adaptive Threshold Block Size	15
Adaptive Threshold Constant	2

TABLE I: Input Parameters for the oxide of FinFETs

Parameter	Value
Bilateral Filter Diameter	15
Bilateral Filter Sigma Color	50
Bilateral Filter Sigma Space	50
Adaptive Threshold Block Size	21
Adaptive Threshold Constant	3

TABLE II: Input Parameters for the substrate of FinFETs

Parameter	Value
Bilateral Filter Diameter	15
Bilateral Filter Sigma Color	120
Bilateral Filter Sigma Space	120
Adaptive Threshold Block Size	31
Adaptive Threshold Constant	3

TABLE III: Input Parameters for the gate metal of FinFETs

If the EM image is comprised of differently arranged or a different number of materials this process can be customized accordingly, aided by the modular design of STIR. Passing the resulting structure on to device simulation, we show the seamless integration of detected EM materials into a full technology computer aided design (TCAD) flow.

B. FinFET Variability Study

In order to demonstrate the impact of accurate geometry extraction possible with the presented method, fin shapes of a series of EM images were extracted showing the effect of fin bowing [8] on final device performance. A series of 11 EM images was generated with an increasing degree of fin bowing and processed with the same order of operations as described in section II-A. The resulting polygonal geometries were used to emulate full FinFET structures in order to study the variation of electrical properties. Since this variability study was also based on $7\,\mathrm{nm}$ FinFET technology, the same recognition parameters as for the FinFET described in the previous section were used.

C. Stacked Nanosheet

One of the major challenges of NS FET processing remains the inner spacer generation [9]. Accurate modeling of these shapes is therefore necessary to guarantee device viability. Using STIR, it was straight-forward to detect the exact shape of the inner spacers and the gate of an NS FET with three stacked NSs [11]. To achieve this, the six inner spacers were identified according to their gray scale value and their approximate area in the EM image. The gate metal was found via gray scale value comparison. Simulating the transfer characteristics of the device confirmed its proper function with the detected spacer and gate shapes. The input parameters used for the detection of materials via their gray scale value are listed in Tables IV and V.

Parameter	Value
Bilateral Filter Diameter	7
Bilateral Filter Sigma Color	100
Bilateral Filter Sigma Space	100
Adaptive Threshold Block Size	15
Adaptive Threshold Constant	2

TABLE IV: Input Parameters for the inner spacers of NS

Parameter	Value
Bilateral Filter Diameter	9
Bilateral Filter Sigma Color	100
Bilateral Filter Sigma Space	100
Adaptive Threshold Block Size	1001
Adaptive Threshold Constant	-70

TABLE V: Input Parameters for the gate metal of NS

III. Results

A. 7 nm FinFET

As shown in Fig. 2, the extraction results in an accurate representation of the reference EM image. On the left, the extracted polygons have been superimposed onto the original EM image in the corresponding colors. The device on the right was completed by adding missing parts in the EM image through process emulation. Due to the high resolution used in the emulation, extraction artifacts due to the low resolution in the EM image are visible on the final device. This can be mitigated by applying additional smoothing to the detected curves during image recognition or process emulation.

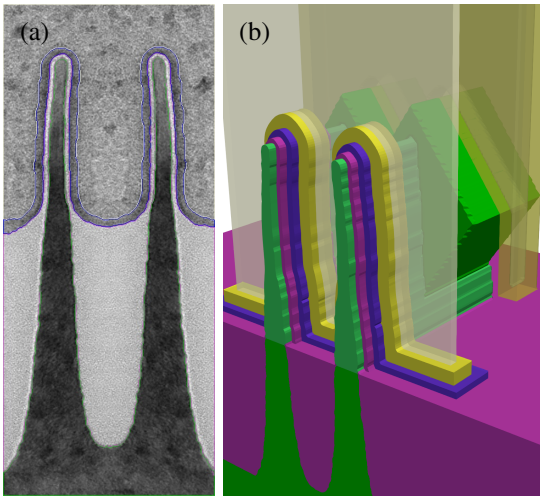

Fig. 2: (a) EM image [7] of a 7 nm FinFET and (b) the extracted geometry used for device simulation

The device simulation yielded transfer characteristics within the expected range [10] for the given technology node as seen in Fig. 3.

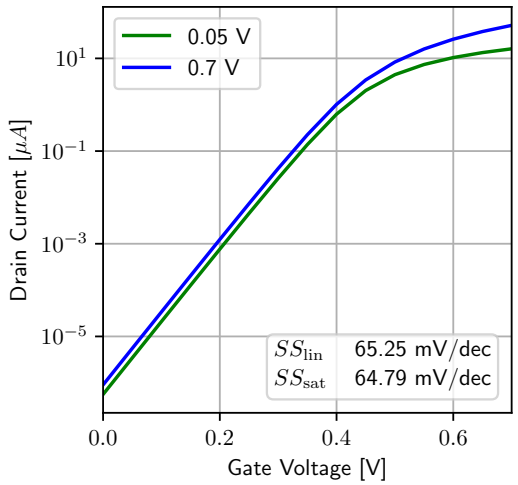

Fig. 3: Transfer characteristics of the extracted 7 nm FinFET

B. Variability Study

Due to the robustness of the proposed library, it is straightforward to detect a series of images automatically and compare the resulting devices, as shown in Fig. 4. The original EM images for the variability study, shown on the left with the extraction superimposed, have a resolution of 856 x 1612. Hence, artifacts around the contour are less visible in the completed device on the right compared to the 7 nm FinFET, but could still benefit from further smoothing.

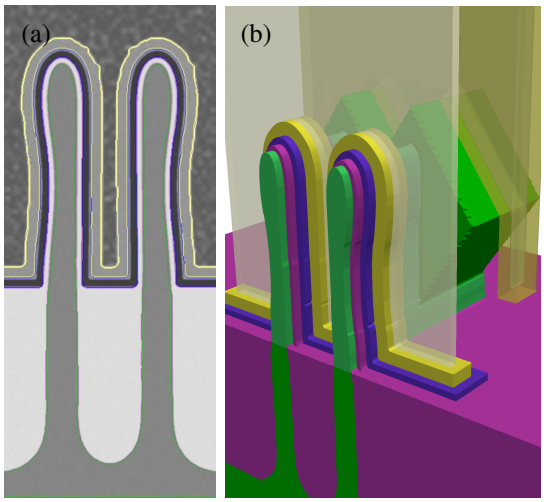

Fig. 4: (a) EM image showing 1 nm of fin bowing and (b) extracted geometry used for device simulation

Device simulations showed a correlation between fin bowing and a shift in threshold voltage as well as subthreshold swing over the tested fin bowing range of 0 nm to 2 nm, as seen in Fig. 5.

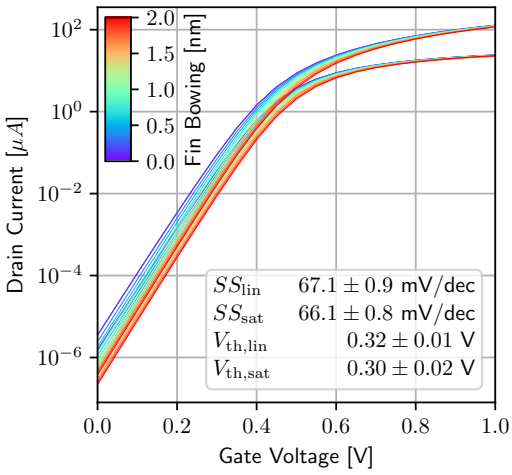

Fig. 5: Variations in the transfer characteristics of the extracted transistors with varying fin bowing

C. Stacked Nanosheet

As shown in Figs. 6 and 7, the inner spacers and gate shapes could be reproduced accurately to match the EM profile. The versatility and applicability of STIR to different orientations and architectures is highlighted by extracting the inner spacer shapes of a stacked NS geometry. The resulting analysis of device properties is presented in Fig. 8.

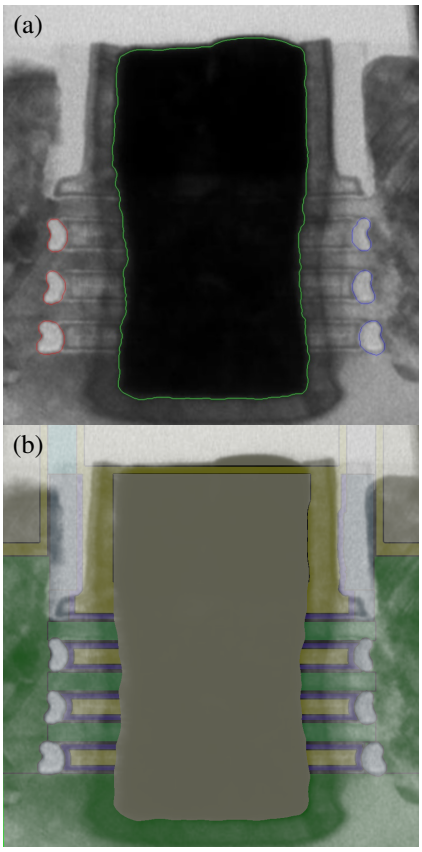

Fig. 6: (a) Nanosheet [11] slice along the channel and (b) EM image superimposed on the emulated structure

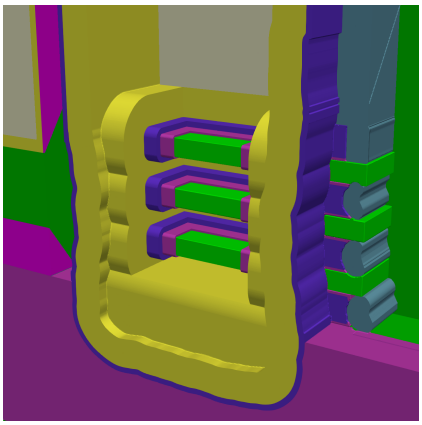

Fig. 7: 3D rendering of the final stacked NS device

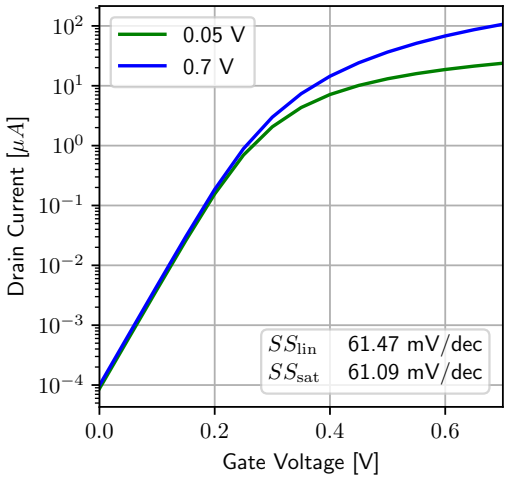

Fig. 8: Transfer characteristics of the extracted NS device

IV. Conclusion

A novel image detection library, based on OpenCV, tuned for the identification of advanced node device structures from EM images was presented. Its robustness and efficiency was shown by obtaining device characteristics of a 7 nm FinFET as depicted by its channel cross-section in a fully automated workflow. An exemplary variability study identifying the impact of fin bowing on transfer characteristics showed the ease with which to accurately model process variations with the STIR library. Furthermore, the gate cross-section of a stacked NS FET was used to show the versatility of the library supporting a range of technologies and cut orientations.
Moreover, selective use of the extracted material geometries in process emulation expands the realm of possible use cases, such as only extracting the fin shape and adding the remaining materials in process emulation to desired specifications. The benefits of STIR are multifaceted in combining the accuracy of real measurement data with the flexibility of process emulation, resulting in a more streamlined TCAD workflow. The presented approach thus enables process engineers to quickly and accurately model real devices to accelerate the development of advanced technologies.

References

[1] Global TCAD Solutions, “ProEmu”.[Online]. Available: https://www.globaltcad.com/proemu/
[2] G. Bradski et al., “OpenCV”.[Online]. Available: https://opencv.org/
[3] C. Tomasi et al., Proc. ICCV, pp. 839-846, 1998.
[4] W. Burger et al., “Digital Image Processing”, pp. 261-273, 2022.
[5] B. Batchelor et al. “Morphological Image Processing”, pp. 801-870, 2012.
[6] F. Bolleli et al., IEEE Trans. on Image Process., vol. 29, pp. 1999-2012, 2020.
[7] Hitachi High Technologies, “TEM observation of the FinFET in a 7 nm process SRAM,” [Online]. Available: https://biz.hitachi-hightech.com/sinavi/asi_applicationdetail?kijiId=AP100473&viewLanguage=en_Us
[8] J. Bobinac et al., Micromachines, vol. 14, no. 3, pp. 665, 2023.
[9] S. Lee et al., Nanomaterials, 12, 3349, 2022.
[10] P. Magnone et al., IEEE Trans. Electron Devices, vol. 57, no. 11, pp. 2848-2856, 2010.
[11] T. Shen et al., Proc. IRPS, pp. 1-5, 2020.