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Process Emulation and Device Simulation of Monolithic CFET Inverter and Transmission Gate with Split-Gate Structure

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***Abstract*— In this work, by using an in-house process emulator, the monolithic CFET technology has been considered. Two fabrication options – a conventional common-gate structure and a split-gate structure – are proposed. With the split-gate structure, a transmission gate, which is essential in realizing the standard logic cells, can be fabricated without any area penalty. Electrical performance of an inverter and a transmission gate is also simulated with an in-house device simulator. The subthreshold swings (SS) of 70.1mV/dec and 69.6mV/dec are obtained for the NMOSFET and the PMOSFET, respectively. The transient simulation results for a transmission gate with 1fF and 0.1fF load capacitances show: τPLH of 3.45ps and τPHL of 3.49ps at 1fF, and τPLH of 0.55ps and τPHL of 0.52ps at 0.1fF.**

Keywords—CFET, GAA, Inverter, Split-Gate, Transmission Gate, process emulation, device simulation.

I. Introduction

The complementary field-effect transistor (CFET) technology has gained research interest recently. This technology is inspired by the complementary nature of the logic circuits, where a pair of MOSFETs shares a common input signal. However, the complementary relation is sometimes disrupted, as exemplified by SRAMs and the transmission gate [1]. Since the transmission gate is a crucial component of standard logic libraries, it is important to integrate it within the CFET technology. Therefore, there is an urgent need to develop the CFET technology which supports the split-gate option. Constructing logic with a split-gate structure allows for area efficiency through the use of transmission gates, and enables application in CMOS logic devices. In contrast to the common-gate structure, which requires only one metal line, the frontside interconnection of the split-gate structure may potentially suffer from a crowding issue [2]. These congestion issues can lead to electrical signal interference and result in performance degradation of the device. Therefore, an effective interconnection method is necessary to address these problems.

In order to address this issue, the split-gate structure with the backside interconnection is proposed in this work. GAA (3-nanosheet channel) transistors are stacked and used for both the top NMOS and the bottom PMOS. The fabrication flows of the conventional common-gate structure and the split-gate structure are followed by using our in-house TCAD process emulator, which can directly generate a 3D mesh for device simulation from the emulation results. The performance of the common-gate CFET inverter and the transmission gate with the split-gate structure is also evaluated using our in-house device simulator.

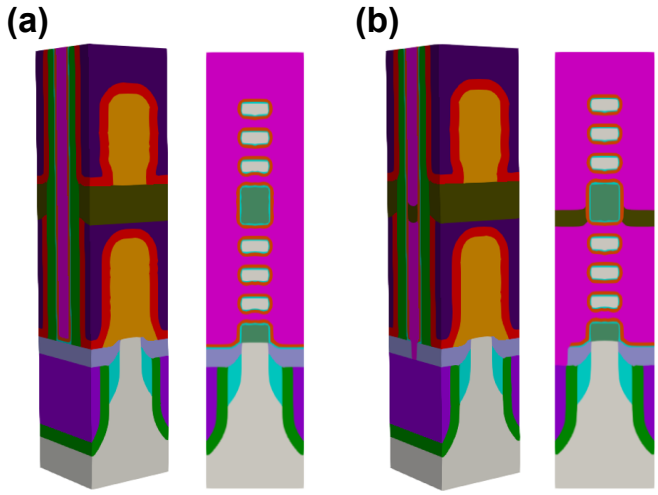

Fig. 1. CFET device and cross-section of (a) the common-gate structure and (b) the split-gate structure with the bottom PMOS gate connected to the BPR.

II. Process Emulation

The process emulation for the CFET inverter and the transmission gate has been conducted using an in-house emulator, G-Process [3], which implements the 3D multi-level-set method. The marching cube algorithm for the boundary extraction and the sparse field method for fast computation have also been employed [4][5]. Fig. 1 compares a CFET inverter with the common-gate structure and a CFET transmission gate with the split-gate structure.

The device structure comprises a bottom PMOS and a top NMOS. The middle dielectric isolation (MDI) is employed for smooth work-function metal (WFM) patterning of the top and bottom devices. When a thick SiGe sacrificial layer is included in the CFET epi stack, sufficient N-P space in the split-gate should be ensured. The MDI can simplify formation of inner spacer and multi-Vt patterning [6].

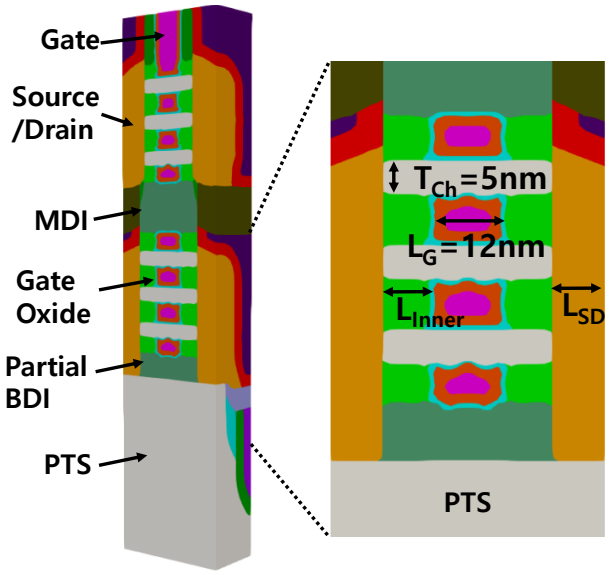

Fig. 2. Schematic of the simulated CFET with a partial BDI under the gate. BDI is only located under the gate and inner spacer regions, and not under the S/D regions.

Considering the compressive stress associated with the presence of Si bulk at bottom PMOS, Fig. 2 shows a partial bottom dielectric isolation (BDI) structure with the punch-through stopper (PTS) scheme [7-9]. To prevent leakage current due to the absence of BDI under the source/drain (S/D), the PTS doping has been considered. The Si substrate is doped with a concentration of $10^{19}cm^{-3}$ for reduced the leakage current.

Key parameters used in process emulation and device simulation are as follows. The contacted poly pitch (CPP) is 42nm, which is defined with the channel width of 12nm for both top and bottom devices. The top device has an inner spacer of 5nm and a gate length of 12nm. In contrast, the bottom device, defined by cavity patterning, features a channel length of 26nm and an inner spacer of 7nm. The thickness of HfO_2(/SiO_2) layer is set as 1.5nm(/0.7nm).

Fig. 3 shows the process flows for a CFET inverter with a common-gate structure. It includes MDI and partial BDI formation as depicted in Fig. 3(b). It also includes cavity patterning as depicted in Fig. 3(c), which uses a cover spacer to protect the top Si channel during the epitaxial growth of the bottom S/D [10]. In this work, the cover spacer is deposited at a thickness of 2nm. The thickness of the cover spacer used in cavity patterning results in differences in inner spacer thicknesses and channel lengths between NMOS and PMOS. The top S/D region is initially etched, followed by the formation of the inner spacer and the deposition of the cover spacer. Subsequently, the same process is replicated for the bottom S/D region. After the cavity patterning, the epitaxial growth of the S/D and contact formation are conducted from the exposed Si channel in the bottom region. To isolate the top and bottom S/D regions, dielectric fill, top S/D epitaxial growth, and contact formation are subsequently performed, as depicted in Figs. 3(e) and (f). Next, dummy gate removal and $Si_{0.8}Ge_{0.2}$ sacrificial layer release are performed, followed by WFM patterning, gate oxide (HfO_2/SiO_2) formation, and gate metal deposition, as shown in Figs. 3(g) and 3(h).

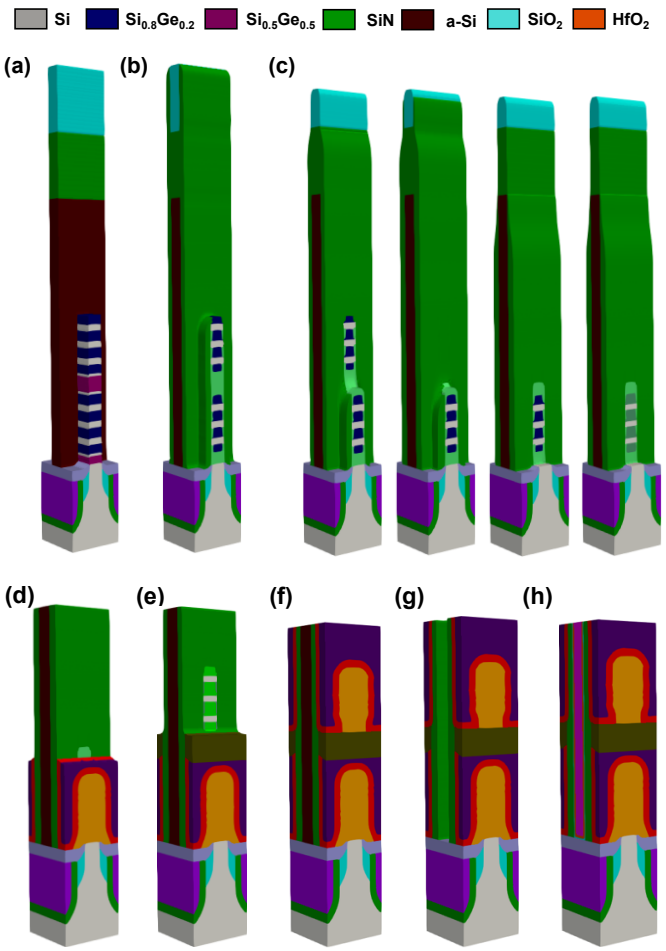

Fig. 3. Process emulation flow of the CFET inverter with common-gate. (a) Dummy gate patterning (b) Gate spacer deposition after MDI and partial BDI formation (c) Cavity patterning for top and bottom isolation (d) Bottom S/D epitaxial growth and contact formation (e) Dielectric fill for top and bottom isolation (f) Top S/D epitaxial growth and contact formation (g) Dummy gate removal and $Si_{0.8}Ge_{0.2}$ sacrificial layer release (h) WFM patterning and gate metal deposition.

The split-gate process for the transmission gate follows the same steps as the common-gate process up to the dummy gate removal and SiGe release stages, as shown in Fig. 3(g), but diverges in the subsequent steps. Fig. 4 illustrates the split-gate process flow following the dummy gate removal and SiGe release steps in the CFET common-gate process flow. As shown in Fig. 4(b), after patterning with spin-on carbon (SOC), high aspect ratio (HAR) etching for backside interconnection is performed. Subsequently, SOC removal and bottom gate metal formation are conducted. The gate metal formation process can include WFM patterning using SOC. After the formation of the bottom gate contact, dielectric fill and top gate metal formation for the split-gate are performed.

The interconnection for the split-gate is expected to be carried out using either the buried power rail (BPR) or the top contact, as illustrated in Fig. 5**.** In addition to the BPR, the bottom direct contact (BDC) may also be considered as a potential option for the backside interconnection [11].

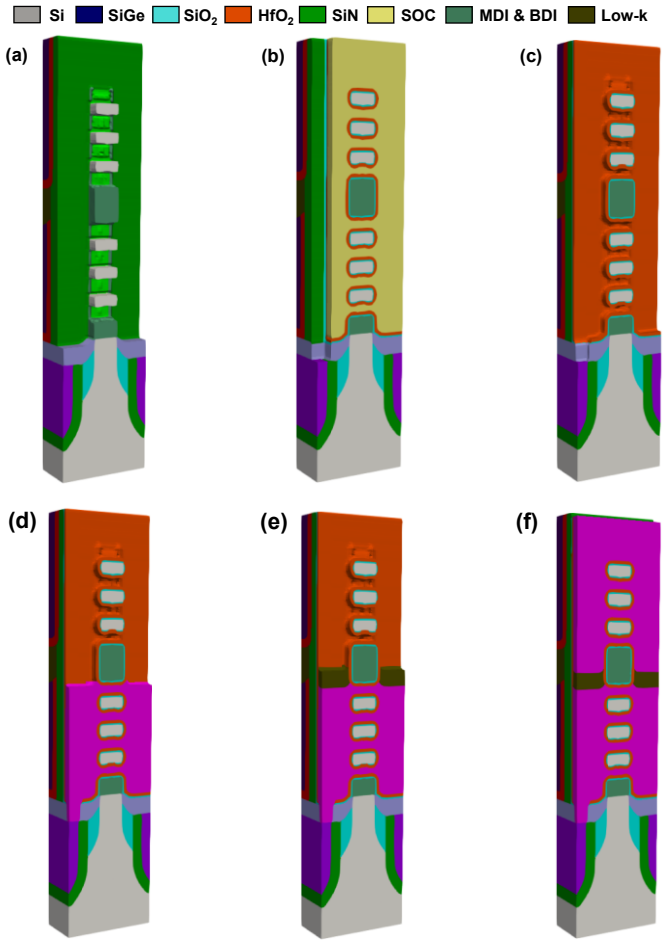

Fig. 4. Process flow for a CFET technology with the split-gate structure. The bottom-tier PMOS gate is connected to the backside interconnection.(a) Dummy gate removal and $Si_{0.8}Ge_{0.2}$ sacrificial layer release (b) SOC patterning and HAR etching for backside interconnection (c) SOC removal (d) Bottom gate metal formation (e) Dielectric (low-k) fill for isolation (f) Top gate metal formation

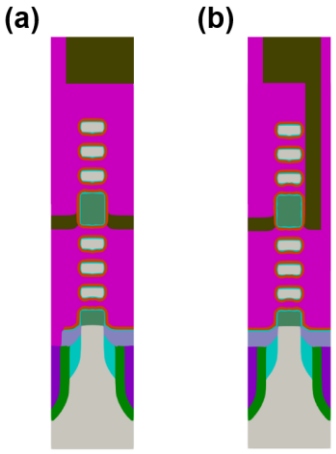

Fig. 5. Two types of possible interconnections. (a) The backside (b) The frontside.

III. Device Simulaion

The electrical characteristics of the CFET inverter and transmission gate are evaluated by using our in-house device simulator, G-Device [12].

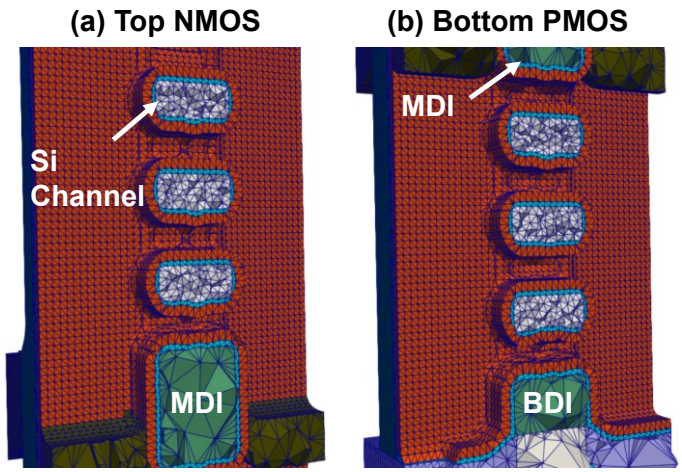

Fig. 6. Three-dimensional tetrahedron mesh for the device simulation. (a) Top NMOS (b) Bottom PMOS.

	Top NMOS	Bottom PMOS
CPP (nm)	42	42
L_G (nm)	12	12
L_{SD} (nm)	10	8
Inner spacer (nm)	5	7
$W_{channel}$ (nm)	12	12
$T_{channel}$ (nm)	5	5
T_{HfO2} (nm)	1.5	1.5
T_{SiO2} (nm)	0.7	0.7

TABLE I. The Geometric Parameters of the CFET Devices.

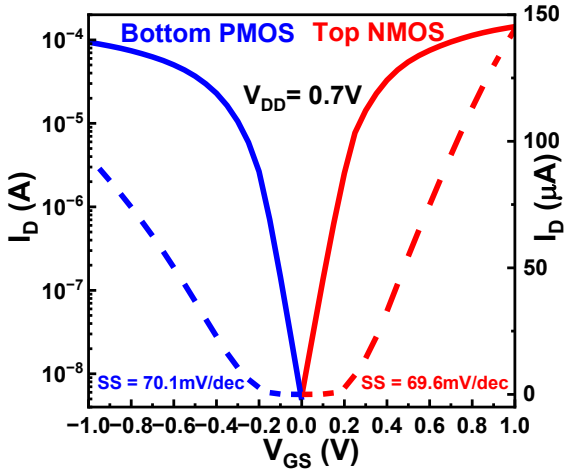

Fig. 7. DC I-V characteristics of 42nm CPP NMOS and PMOS.

The boundary structure generated from process emulation is directly used to generate a 3D mesh for device simulation as shown in Fig. 6. Therefore, the parameters used in the device simulation are identical to the structures generated from process emulation, as summarized in Table I.

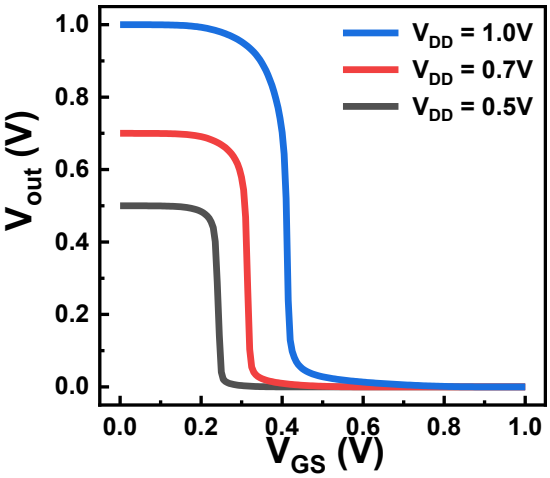

Fig. 8. DC I-V characteristics of an inverter.

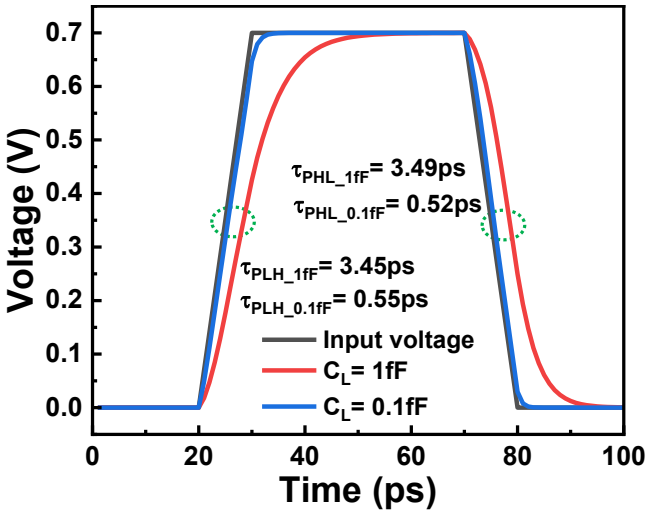

Fig. 9. Propagation delay of a transmission gate with load capacitances of 1fF and 0.1fF.

TetGen has been utilized for the generation of the 3D mesh [13]. In the device simulation, the physics model employed included the velocity saturation, Shockley-Read-Hall (SRH) recombination, and effective intrinsic density models.

Fig. 7 show the SS of 70.1mV/dec and 69.6mV/dec for NMOS and PMOS, respectively. Fig. 8 shows the voltage transfer curve of the inverter based on CFET with a common-gate structure. Transient simulation for a CFET transmission gate with a split-gate structure is conducted assuming load capacitances of 0.1fF and 1fF. Transient simulation results for a transmission gate with 1fF and 0.1fF load capacitances show: τ_{PLH} of 3.45ps and τ_{PHL} of 3.49ps at 1fF, and τ_{PLH} of 0.55ps and τ_{PHL} of 0.52ps at 0.1fF, as shown in Fig. 9.

IV. Conclusions

In order to fully utilize CFET as a CMOS logic device, the transmission gate is necessary. Therefore, a simulation study on the split-gate structure with backside interconnection has been conducted. In this study, process emulation was conducted using BPR for backside interconnection, but the option of bottom direct contact is also anticipated to be feasible. The TCAD process emulation for the CFET inverter and transmission gate with the split-gate structure has been performed using a process flow that includes PTS, backside interconnection with bottom PMOS, and cavity patterning for the top and bottom S/D isolation. Subsequently, the device simulation has been conducted to assess the electrical characteristics of the generated structure.

V. Acknowledgement

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