Predictive Simulation of Nanosheet Transistors including the Impact of Access Resistance

Tapas Dutta*†, Fikru Adamu-Lema*†, Nikolas Xeni*†, Ali Rezaei*, Ankit Dixit*,
Ismail Topaloglu†, Vihar Georgiev*, Asen Asenov*†

*Device Modelling Group, School of Engineering, University of Glasgow, Glasgow, Scotland, UK.
†Semiwise Ltd., Rankine Building, Glasgow, Scotland, UK.
e-mail: tapas.dutta@glasgow.ac.uk

2024 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD) | 979-8-3315-1635-2/24/$31.00 ©2024 IEEE | DOI: 10.1109/SISPAD62626.2024.10733048

***Abstract*—In this work we present a hierarchical computational approach to study the impact of source/drain access resistance in nanosheet transistors at the 3nm technology node and beyond. We employ the non-equilibrium Green's function (NEGF) approach to derive the current-voltage characteristics of the nanosheet transistors having extremely short source/drain extensions. Subsequently, we calibrate our quantum-corrected drift-diffusion simulator based on the density gradient formalism, which is then used to simulate structures with realistic lengths of source/drain regions. The device characteristics thus obtained reflect the impact of the access resistance. We analyse the impact of geometry scaling and doping levels in the Source/Drain extensions on the access resistance for different technology nodes.**

***Index Terms*—Nanosheet, Transistors, NEGF, Density-Gradient, Drift-Diffusion, Access Resistance**

I. Introduction

Nanosheet field effect transistors (NSFETs) have become the flagship transistors driving the semiconductor industry from the 3 nm node and beyond [1]. Mitigating source/drain access resistance is a significant challenge in enhancing complementary metal-oxide-semiconductor (CMOS) device performance, particularly in advanced technology nodes, and there has been a continuous focus on researching and implementing strategies for achieving this [2]–[4], and hence it is crtical to consider access resistance while designing NSFETs.

In this work we present a methodology to capture the impact of source/drain access resistance(R_{SD}) in the extremely scaled state-of-the-art nanosheet transistors combining full quantum transport simulations with quantum-corrected drift-diffusion simulations. We perform R_{SD} extraction using a modified Y-function approach, and compare R_{SD} for different technology nodes, and examine the impact of cross-section scaling. We also demonstrate the significance of R_{SD} in determining the on-current variability in nanosheet transistors considering random discrete dopants (RDD) in the source/drain regions. The approach is implemented using our in-house TCAD tool NESS (Nano-Electronic Simulation Software) [5]–[8].

II. Methodology

The approach utilized in this study is outlined in the flowchart depicted in Fig. 1. The first step is the creation of the device structure using the Structure Generator module of NESS. To include the impact of cross-sectional dimensions and crystal orientation, we then perform bandstructure calculations based the tight-binding approach. One can choose to use first principles based calculation e.g. density functional theory as well. These simulations allow us to extract the electronic band structure of the nanosheets as the cross-section thickness varies while the width is kept the same. From the bandstructure, the effective masses in the transport and confinement direction in the NSFETs are extracted using the

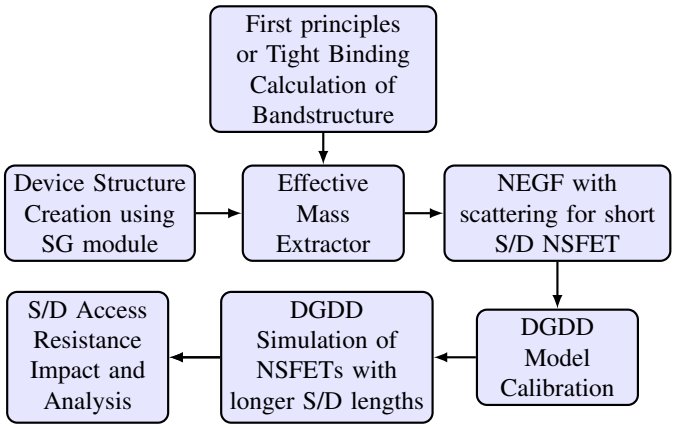

Fig. 1. Summary of the methodology used in this work using the various modules of NESS.

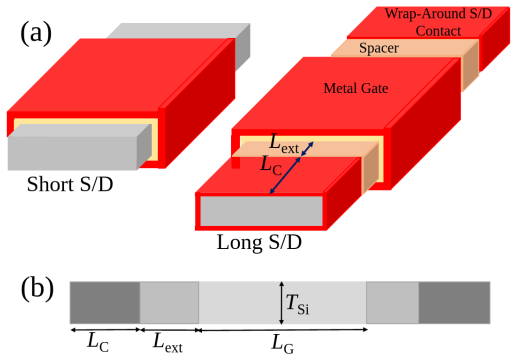

Fig. 2. Schematics of NSFET Devices: (a) 3D view of the short and long Source/Drain devices (b) channel region with critical dimensions in this study. T_{Si} = channel thickness, = channel width, L_G = channel length, L_{ext} = S/D extension length, L_{SDC} = S/D contact length.

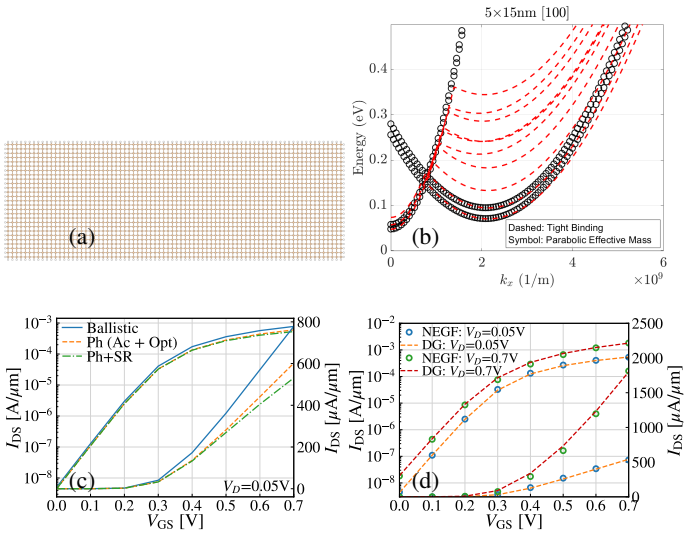

Fig. 3. (a) The atomistic representation of the 5nm X 15nm cross-section nanosheet set up in QATK. (b) Bandstructure: QATK output vs parabolic effective mass approximation using the EME module. (c) I_D-V_G characteristics of the short S/D NSFET from the NEGF solver considering Ballistic transport, and with acoustic and optical phonon scattering (Ac + Opt), and phonons and surface roughness scattering both acting together (Ph +SR) showing cumulative reduction in the transistor current. (d) I_D-V_G calibration of the DGDD simulator to NEGF results (including phonons and surface roughness scattering) at low and high drain bias for the 'short' S/D device (shown in Fig. 2(a)). Note that this device has S/D region length of 1nm with doping of $5{\times}10^{20}$ cm^{-3}.

Effective Mass Extractor module of NESS [9].

NESS incorporates a range of transport solvers, spanning from classical to full quantum formalisms. Given that quantum confinement and tunneling effects play a crucial role in highly scaled devices such as these nanosheet transistors, the most robust formalism that can be used is the non-equilibrium Green's function (NEGF) approach. To achieve accurate device simulations, we activate dissipative transport in the NEGF solver. This entails considering phonon (acoustic and optical) and surface roughness scattering mechanisms using the self-consistent Born approximation (SCBA). Note that this module involves a self-consistent solution of the Poisson's equation and the NEGF equations within the framework of the coupled mode space approach.

We start with the NEGF simulation of nanosheet transistors with short source/drain regions (1 nm long each) including phonons and surface roughness scattering (but no impurity scattering). This essentially captures the intrinsic performance of the device with minimal impact of the S/D regions. Next, we calibrate the density gradient based quantum-corrected drift-diffusion solver (DGDD) in NESS [10] to the NEGF results. The DGDD solver uses the solution of the density gradient equation to apply quantum correction to the classical DD formalism. It is relatively faster than the other option of using Schrödinger equation based quantum correction [11].

The key parameters tuned for the DG solver are the three anisotropic DG effective masses that account for the quantum behavior. Quantum confinement is captured via the transverse

TABLE I
NOMINAL NSFET DEVICE: GEOMETRY AND DOPING

Parameter	Value
L_{G} (Gate Length)	16 nm
T_{Si} (Channel Thickness)	5 nm
W_{Si} (Channel Width)	15 nm
L_{ext} (S/D Extension Length)	6 nm
L_{SDC} (S/D Contact Length)	10 nm
EOT (Effective Oxide Thickness)	1 nm
N_{Ch} (Doping in Channel)	1e15 cm^{-3}
N_{Ext} (Doping in S/D Extension)	1e20 cm^{-3}
N_{SDC} (Doping in S/D Contact)	5e20 cm^{-3}

DG effective masses, while Source-to-Drain tunneling can be mimicked by the longitudinal DG effective mass (which is kept high in our study as the gate lengths are long enough to ignore S-to-D tunneling). The other set of parameters that are extracted are those of the DD mobility models: namely the Masetti model (takes into account the impact of doping dependence of mobility), the Yamaguchi model (to capture the effect of the vertical electric field), and the Caughey-Thomas model (to incorporate the impact of the longitudinal electric field on mobility).

We then simulate more realistic nanosheet structures with longer source/drain lengths (with varying S/D extensions i.e. access region lengths) using the calibrated DGDD solver. The difference in the current-voltage characteristics obtained from these devices with different S/D extension regions highlights the impact of the source/drain access resistance. Further, the doping in the access regions will affect the access resistance and the drive currents, and hence we have performed simulations with multiple access region doping as well.

III. Results and Discussion

Fig. 2 shows the NSFET structure with channel thickness T_{Si} of 5 nm, channel width, W of 15 nm, gate oxide (SiO_2) thickness 1 nm, and channel length, L_G of 16 nm which corresponds to the "3nm" technology node [12]. The "nominal" NSFET device is the one corresponding to the IRDS 2022 recommendations for 3 nm node. The relevant device parameters are listed in Table I. The doping in the channel is $1{\times}10^{15}$ cm^{-3} and $5{\times}10^{20}$ cm^{-3} in the S/D contact regions. The 'short' S/D device has S/D region length of 1nm with doping of $5{\times}10^{20}$ cm^{-3}. In the 'long' S/D devices, the S/D region is split into two parts: extension region with length equal to the spacer length and is varied from 1 nm to 8 nm (the nominal spacer length is 6 nm as per IRDS recommendations), and the contact region length (L_{SDC}) which is fixed to 10 nm.

Fig. 3(a) illustrates the atomistic depiction of a nanosheet cross-section with 5nm X 15nm dimensions in the Quantum ATK (QATK) set up. The parabolic effective masses that were extracted yield a strong agreement with the band structure obtained using the QuantumATK tool [13], particularly in the vicinity of the band minimum. This correspondence is shown in Fig. 3(b).

The I_D-V_G characteristics, obtained from the NEGF solver, are presented in Fig. 3(c). It presents three cases: pure ballistic transport, transport with acoustic and optical phonon scattering, and transport with the combined effects of phonon and surface roughness (SR) scattering. As expected, as we add more sources of scattering, the drive current further reduces. Note that in this paper, all currents in units of per μm are normalized to the device lateral pitch, which for the 3nm node is set to 24 nm as per IRDS.

A. DGDD Calibration of the "short S/D" NSFET

Fig. 3(d) displays the I_D-V_G characteristics of the short source/drain (S/D) NSFET at low and high drain biases obtained from the NEGF simulations, considering various scattering mechanisms, and from the calibrated DGDD simulations, demonstrating the excellent agreement achieved. For this, we adjust parameters such as the gate workfunction, mobility parameters, and effective masses within the DGDD model, as described in section II.

B. Impact of Extension Region on Drive Current

Using the calibrated DGDD parameters, we simulate NSFET devices with different extension region lengths (L_{ext} varying from 1 nm to 8 nm) and extension region doping (N_{ext} varying from 1e20 to 5e20 cm^{-3}. A comparison of the transfer characteristics of the NSFETs with varying extension region lengths for the extension region doping of 1e20 cm^{-3} has been shown in Fig. 4.

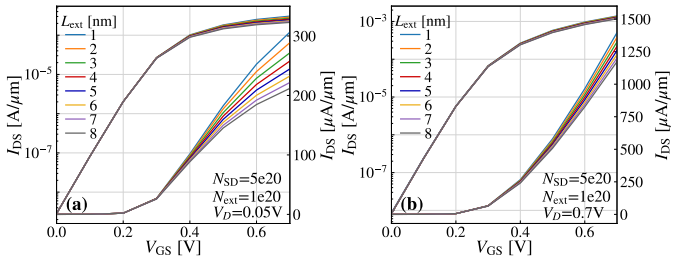

Fig. 4. DGDD Simulation of longer L_{SD} NSFETs (a) low V_D (b) high V_D for extension region doping (N_{ext}) of 1e20 cm^{-3}. S/D extension lengths from 1 nm to 8 nm, in steps of 1 nm were considered. The S/D region length under contacts remains fixed at 10 nm with a doping of 5e20 cm^{-3}.

The on-state current I_{ON} in linear and saturation regimes as a function of the source/drain extension length for different doping in the extension regions is shown in Fig. 5. We observe the degradation in the on-state current with increasing L_{ext} in almost linear fashion. A higher N_{ext} doping results in higher I_{ON}, but the gains obtained by increasing N_{ext} tend to saturate as we approach the doping under the S/D contact regions.

C. Access Resistance: Extraction and Analysis

1) Extraction of Access Resistance: There are several approaches present in literature to extract the source/drain access resistance [3]. We use the methodology described in [14], which has been shown to be applicable to nanowire FETs,

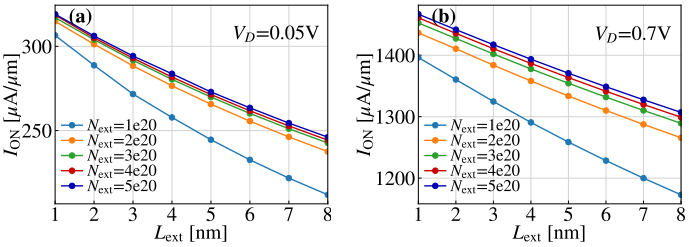

Fig. 5. ON-current as a function of the S/D extension region length at (a) low and (b) high drain bias.

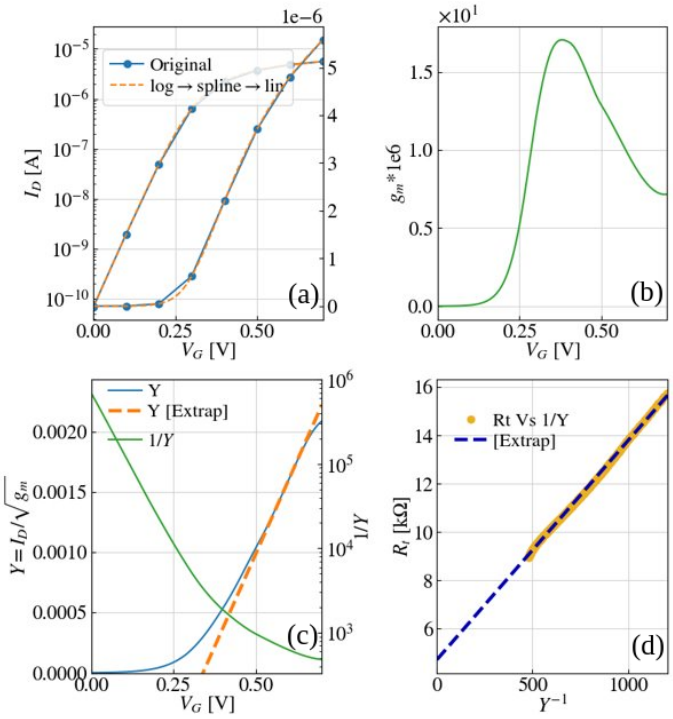

Fig. 6. Summary of the R_{SD} extraction steps: (a) $I_{\text{DS}} - V_{\text{GS}}$ interpolation, (b) Transconductance (g_m) calculation, (c) Calculation of the Y function, its inverse, and extrapolation, (d) R_t (total resistance) Vs Y^{-1} (inverse of Y function) in the relevant gate bias range and extrapolation to extract R_{SD} from the y-axis intercept.

and is expected to work for the nanosheet FETs we are analysing in this work. The method is based on the Y-function [15] and extracts the source/drain resistance as the y-axis intercept from a linear extrapolation of the plot of the total resistance against the inverse of the Y-function i.e. $\sqrt{g_m}/I_D$, where g_m is the transconductance, and I_D, the drain current. The R_{SD} extraction is performed at a low drain bias. A demonstration of the method, as applied to our NSFET devices, is shown in Fig. 6.

2) Impact of L_{ext} and N_{ext} on Access Resistance: The R_{SD} thus extracted as a function of the source/drain extension length for the different doping values in the extension regions is shown in Fig. 7(a). We observe a linear increase in R_{SD} with

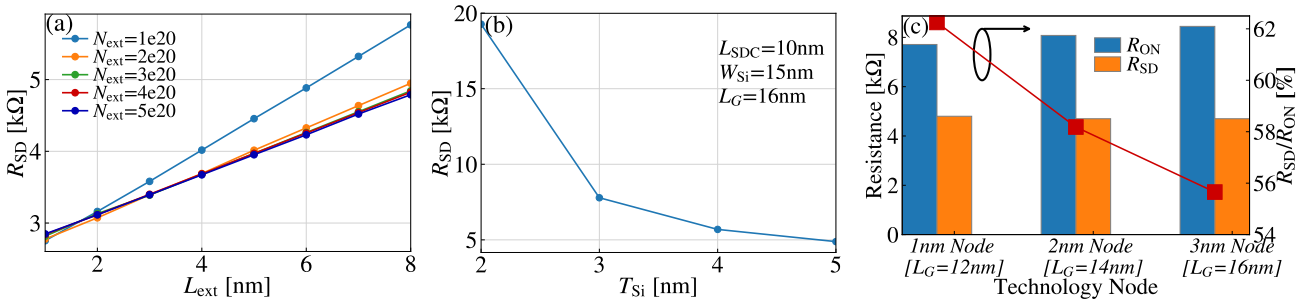

Fig. 7. (a) R_{SD} as a function of source/drain extension lengths, L_{ext} for different doping in the source/drain extensions. We observe a saturation in the R_{SD} values for N_{ext} above 2e20 cm^{-3}. The extractions were performed on $I_{DS} - V_{GS}$ curves simulated at V_{DS}=0.01V. (b) R_{SD} as a function of channel thickness at 3nm node. (c) Left axis: Comparison of R_{SD} and R_{ON} at different technology nodes for fixed cross-section dimensions (5 nm × 15 nm). Right axis: the ratio R_{SD}/R_{ON} in %.

increase in the extension length. Further, a sharp drop in R_{SD} is seen when going from N_{ext} of 1e20 cm^{-3} to 2e20 cm^{-3}, with little change with further increase in N_{ext}.

3) Cross-Section Dependence of Access Resistance: With cross-section scaling, R_{SD} becomes increasingly important, along with the inherent mobility degradation. We extend the approach described in section II to consider NSFET devices at the 3nm node, with the channel thickness varying from 2nm to 5nm with the other geometrical and doping parameters remaining the same. Following the same approach, we extract the S/D resistance as a function of T_{Si}. As shown in Fig. 7(b), we see a non-linear increase in the access resistance with scaling down of the channel thickness. The novelty of this study is that it connects the changes in quantum confinement manifested via effective masses to R_{SD}.

4) Access resistance for Beyond 3nm Node: We consider the 2nm and 1nm technology nodes, characterized by the channel lengths of 14 nm and 12 nm respectively [12]. For this we have kept the nominal cross-section of 5 nm X 15 nm, and the same doping levels as the 3nm node devices studied earlier. We again use the flow summarized in Fig. 1. The mobility models are re-calibrated for the different gate lengths. We extract the S/D access resistance and also further compare the S/D access resistance to the total on resistance ($R_{ON} = V_{DD}/I_{ON}$). While the R_{SD} itself doesn't change much, we find that the contribution of the access resistance to the total resistance increases from 55.5% at the 3nm node to 61.7% at the 1nm node as illustrated in Fig. 7(c).

IV. Conclusion

We have introduced a methodology to investigate the impact of source/drain access resistance in advanced nanosheet FETs, combining comprehensive quantum transport simulations based on NEGF formalism with quantum-corrected drift-diffusion simulations. The results obtained underscore the necessity of minimizing the lengths of source/drain regions while keeping the doping high. These measures are essential to prevent the loss of drive current, even in the presence of well controlled electrostatics in gate-all-around nanosheet FETs operating under near-ballistic intrinsic conditions. Cross-section scaling leads to non-linear increase in R_{SD}. The dominance of the source/drain access resistance over the total on-resistance intensifies at advanced technology nodes. An extension of this work would be to study the impact of random discrete dopants in the S/D regions on R_{SD}.

References

[1] G. Bae *et al.*, "3nm gaa technology featuring multi-bridge-channel fet for low power and high performance applications," in *IEEE International Electron Devices Meeting (IEDM)*, 2018, pp. 28–7.

[2] S.-C. Fan *et al.*, "Parasitic resistance reduction for aggressively scaled stacked nanosheet transistors," in *IEEE International Interconnect Technology Conference (IITC)*, 2020, pp. 31–33.

[3] A. Ortiz-Conde *et al.*, "A review of dc extraction methods for MOSFET series resistance and mobility degradation model parameters," *Microelectronics Reliability*, vol. 69, pp. 1–16, 2017.

[4] K. Takeuchi *et al.*, "Variability of MOSFET series resistance extracted from individual devices: Is direct variability measurement possible?" in *2023 35th International Conference on Microelectronic Test Structure (ICMTS)*. IEEE, 2023, pp. 1–4.

[5] S. Berrada *et al.*, "Nano-electronic Simulation Software (NESS): a flexible nano-device simulation platform," *J. of Comput. Electron.*, vol. 19, pp. 1031–1046, 2020.

[6] C. Medina-Bailon *et al.*, "Simulation and modeling of novel electronic device architectures with NESS (nano-electronic simulation software): A modular nano TCAD simulation framework," *Micromachines*, vol. 12, no. 6, 2021.

[7] C. Medina-Bailon *et al.*, "Nano-Electronic Simulation Software (NESS): a Novel Open-Source TCAD Simulation Environment," *Journal of Microelectronic Manufacturing*, vol. 3, no. 4, p. 20030404, 2020.

[8] T. Dutta *et al.*, "TCAD Simulation of Novel Semiconductor Devices," in *14th IEEE International Conference on ASIC (ASICON)*, 2021.

[9] O. Badami *et al.*, "Comprehensive study of cross-section dependent effective masses for silicon based gate-all-around transistors," *Applied Sciences*, vol. 9, no. 9, p. 1895, 2019.

[10] T. Dutta *et al.*, "Density gradient based quantum-corrected 3D drift-diffusion simulator for nanoscale MOSFETs," in *16th IEEE Nanotechnology Materials and Devices Conference (NMDC)*, 2021, pp. 1–4.

[11] T. Dutta *et al.*, "Schrödinger Equation Based Quantum Corrections in Drift-Diffusion: A Multiscale Approach," in *2019 IEEE 14th Nanotechnology Materials and Devices Conference (NMDC)*, 2019, pp. 1–4.

[12] IEEE International Roadmap for Devices and Systems - IRDS 2022. (accessed: March 31, 2023). [Online]. Available: https://irds.ieee.org/images/files/pdf/2022/2022IRDS_MM.pdf

[13] Synopsys *QuantumATK*, 2023. [Online]. Available: https://www.synopsys.com/silicon/quantumatk/

[14] R. Trevisoli *et al.*, "A new method for series resistance extraction of nanometer MOSFETs," *IEEE Transactions on Electron Devices*, vol. 64, no. 7, pp. 2797–2803, 2017.

[15] G. Ghibaudo, "New method for the extraction of MOSFET parameters," *Electronics Letters*, vol. 24, no. 9, pp. 543–545, 1988.