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Optimization of Complementary Reconfigurable Field-Effect Transistor for Improved Circuit-Level Metrics

Juhan Ahn
Electrical and Computer Engineering
The University of Texas at Austin
Austin, Texas, USA
juhan.ahn@utexas.edu

Saroj Satapathy
Electrical and Computer Engineering
The University of Texas at Austin
Austin, Texas, USA
sarojs@utexas.edu

Jaydeep P. Kulkarni
Electrical and Computer Engineering
The University of Texas at Austin
Austin, Texas, USA
jaydeep@austin.utexas.edu

***Abstract*—The Reconfigurable Field-Effect Transistor (RFET) enables dual-mode (n-type and p-type) operation in a single device, enhancing circuit design efficiency. However, conventional silicon-based RFETs often exhibit low saturation currents, which restrict their application in high-performance circuits. In this study, the Complementary RFET (CRFET) was studied to overcome this limitation by optimizing p-type and n-type doping in a vertically stacked RFET configuration. Also, we present the enhanced CRFET (ECRFET), which incorporates a reduction of the Schottky barriers at the source/drain (S/D) contacts using platinum and titanium with a thin zinc oxide interfacial layer for p-type and n-type, respectively, along with the S/D doping. Both the CRFET and ECRFET achieve significantly improved performance with near-zero ION variability, operating effectively at a low voltage of 0.7 V. Compared to conventional RFETs, the ECRFETs show significantly higher ON-currents, with the p-type and n-type increasing by factors of 281 and 152, respectively, while maintaining an OFF-current below 1×10^{-11} A. Moreover, ECRFET-based 6T SRAM exhibits read SNM at 185 mV.**

Keywords—Reconfigurable Field-Effect Transistor, Schottky Barrier, Workfunction, Metal-Interfacial Layer-Semiconductor Source/Drain, TCAD, Verilog-A Model, SPICE, SRAM

I. Introduction

With the ongoing reduction in semiconductor process dimensions, transistor sizes are rapidly approaching the physical limitations of silicon, leading to considerable production challenges and cost-related issues. The reconfigurable field-effect transistor (RFET) emerges as a key innovation, capable of exhibiting both n-type and p-type behavior [1]. This dual-mode operation not only enhances design flexibility but also allows for denser functional integration within the same chip area, thereby achieving the same functionality with a reduced number of transistors. The remarkable reconfigurability of RFETs signifies a new era in integrated circuit design, extending beyond the conventional limits set by Moore's Law. Research efforts since the introduction of the RFET concept have spanned Technology-Computer Aided Design (TCAD) simulations [7], [16], theoretical modeling [15], and empirical studies [1], [14].

Despite the innovative nature of RFETs, their application in high-performance circuits is limited by insufficient saturation drive currents and the necessity for high operating voltages (V_{OP}), primarily because of the challenges in overcoming the high Schottky barrier (SB) at the source/drain (S/D) contact region. The Wentzel-Kramers-Brillouin (WKB) approximation-based tunneling model indicates that enhancing the tunneling probability for carriers can be achieved by employing channel materials with a smaller bandgap [10], or by reducing carrier effective tunneling masses [11], [12]. Alternatively, enlarging the area where carrier tunneling occurs can be accomplished through structural redesign [13]. However, the majority of existing studies rely on Schottky tunneling with metallic S/D contacts, typically using nickel silicide (NiSi) (see Fig. 1(a)), to ensure symmetric performance between n-type and p-type configurations [1]. This reliance makes it difficult for carriers to overcome the SB, which is typically over 0.5 eV. Another study introduces a fin-shaped RFET with dual-doped S/D contacts for higher ON-current (I_{ON}) [7]. Nevertheless, the complexity of the fabrication process not only renders this design more difficult to manufacture compared to other RFETs but also poses significant challenges for large-scale integration.

To overcome such challenges, we propose an optimized design termed the complementary RFET (CRFET) [2]. This novel architecture advances the conventional RFET paradigm by vertically integrating a pair of RFETs, employing strategic doping to configure a dual RFET system—one serving as a p-type and the other as an n-type device. In this innovative architecture, the source, drain, polarity gate (PG), and control gate (CG) terminals of the two transistors are individually interconnected, allowing the device to function as either type within the spatial confines occupied by a single RFET. Additionally, we present an advanced version of the CRFET, termed the Enhanced CRFET (ECRFET), which demonstrates even improved I_{ON} at reduced operational voltages of 0.7 V, surpassing those of the conventional RFETs. We achieve this enhancement by adopting methods to reduce contact resistance, focusing particularly on adjusting the SB height at the S/D. This modification involves the deliberate selection of contact metals that are most effective in enhancing this property: platinum is used for p-type enhancement, while titanium (Ti) and zinc oxide (ZnO) are employed for n-type enhancement. Notably, the latter structure form a metal-interfacial layer-semiconductor (M-I-S) structure at the S/D contacts, which is effective in mitigating the

effects of Fermi-level pinning, as referenced in [5]. The electrical properties of the suggested designs were confirmed using TCAD device simulation tools. Moreover, Based on the TCAD simulation results, we developed a SPICE model of the ECRFET using Verilog-A [6]. This model is essential for conducting complex circuit simulations within a SPICE framework, enabling an in-depth evaluation of the CRFET's performance across various electronic circuit applications. The full ECRFET-based 6T SRAM circuit has been validated through SPICE simulation, showcasing the potential of ECRFETs in high-performance, low-power applications.

II. Simulation Method

To substantiate the proposed device architectures, three-dimensional (3-D) simulations were performed using Synopsys Sentaurus TCAD [3]. These simulations employed both doping-dependent and field-dependent mobility models to precisely represent the carrier transport characteristics. Additionally, the WKB-based Schottky tunneling model [3] and the associated tunneling masses [4] were implemented to accurately describe the tunneling mechanisms occurring near the S/D contacts. The work function of the NiSi S/D contacts in both the conventional RFET and the CRFET was set to 4.64 eV. In the case of the ECRFET, the work function for the p-type region was adjusted to 4.9 eV to counteract the Fermi-level pinning effect that occurs with the platinum (Pt) to silicon (Si) junction. For both the CRFET and the ECRFET, the doping concentrations in the source/drain regions were set at 1×10^{20} cm^{-3} for n-type and 6×10^{19} cm^{-3} for p-type. The gate work function for all gates was standardized at 4.68 eV to ensure uniformity throughout the devices. In the n-type part, a distributed resistance methodology was adopted, setting the contact resistivity at 1.9×10^{-8} Ω·cm^2. This technique was chosen to precisely represent the M-I-S S/D configuration of a Ti/ZnO/Si contact structure, as theoretically investigated in [5]. To ensure that the transistor pair operates effectively in dual-mode, we managed the terminals of both the upper and lower transistors simultaneously as a single unit.

Additionally, a Verilog-A model [6] was formulated based on the device simulation data acquired from TCAD under a range of operating conditions. To guarantee the model's accuracy, we varied the control gate voltage (V_{CGS}) and polarity gate voltage (V_{PGS}) in increments of 0.02 V, and adjusted the drain voltage (V_{DS}) in steps of 0.05 V. Using the developed model, we conducted circuit simulations for a 6T SRAM cell to validate its read margin.

III. Results and Discussion

A. Assessment of Innovative RFET Designs

The schematic diagrams, which include the device parameters of the standard RFET, CRFET, and ECRFET, are illustrated in Fig. 1(a), (b), and (c), respectively. Fig. 1(d) provides a 3-D representation of the proposed structure, emphasizing the primary (I_{major}) and secondary (I_{minor}) current pathways through the interconnected nodes when there is a shift in the polarity of the applied voltage. The transfer characteristics in Fig. 1(e) confirm that the CRFET exhibits a significantly increased I_{ON} compared to the RFET pair, which is attributed to the doping effect. Furthermore, the ECRFET shows an even higher I_{ON} as a result of the reduced SB. Notably, the enhancement in I_{ON} is more pronounced during low-voltage operational modes. At an V_{OP} of 0.7 V, the p-type operation mode shows a 281-fold enhancement and the n-type operation mode demonstrates a 152-fold increase in I_{ON} over their NiSi (conventional) RFET counterparts. Additionally, the suggested designs show a marked reduction in I_{ON} fluctuation in response to changes in V_{OP}. Although there was an increase in the off-current (I_{OFF}) for the ECRFET, it remained below 1×10^{-11} A for both operation modes. Fig. 2 compares the current flow in the ECRFET to that in a dual-stacked gate-all-around FET (GAAFET) configuration under the same n- and p-type doping scenarios. With the GAAFET duo, a current level close to the on-state is maintained even with reduced biases at the CG across both modes of operation, thereby compromising the transistor's ideal switching behavior. This occurs as a result of the interconnection at each terminal of the pair transistors, meaning that when the bias causes one transistor to deactivate, the other is automatically triggered to activate. In contrast, the CRFET

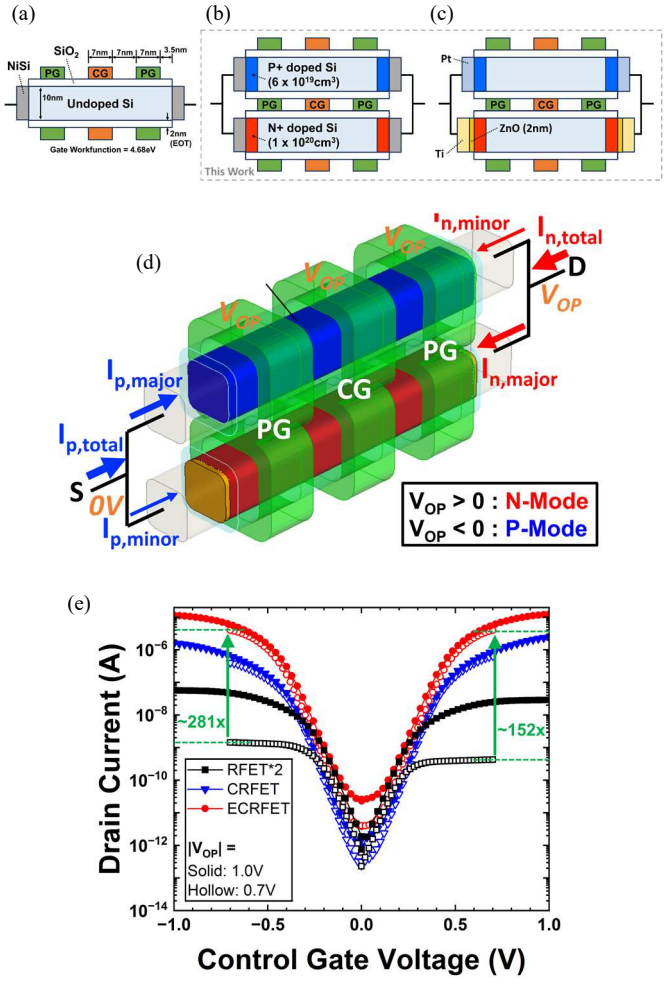

Fig. 1. (a) to (c) respectively show cross-sectional view of a conventional RFET, a CRFET, and an ECRFET. (d) illustrates the 3-D bird's eye view of the ECRFET used in TCAD simulations. (e) compares the I_D-V_{CGS} curves for the structures.

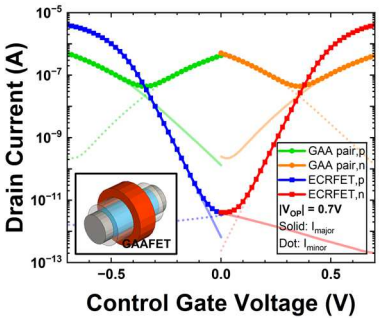

Fig. 2. Comparison of I_D-V_{CGS} curves between a pair of GAAFETs and an ECRFET, examining each current component and the overall total. The inset features the single GAAFET structure employed in the dual-stack arrangement.

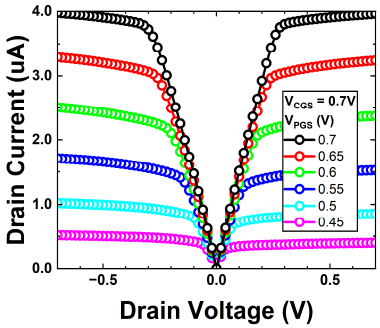

Fig. 3. The I_D-V_{DS} characteristics of the ECRFET, plotted as the V_{PGS} is altered in 0.05 V steps, with the V_{CGS} held constant at 0.7 V.

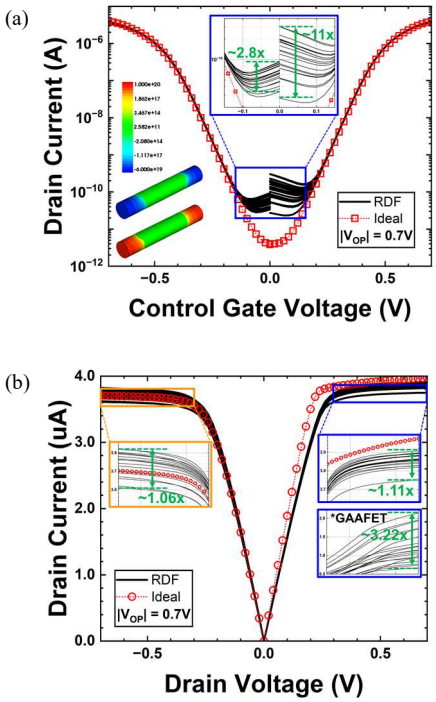

Fig. 4. Illustration of twenty randomly generated ECRFETs incorporating RDF effects (black line) versus an ideally doped ECRFET (red symbol) at $|V_{DS}|$=0.7 V: (a) the I_D-V_{CGS} characteristics with an inset showing one of the structures, and (b) the I_D-V_{DS} curves with an inset depicting the variation of I_{ON} in a GAAFET under identical device conditions.

effectively minimizes I_{minor} through the PG, ensuring proper performance for both polarities. Fig. 3 illustrates that the performance of the ECRFET is influenced by the bias applied to the PG, with increments of 0.5 V revealing a distinct variation in the I_{ON}. This feature offers the potential to adjust the device's driving strength without modifying the CG bias, thus providing an extra control parameter to enhance design flexibility. The electrical characteristics of 20 randomly generated ECRFETs affected by random dopant fluctuation (RDF) effect are depicted in Fig. 4, compared with the curve of a device with ideally abrupt doping profiles. Fig. 4(a) suggests that RDF has a relatively greater impact on the I_{OFF}. The underlying reason is that changes in the doping concentration in the edge of the S/D regions can modify the thickness of the tunneling barrier, which in turn can alter the tunneling probability of carriers in both the primary and secondary path transistors. Whereas, Fig. 4(b) shows a variation in I_{ON} of approximately 11 % for n-type and 6 % for p-type, significantly better than the GAAFET's ~322 % under the same device parameter settings. In the proposed structures, the S/D doping is established away from the region controlled by the CG, enabling the near-total elimination of RDF effects on I_{ON}.

B. Verilog-A Model Validation and Circuit Simulations

Fig. 5 presents the SPICE simulation outcomes for the ECRFET, utilizing a Verilog-A model that has been meticulously constructed from an extensive dataset comprising 19,440 I_D-V_{PGS} measurement points. The simulation results exhibit a high degree of correlation with the TCAD simulations, thereby substantiating the characteristics of the developed model. Subsequently, Fig. 6(a) illustrates the 6T SRAM cell architecture, which is completely based on the ECRFET. In this configuration, the PGs of both the access and pull-down transistors are connected to the *Vdd*, which is set at 0.7 V, while the PGs of the pull-up transistors are tied to the *Vss* (GND). Furthermore, Fig. 6(b) showcases the simulated read static noise margin (SNM) butterfly curve, which has been derived through HSPICE simulations employing the aforementioned Verilog-A model. The read SNM is evaluated through this graph to be around 185 mV, indicating stable and reliable operation of the SRAM cell. Further simulations can also be performed using this HSPICE model to determine the SRAM's minimum operating voltage (Vmin), performance, and aging characteristics [8], [9]. Additionally, this model can be utilized to design and simulate more complex circuits, providing a detailed comparison between CMOS and ECRFET technologies.

C. Performance Benchmark of RFETs

Table I presents a detailed comparative analysis of the electrical characteristics of the ECRFET with the conventional RFETs as reported in [1], [7]. This comparison is carried out by considering devices that are comparable in terms of their total channel lengths, ensuring a fair assessment of the performance metrics. Notably, the ECRFET developed in our study demonstrates a superior operational efficacy, particularly when evaluated at a significantly reduced V_{OP} of 0.7 V. This achievement is particularly significant as the applied voltage of the ECRFET is proximate to the standard voltage levels employed by cutting-edge CMOS technologies.

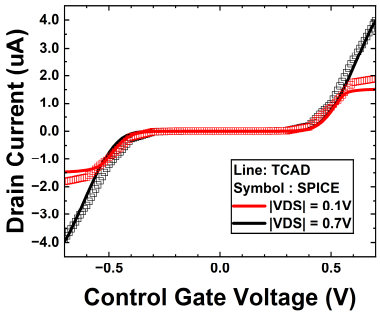

Fig. 5. Contrast between the I_D-V_{CGS} characteristics at different V_{DS} from HSPICE simulations using the Verilog-A model (symbol) and those obtained from TCAD simulations (line).

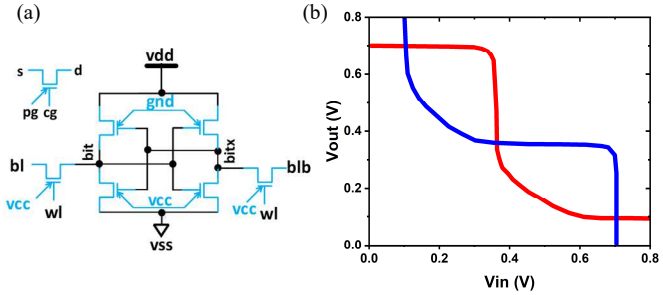

Fig. 6. (a) Schematic representation of the SRAM cell constructed entirely with ECRFETs and (b) the resulting read SNM butterfly curve derived from HSPICE simulation.

TABLE I. COMPARISON OF RFETS

Metrics	RFET [1]	RFET [7]	ECRFET (This work)
Channel length (Silicon edge-to-edge)	50 nm	50 nm	42 nm
I_{ON} [nMOS, pMOS]	~1 uA, >1 uA	~20 uA, ~20 uA	4.0 uA, 4.0 uA
Subthreshold Slope [nMOS, pMOS]	90 mV/dec, N/A	98 mV/dec, 94 mV/dec	71.9 mV/dec, 72. 7mV/dec
I_{ON}/I_{OFF} [nMOS, pMOS]	3×10^6, N/A	8×10^8, 1×10^9	$9{,}9\times10^5$ 1.04×10^6
Operating Voltages [$\lvert V_{PGS}\rvert$, $\lvert V_{CGS}\rvert$, $\lvert V_{DS}\rvert$]	1 V, 1 V, 1.2 V	2 V, 2 V, 2 V	0.7 V, 0.7 V, 0.7 V

IV. CONCLUSION

In our study, we introduce an optimized CRFET and an advanced version, the ECRFET, designed to deliver superior performance at reduced operating voltages. This is achieved by refining the Schottky barrier through selective doping of the S/D regions and incorporating a M-I-S S/D structure into the traditional RFET architecture. Our 3-D TCAD simulations reveal that the proposed devices exhibit increased I_{ON}s at operational voltages below 1.0 V compared to previously studied RFETs. The robustness of the ECRFET against variability was assessed using RDF analysis. Additionally, We have developed a highly precise Verilog-A model based on our proposed device, which demonstrates its utility in complex circuit configurations, such as a 6T SRAM, and in calculating the SNM or minimum Vmin using SPICE-based simulations.

REFERENCES

[1] A. Heinzig, S. Slesazeck, F. Kreupl, T. Mikolajick, and W. M. Weber, "Reconfigurable silicon nanowire transistors," Nano Lett., vol. 12, no. 1, pp. 119–124, 2012.

[2] J. Ahn, S. Satapathy, and J. P. Kulkarni, "Advancing Low-Voltage Complementary Reconfigurable Field-Effect Transistor Operation with Reduced Schottky Barriers," in *Proc. IEEE Device Research Conference*, Maryland, USA, June 2024., in press.

[3] Synopsys Inc., *Sentaurus Device User Guide, Version S-2021.06-SP1*, Mountain View, CA, USA, June 2021.

[4] J. Trommer, A. Heinzig, S. Slesazeck, T. Mikolajick and W. M. Weber, "Elementary Aspects for Circuit Implementation of Reconfigurable Nanowire Transistors," *IEEE Electron Device Lett.*, vol. 35, no. 1, pp. 141-143, Jan. 2014.

[5] J. -K. Kim, S. -H. Kim, T. Kim, and H. -Y. Yu, "Universal Metal–Interlayer–Semiconductor Contact Modeling Considering Interface-State Effect on Contact Resistivity Degradation," *IEEE Trans. Electron Devices*, vol. 65, no. 11, pp. 4982-4987, Nov. 2018.

[6] G. Gore, P. Cadareanu, E. Giacomin, and P. -E. Gaillardon, "A Predictive Process Design Kit for Three-Independent-Gate Field-Effect Transistors," in *Proc. 2019 IFIP/IEEE 27th International Conference on Very Large Scale Integration (VLSI-SoC)*, 2019.

[7] R. Zhang *et al.*, "Novel 3-D Fin-RFET With Dual-Doped Source/Drain to Improve ON-State Current," *IEEE Trans. Electron Devices*, vol. 69, no. 12, pp. 6569-6575, Dec. 2022.

[8] S. Satapathy, W. H. Choi, X. Wang and C. H. Kim, "A revolving reference odometer circuit for BTI-induced frequency fluctuation measurements under fast DVFS transients," 2015 IEEE International Reliability Physics Symposium, Monterey, CA, USA, 2015.

[9] A. Ghosh, S. Satapathy, J. P. Kulkarni and P. D. Joshi, "Aging Effects On Clock Gated Memory Phase Paths," 2022 IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT), Austin, TX, USA, 2022.

[10] T. Mikolajick, A. Heinzig, J. Trommer, T. Baldauf, and W. M. Weber, "The RFET—A reconfigurable nanowire transistor and its application to novel electronic circuits and systems," Semicond. Sci. Technol., vol. 32, no. 4, Apr. 2017, Art. no. 043001.

[11] A. Heinzig, T. Mikolajick, J. Trommer, D. Grimm, and W. M. Weber, "Dually active silicon nanowire transistors and circuits with equal electron and hole transport," Nano Lett., vol. 13, pp. 4176–4181, Aug. 2013.

[12] T. Baldauf, A. Heinzig, J. Trommer, T. Mikolajick, and W. M. Weber, "Tuning the tunneling probability by mechanical stress in Schottky barrier based reconfigurable nanowire transistors," Solid-State Electron., vol. 128, pp. 148–154, Feb. 2017.

[13] X. Li, Y. Sun, X. Li, Y. Shi, and Z. Liu, "Electronic assessment of novel arch-shaped asymmetrical reconfigurable field-effect transistor," IEEE Trans. Electron Devices, vol. 67, no. 99, pp. 1–8, May 2020.

[14] M. D. Marchi et al., "Polarity control in double-gate, gate-all-around vertically stacked silicon nanowire FETs," in IEDM Tech. Dig., San Francisco, CA, USA, Dec. 2012, p. 8, doi: 10.1109/IEDM.2012.6479004.

[15] W. Ni, Z. Dong, B. Huang, Y. Zhang, and Z. Chen, "A physicbased explicit compact model for reconfigurable field-effect transistor," IEEE Access, vol. 9, pp. 46709-46716, 2021.

[16] J. Trommer, A. Heinzig, S. Slesazeck, T. Mikolajick, and W. M. Weber, "Elementary aspects for circuit implementation of reconfigurable nanowire transistors," IEEE Electron Device Lett., vol. 35, no. 1, pp. 141–143, Jan. 2014.