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Novel Mobility Enhancement Schemes for Next Generation Silicon Carbide (SiC) Trench MOSFET Technology

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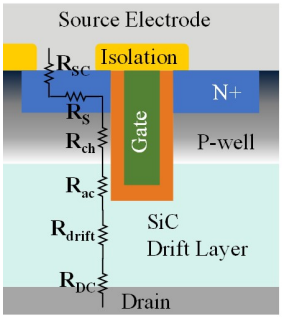
***Abstract*—New mobility improvement solutions are proposed for next generation SiC trench MOSFET with higher aspect ratio trenches. A combination of channel counter-implant and pocket implant is shown to be most effective for improving mobility without V_T loss. Using our proposed integration scheme and calibrated modeling, we project an 80% improvement in mobility and 40% improvement in channel resistance, realizing the true potential of trench MOSFET architecture for next generation SiC power device technology.**

***Index Terms*—SiC, Mobility, Implants, Power, MOSFET, circuit design, device modeling, process modeling.**

Resistance Components of SiC Trench MOSFET



Resistance Component	Definition
R_{SC}	Source contact Resistance
R_S	Source Resistance
R_{ch}	Channel Resistance
R_{ac}	Spreading Resistance
R_{Drift}	Drift resistance
R_{DC}	Drain contact Resistance

Fig. 1. Resistance (R_{DSon}) components of SiC trench MOSFET. The channel resistance (R_{ch}), being 60-70% of total R_{DSon} is the major resistance component.

I. Introduction

Silicon carbide (SiC) trench MOSFETs [1]–[3] are expected to gradually replace the traditional planar SiC technology for advanced power switching device applications due to lower on-resistance (R_{ON}). Higher electron mobility in the vertical direction of the channel further adds to the performance benefit. The aspect ratio of the trench is projected to increase for the next generations of SiC trench MOSFETs. R_{DSon} scaling requirement with each new generation of SiC technology calls for scalable mobility and drive-current improvement techniques. Fig. 1 shows the different components of resistance (R_{DSon}) for SiC trench MOSFET. The channel resistance (R_{ch}) is the dominant component, being 60-70% of the total R_{DSon} [4]. Thus, channel mobility improvement has been shown to be the key path forward to reduce R_{DSon} for next generations of SiC MOSFET technology. In this paper, we propose novel device design schemes for mobility improvement and project their impact on SiC transistor performance through our calibrated SiC modeling platform [5]–[8].

SiC Lateral MOSFET Electrical Characterization Test Vehicle

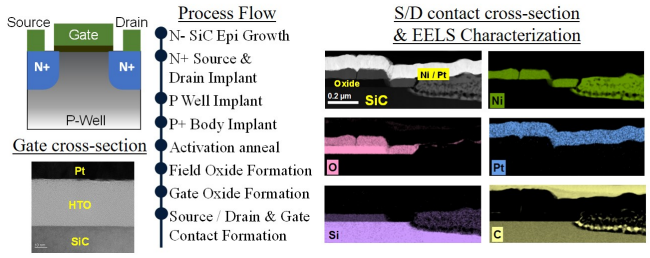


Fig. 2. Lateral SiC MOSFET test vehicle for novel HTO gate-oxide and advanced mobility enhancement schemes & channel resistance (R_{ch}) characterization.

SiC MOSFET Mobility Improvement Scheme: Channel Counter-Doping (Modeling-based Projection)

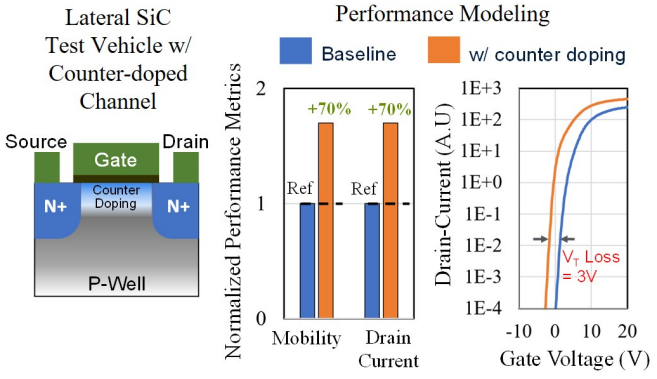


Fig. 3. Counter-doping the SiC channel leads to 70% mobility and drive-current improvement (modeling). However, it also leads to undesirable 3 V V_T loss.

Optimization of Channel Counter-doping & Experimental Demonstration

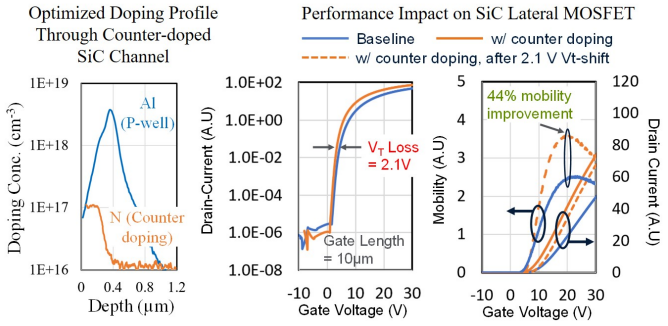


Fig. 4. Experimental demonstration of SiC mobility & drive-current enhancement by using nitrogen (n-type) counter-doping in channel.

II. Experiment Setup and Modeling Platform

To characterize channel mobility impact with our proposed device design schemes, we have developed a lateral SiC MOSFET test vehicle (Fig. 2). In conjunction, we have also developed an advanced SiC transistor modeling platform for technology exploration and performance projection. Our drift-diffusion based modeling platform is closely calibrated to the test vehicle highlighted in Fig. 2.

III. Channel Counter-Doping - SiC MOSFET Channel Mobility Improvement

Despite high bulk mobility ($\sim$1000 cm^2/$V.s$) [9], SiC MOSFET transistors have been demonstrated only with 10 - 40 cm^2/$V.s$ channel mobility [10]–[12]. The low channel mobility has been attributed to high interface density near band-edges [13], [14] and coulomb scattering from trapped electrons due to the formation of carbon-clusters and degradation of surface roughness during the dopant activation (greater than 1650°C) and thermal gate-oxidation process. The impact of interface states and surface roughness can be partially mitigated by creating the channel away from the surface (buried channel) using a high n-type channel doping (counter doping) in conjunction with a low p-well doping ($\sim$1e15 – 1e16 cm^{-3}) [13], [15], [16]. However, besides higher channel mobility, this approach also results in a threshold voltage (V_T) loss, thus unusable for practical application. Our modeling shows that n-type channel counter-doping (1e17 cm^{-3}) can be used with a high p-well doping ($\sim$2e18 cm^{-3}) for mobility and drive-current improvement (Fig. 3). However, this also results in very low threshold voltage (V_T), problematic for practical application. With the help of our modeling platform, we have optimized the counter-doping using nitrogen implant, while using a comparatively higher p-type well doping (aluminum 1e18 cm^{-3}, Fig. 4) to keep the V_T loss under control. 47% drive-current and mobility improvement (at constant over-drive $V_{OV} = V_G - V_T$) is achieved with 2.1 V V_T loss (Fig. 4) using our test vehicle. The trade-off between V_T loss and drive-current improvement (Fig. 5(a)), obtained by varying

V_T Loss & Drive-current Improvement with Channel Counter Doping

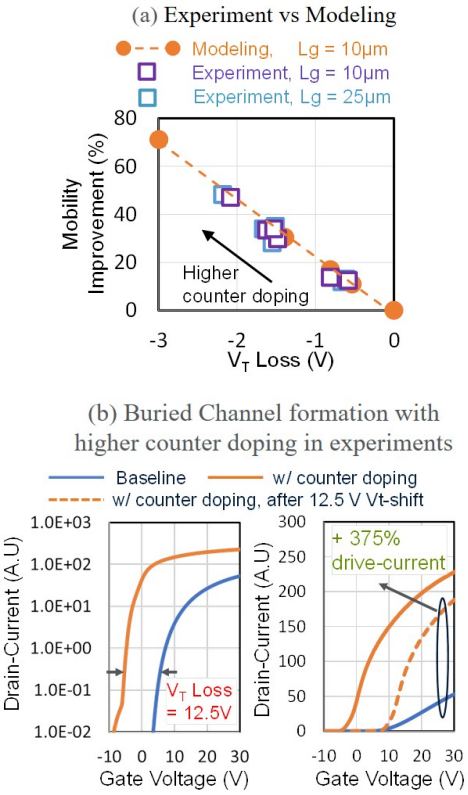


Fig. 5. (a) Trend of V_T loss & mobility improvement for different channel counter-doping (6e16 - 5e17 cm^{-3}) in experiments, matching with process & device modeling. 70% mobility & current gain can be achieved with counter doping at the cost of 3 V V_T loss. Figure 11(b) Higher channel counter doping leads to formation of buried channel with higher mobility & drive-current (375%) gain, but simultaneously very high V_T loss (12.5 V).

the counter-doping implant dose experimentally shows a linear trend, closely aligned with our calibrated SiC modeling framework [5]. A higher counter-doping (Fig. 4(b)) leads to buried channel formation, very high drive-current (375%) and mobility improvement, typically reported in literature [15]. But it simultaneously results in very high un-recoverable V_T loss (12 V) and therefore is not suitable for practical applications.

IV. Recessed Counter-Doping and Pocket Implants - Threshold Voltage Recovery

For proper industry adoption of counter-doping in SiC power devices, we propose two different V_T recovery schemes and use our calibrated modeling framework to characterize those. Figure 6 summarizes the first scheme: recessed counter-doping to keep the counter-doping implant away from the source/channel and the drain/channel junction. This allows for a short region of net p-type doping in between the counter-doped channel and source/drain Epi. The idea is to introduce potential barriers along the path of the electron to recover the V_T loss introduced by channel counter-doping. With this scheme, the V_T loss can be reduced to less than 1 V (from 3

V_T Recovery Scheme I: Recessed Counter Doping & Projected Performance Impact

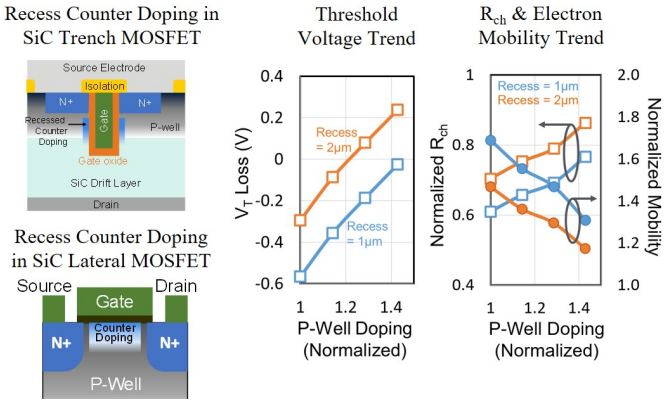


Fig. 6. Proposed recessed channel counter-doping scheme to recover V_T loss associated with channel counter-doping. Co-optimization of recess with p-well doping is required for full recovery of V_T loss in SiC lateral MOSFET. V_T recovery with this scheme brings down R_{ch} improvement from 35% to 23%.

V_T Recovery Scheme II : Pocket Implant (Modeling-based Analysis)

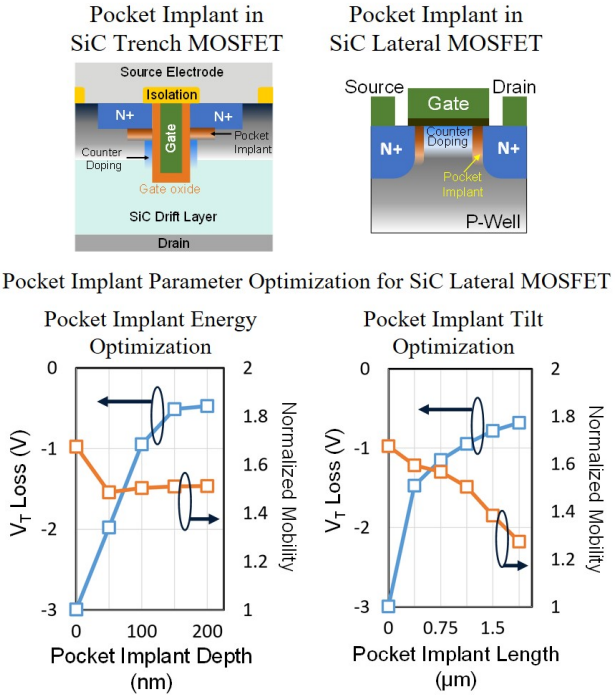


Fig. 7. Proposed p-type pocket-implant scheme to recover V_T loss associated with counter doping (top). The pocket-implant can be designed to achieve the target doping profile, namely, the implant depth & length for SiC lateral MOSFET (bottom).

V for the case of without laterally recessed counter-doping). Further V_T loss reduction can be achieved by increasing the p-well doping (Fig. 6). However, the increase in p-well doping leads to an increase in channel resistance and decrease in electron mobility. Our modeling (Fig. 6) shows that a V_T-neutral channel resistance improvement of 23% and electron

Modeling of V_T Recovery with Pocket Implant Dose in SiC Lateral MOSFET

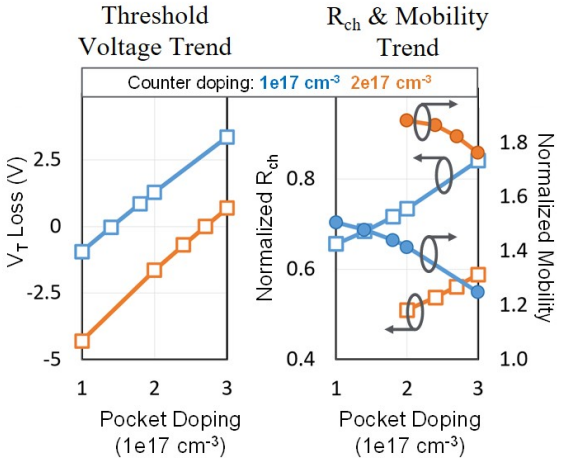
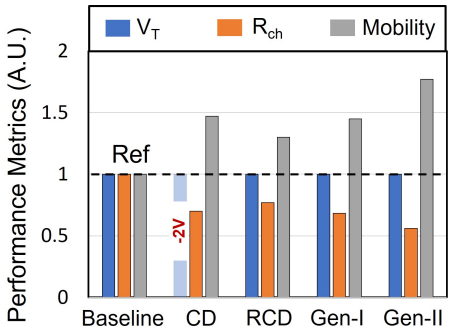


Fig. 8. Pocket implant optimization can lead to R_{DSon} improvement with full V_T recovery.

mobility improvement of 30% can be achieved by optimizing the counter-doping lateral recess and p-well doping.

Figure 7 proposes the second scheme to recover the V_T loss associated with channel counter-doping: introduction of p-type pocket implants. The working principle is identical to the recessed counter-doping design. However, instead of recessing the counter-doping, p-type regions are explicitly introduced between the counter-doped channel and the source/drain Epi through p-type ion implants. Using a proper combination of pocket implant process parameters (energy and tilt for SiC lateral MOSFET), the pocket implant can be placed

Comparison of SiC MOSFET Performance Improvement Schemes



Baseline	w/o Channel Counter-doping
CD	Channel Counter-Doping
RCD	Recessed Counter-Doping
Gen-I	Counter-doping + optimized pocket implant
Gen-II	Higher Counter-doping + Optimized pocket implant

Fig. 9. Summary of the different performance improvement schemes. Pocket implant with counter-doping provides the lowest channel resistance without V_T loss

at the source/channel and drain/channel junction, leading to reduction of V_T loss (Fig. 7). By controlling the pocket-doping concentration (1e17 - 3e17 cm^{-3}), the V_T loss can be fully recovered, even for a higher counter-doping (Fig. 8), leading to the possibility of achieving a high drive-current improvement (77%) without any V_T loss. Thus, the pocket implant together with counter doping, provides a scalable technique for mobility improvement which is critical for enabling node-to-node scaling of SiC technology. Figure 4 summarizes the different schemes of mobility improvement indicating that the combination of counter-doping and pocket implant to be the most promising. Based on the projection from our calibrated modeling, we can achieve an $\sim$80% mobility enhancement and $\sim$40% channel resistance reduction without any V_T loss by optimizing the counter-doping and pocket implant together.

V. Conclusion

In this paper, we have proposed novel device design schemes based on the use of channel counter-doping to improve SiC MOSFET hole mobility and resistance. Utilizing our advanced and calibrated SiC modeling platform, we project that our proposed integration flow of using channel counter-doping with a pocket implant for V_T recovery can provide 80% and 40% mobility and channel resistance improvement, respectively, thereby realizing the true potential of the trench MOSFET architecture for next-generation SiC power device technology.

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