Modeling Row Hammer Effect in 3D Capacitor-less DRAM using Triple-Gated Silicon Nanosheet Device

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***Abstract*— A monolithically stackable 3D capacitor-less DRAM structure using triple-gated silicon nanosheet device is demonstrated using TCAD simulation. Our proposed device exhibits a low programming voltage of 1.8 V, a high current sense margin of 78 µA, a fast speed of 5 ns and a data retention time of more than 10^4 s. In addition, we evaluate the row hammer effect on the 3D array level, including program, erase, read, and hold operations. The simulation results show a robust storage node potential despite repeated attack operations from the neighboring cell.**

Keywords—3D stackable DRAM, row hammer effect, retention time, capacitor-less DRAM, feedback mechanism.

I. Introduction

The conventional one-transistor-one-capacitor (1T-1C) dynamic random-access memory (DRAM) has faced challenges in reducing memory cell size within the sub-10 nm technology node due to ultra-high aspect ratio capacitor, increasing leakage currents and capacitive coupling induced row-hammer effect [1-2]. Hence, three-dimensional (3D) stackable DRAM emerges as one of the promising solutions for continuing DRAM scaling such as 3D 1T-1C DRAM and IGZO based 2T0C DRAM [3-5]. However, 3D 1T-1C DRAM with vertical BL or WL, requires the horizontal capacitor that occupy a large footprint. While IGZO based 2T0C DRAM offers advantages such as compact cell size and improved retention, it lacks a bit-cost-effective 3D stacking fabrication process. Recently, the thyristor-based 3D stackable capacitor-less DRAM has been proposed by the industry [4], with experimentally validated performance. In this paper, we further optimize such triple-gated silicon nanosheet device that aims to reduce programming voltage to 1.8 V and improved retention time to 10^4 s. Especially, we demonstrate that the optimized triple-gated silicon nanosheet device can reduce the band-to-band tunneling (BTBT) rate, which aggravates the retention time in the device, by lengthening the distance between the drain and the gate electrode. For the first time, row hammer effect is evaluated in such 3D stackable DRAM. It is well known that the row hammer effect has been a security vulnerability in the conventional 2D DRAM.

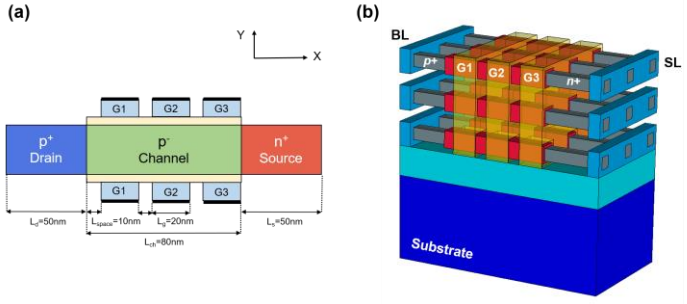
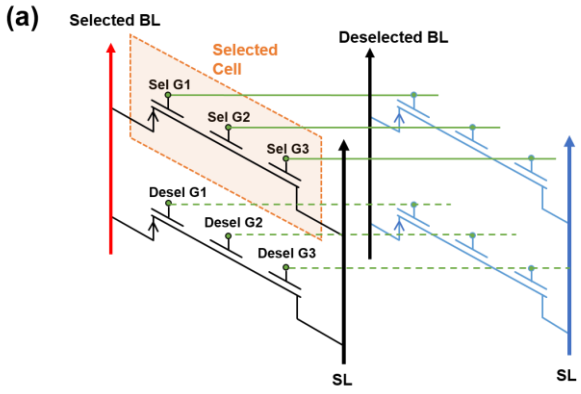


Fig. 1(a) Cross-sectional view and (b) 3D view of triple-gated silicon nanosheet devices in a 3D stackable DRAM array.

TABLE I. SIMULATION PARAMETERS

Name	Unit
Channel length (L_{ch})	80 nm
Space length (L_{space})	10 nm
Gate length (L_g)	20 nm
Drain length (L_d)	50 nm
Source length (L_s)	50 nm
Oxide thickness, HfO_2 (t_{OX})	2 nm
Channel doping concentration	10^{15} cm^{-2}
Source/drain doping concentration	10^{20} cm^{-2}
Gate work function	4.5 eV
Storage capacitor (1T-1C DRAM)	25 fF



(b)

Voltage(V)	PGM	ERS	Read	Hold
Sel G1	1.0	0.0	1.0	1.0
Sel G2	1.0	0.0	-1.0	-1.0
Sel G3	-1.0	0.0	-1.0	-1.8
Sel BL	1.8	0.0	1.2	0.0
Desel G1	1.8	1.8	1.8	1.0
Desel G2	-1.8	-1.8	-1.8	-1.0
Desel G3	-1.8	-1.8	-1.8	-1.8
Desel BL	1.0	0.0	1.0	0.0
SN	0.0	0.0	0.0	0.0

Fig. 2 (a) Schematic and (b) bias scheme of 3D capacitor-less DRAM array consisting of triple-gated silicon nanosheet devices.

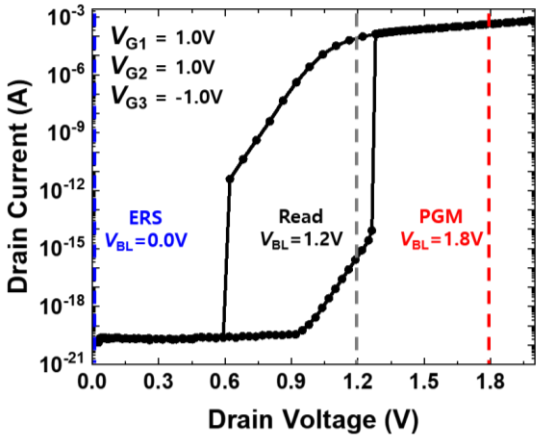


Fig. 3 I_D-V_D output characteristics of triple-gated silicon nanosheet device for program/erase/read operations.

II. Device Structure and Simulation Method

Fig. 1(a) shows the schematic design of optimized triple gated silicon nanosheet device. The structural and dimensional parameters utilized in this paper are summarized in Table I. Each gate length (L_g) and space length (L_{space}) is 20 nm and 10 nm, respectively. Also, the gate1 (G1) electrode is positioned 10 nm away from the drain region to prevent the BTBT rate from the drain side. The 3D stackable array architecture (3×3×3 cells) of triple-gated silicon nanosheet devices have been constructed using TCAD simulations, as shown in **Fig. 1(b).** To prevent disturbances, with adjacent cells, we investigate array-level bias scheme **(see Fig.2(a))**. The deselected cell's state is maintained during selected cell's operation including program, erase, read,

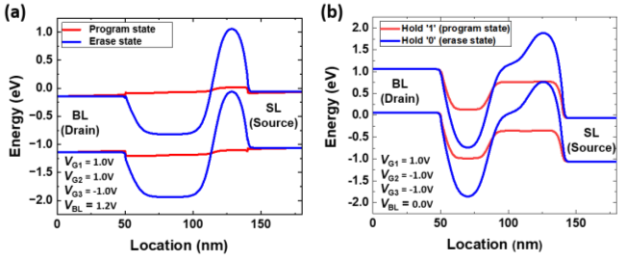


Fig. 4 Energy band diagram of proposed capacitor-less DRAM (a) under read operation for both PGM and ERS states, and (b) under hold '1' and '0' states, showing the feedback mechanism.

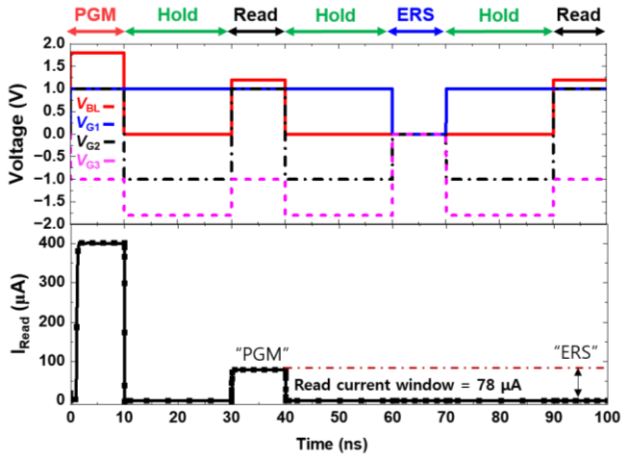


Fig. 5 Simulated timing diagram of the proposed capacitor-less DRAM cell operation including programming, erasing, read, and hold operations.

and hold operations. The deselected cell is divided into bit-line (BL)-shared cells and word line (WL)-shared cells. The selected gate 1 (Sel G1), selected gate2 (Sel G2), selected gate3 (Sel G3), and selected BL voltages are applied to the selected cell in each operation including program, erase, read, and hold state, as shown in **Fig.2(b).** On the other hand, to maintain the data in the unselected cell, the BL-shared deselected cells and the WL-shared deselected cells are applied to different voltage to the BL and WL, as listed in **Fig. 2(b).** We verify all disturb cases on half-selected cells of our proposed device. Device simulations are carried out using Synopsys Sentaurus with a non-local BTBT model, Shockley-Read-Hall recombination model, bandgap narrowing model, and doping dependence mobility model [6]. In addition, conventional buried channel array transistor (BCAT) 1T-1C 2D DRAM (1α node) simulation is conducted using mixed-mode simulation as the baseline. For the conventional BCAT MOSFET, a gate length of 10 nm was utilized, and a storage capacitance of 25 fF was used.

III. Result and Discussion

A. Cell-Level Characteristics of 3D DRAM

The operation of triple-gated silicon nanosheet device is based on the positive feedback mechanism [7, 8]. **Fig. 3** shows the output characteristics of the device. When the drain voltage (BL) is increased from 0.0 V to 2.0 V (with V_{G1} = V_{G2} = 1.0 V, and V_{G3} = -1.0 V), the valance band in the drain region is lowered, allowing holes to be injected into the potential well within gated

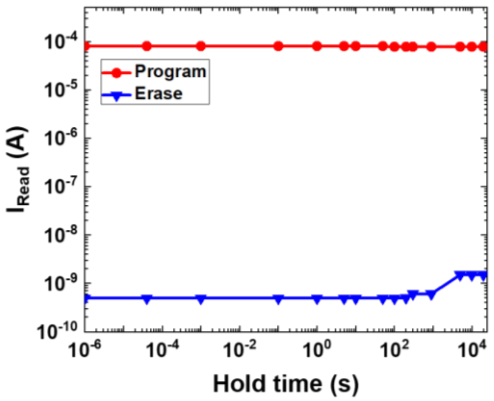


Fig.6 Retention characteristics of proposed capacitor-less DRAM cell.

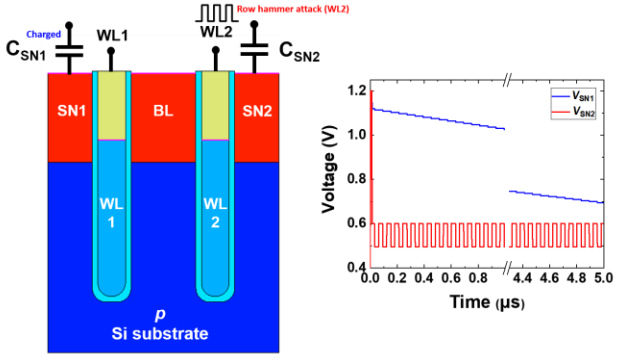


Fig. 7 (a) 2D cross-sectional view of 1T-1C BCAT structure. (b) Potential waveform of SN1 capacitor, induced by switching aggressor WL2, showing rapid decay with less than 5 μs retention time.

channel region. Simultaneously, electrons from the conduction band of the source region are injected, resulting in a rapid increase in the drain current (I_D) at a drain voltage of 1.3 V; this is defined as the latch-up voltage, due to the creation of a positive feedback loop. As the drain voltage is swept back from 2.0 V to its initial values, the drain current decreases rapidly at a drain voltage of 0.6 V, referred to as the latch-down voltage. The latch-down phenomenon results from the elimination of the positive feedback loop. Here, the latch-up voltage differs from the latch-down voltage due to charge accumulation in the channel region [8]. Thus, based on the I_D-V_D output characteristics of the device, we determine the program, erase, and read voltages, as shown in **Fig. 3**. The read voltage is set between the latch-up and latch-down voltages to measure the drain current in each state. **Fig. 4(a)** presents the energy band diagrams during read operation for both the programmed (PGM) and erased (ERS) states. After programming, the device transitions into the PGM state. When the read voltage is applied to the BL, drain current (I_{read}) flows due to the breakdown of the potential barrier, as depicted in **Fig. 4(a)**. Conversely, following the erase operation, the device enters the ERS state, where only low leakage current (I_{read}) flows during the read operation due to the presence of a potential barrier. **Fig. 4(b)** illustrates the energy band diagrams of the hold operation in both the PGM and ERS states. **Fig. 5** presents the simulated timing diagram of the cell memory operation, including program, erase, read, and hold

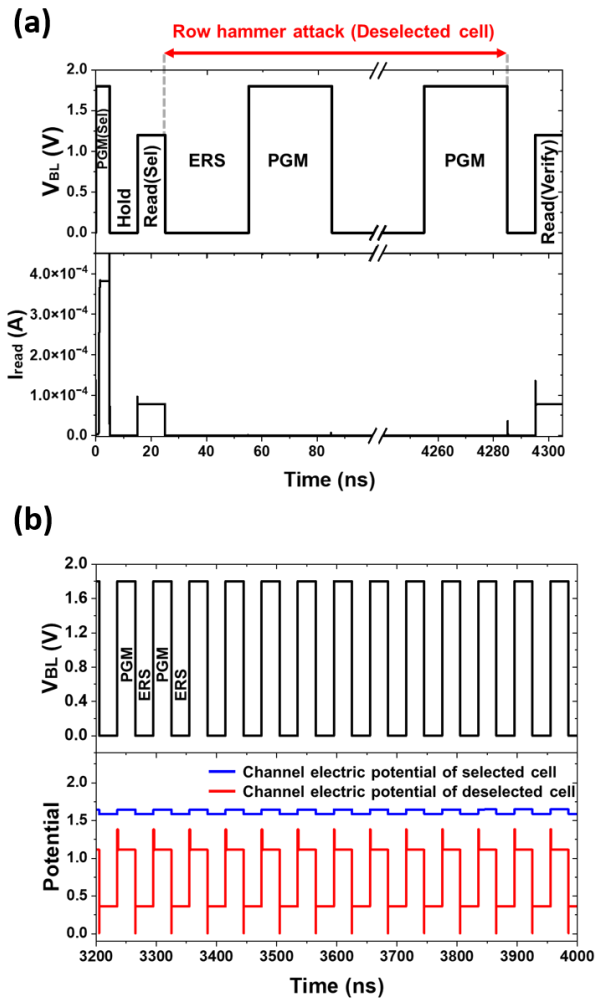


Fig. 8 Timing diagram of row hammer effect simulation for 3D stackable capacitor-less DRAM in array operation. (a) The selected cell (being attacked)'s PGM state can be read by I_{read} after row hammer attack from the deselected cell. (b) Simulated timing diagram shows that potential of channel in selected cell (PGM state) is successfully maintained during adjacent deselected cell's attack.

operations. The program, erase, and read operations were sequentially performed with a pulse width of 10 ns. To program the cell, a V_{BL} of 1.8 V and a V_{WL} (V_{G1}, V_{G2}, V_{G3}) were applied, which induced a positive feedback loop in the channel. Subsequently, the hold operation with a pulse width of 20 ns was executed, featuring low leakage current of 2 nA. Then, the read pulse of V_{BL} = 1.3 V reactivated the positive feedback loop in the channel with I_{read} reached 78 μA, indicating PGM state. The erase pulse of V_{BL}=0 eliminated the positive feedback loop in the channel. Following the erase and subsequent hold operations, the I_{read} was negligible during the read operation in the ERS state. **Fig. 6** shows the retention characteristics of proposed capacitor-less DRAM cell. As the hold time increases from 10 ns to 10^4 s in the unit cell, each programmed and erased state exhibits a data retention time of more than 10^4 s. Therefore, without the storage capacitor, each state is maintained within the device through potential barrier, enhancing retention time characteristics.

B. ARRAY-LEVEL CHARACTERISTICS OF 3D DRAM

Fig. 7 and **Fig. 8** compare the row hammer effect in BCAT 1T-1C 2D DRAM and our proposed triple gated silicon nanosheet device. The row hammer effects occur due to the electrical interference caused by frequent activation and deactivation of the aggressor cell, leading to unintended charge leakage in the adjacent cells. As a result, the stored data in the adjacent cells may become corrupted, reducing the significant data retention time of deterioration [9]. As the SN1 capacitor is charged **(**refer to **Fig. 7(a)),** the aggressor WL2 of the adjacent cell repeatedly performs the row hammer attack for 75 cycles of aggressor WL2 switching, as shown in **Fig. 7(b)**. With each repetition of the WL2 switching cycle, V_{SN1} keeps dropping from its initial charged value, resulting in rapid degradation of data retention time to less than 5 μs.

Fig. 8 demonstrates the mitigated row hammer effect in our proposed capacitor-less DRAM array operation with 75 cycles of aggressor switching from an adjacent cell. The selected cell's state may fluctuate by the operation of deselected cell, which is one of the BL-shared cells; program and erase cycles are repeatedly applied by the deselected cell for 75 cycles (see **Fig. 8(b)**). Therefore, our proposed capacitor-less DRAM array successfully maintains the selected cell's state with robust data conservation properties despite the row hammer.

IV. CONCLUSION

In this paper, our purposed device demonstrates superior memory characteristics, including a high current sense margin of 78 μA, a low operating voltage of less than <1.8 V, a long retention time of 10^4 s, and a mitigated row hammer effect. Therefore, the triple-gated silicon nanosheet device has a great potential for next-generation 3D stackable DRAM.

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