Modeling of SOI-MOSFET with Trap-Rich Substrate for RF Circuit Design

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2024 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD) | 979-8-3315-1635-2/24/$31.00 ©2024 IEEE | DOI: 10.1109/SISPAD62626.2024.10732954

***Abstract*— Many efforts have been undertaken to reduce the substrate-coupling effect in RF circuits. It has been demonstrated that a trap-rich layer underneath the BOX can reduce drastically undesired harmonic distortions (HDs), thus maintaining desired signal integrity. To utilize this technology, a newly developed compact model considers the trap charge based on its physics and is implemented into HiSIM_SOI, which solves the whole potential distribution within the device iteratively. The Fermi energy modeling as a function of trap density (Ntrap) is one of the keys for the achieved consistent modeling. It is also demonstrated that the trap charge improves the linearity of the induced potential characteristics during device operation, resulting in a HD reduction.**

Keywords—SOI-MOSFET, RF applications, compact model, trap-rich Poly-Si layer, substrate coupling, Harmonic Distortion, Fermi energy, Poisson equation

I. Introduction

Low-power and good high-frequency characteristics are a prerequisite for devices applied in advanced RF-circuit generations. To maintain small HDs is inevitable as well. For realization of all these requirements, ETSOI with a trap-rich Poly-Si layer in the substrate has been utilized [1, 2], demonstrating a reduction of HDs by more than 30 dB (see Fig. 1b). Detailed investigation of the trap influence on device characteristics has been done with use of simulation technique [3, 4].

To profitably exploit this new development in circuit design, the used compact model has to reproduce the improved device characteristics based on their origin, which is our aim and focus in the reported research.

The CMC-standard compact model HiSIM_SOI solves the Poisson equation along the device depth direction iteratively by considering all possible charges induced within the device [5]. Here, the trap charge N_{trap} is additionally included in the Poisson equation to model the trap effect physically correct and accurately. The model considers both the floating-body and the body-tie structures under dynamically varying depletion condition so that the model can be applicable for any type of structures.

II. Compact Modeling for Advanced RF Circuits

Fig. 1 shows the studied device structure and the corresponding HDs, obtained by numerical TCAD simulation in 2D/3D with/without the trap charge. Two types of the structure have been developed after applications. One is the floating-body (FB) structure without the V_b node, and the other is the body-tie (BT) structure with the node, where the latter is mostly selected for the RF applications. Our investigation has been done mostly for the BT structures. Because the V_b node loses its influence once the SOI layer becomes fully depleted, and the potential distribution is immediately connected to the substrate. The trap charge is located underneath the relative thick BOX.

HiSIM_SOI solves the Poisson equation from the gate contact V_{gs} to the substrate-bottom contact V_{es} together with boundary conditions as schematically demonstrated in Fig. 2 [6]. All charges are a function of three surface-potential values ϕ_s, ϕ_b, and ϕ_{bulk}. For the thin BOX structure, additional non-smooth potential distribution within the SOI layer must be considered [7]. However, the studied technology applies relative thick BOX, and no potential non-smoothness can occur. The model fulfills following features, which are a prerequisite for the RF circuit design:

- Dynamic switching between partially depleted and fully depleted conditions
- Validity for both floating-body and body-tie structures
- Gate-control extension to substrate, even in a body-tie structure under fully depleted condition
- Accurate higher-order derivatives of all potential values as a function of applied biases

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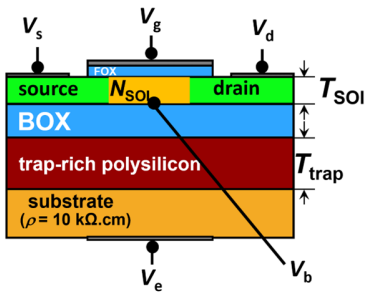

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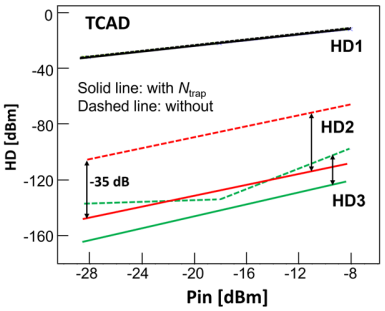


Fig. 1. (a) Structural schematic of a trap-rich SOI MOSFET, and (b) HD characteristics under investigation simulated with TCAD.

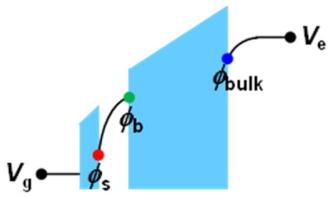


Fig. 2. Schematic of band diagram showing the three surface potentials. The distribution is dependent on bias conditions, as well as structural geometry.

The model extension includes following main feature:

- Explicit trap-charge inclusion in the Poisson equation

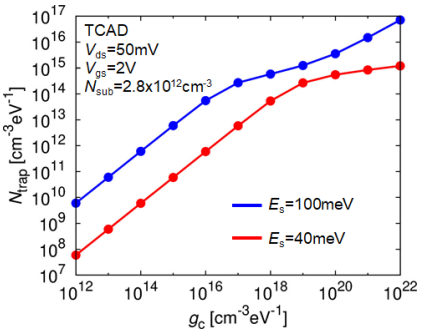
Here, an important task in compact modeling for the studied device is to capture the trap characteristics based on its physics, so that the trap role for the device characteristics is accurately modeled as a function of applied bias conditions. By approximating the trap energy to be mostly located at the Fermi energy, the trap density N_{trap} is written as [8, 10]

$$N_{\mathrm{trap}} = N_0 \exp\left(\frac{E_\mathrm{f} - E_\mathrm{c}}{E_\mathrm{s}}\right) \quad (1)$$

$$N_0 = g_\mathrm{c} E_\mathrm{s} \frac{\frac{kT}{E_\mathrm{s}}}{\sin\left(\frac{kT}{E_\mathrm{s}}\right)} \quad (2)$$

after integrating the equation with respect to energy E. Here g_c and E_s are model parameters describing the magnitude of N_{trap} and that of gradient within the bandgap, respectively. Thus, N_{trap} is a function of E_c-E_f, where the Fermi energy E_f varies according to N_{trap} as well as bias conditions. N_{trap} increases are accompanied by E_f reductions. Fig. 3 shows TCAD simulation results [7] as a function of g_c, where g_c is a model parameter determining N_{trap} magnitude. When g_c reaches $1x10^{18}$ cm^{-3} eV^{-1}, N_{trap} starts to saturate due to the reduction of E_f as shown in Fig. 4. The Fermi energy E_f is a function of ϕ_{bulk} under the non-equilibrium condition, which is again a function of N_{trap}. Thus, the total potential distribution within the device varies according to trap density and bias condition. This implicit feature of the model equations is hardly solvable in the compact-modeling framework. Therefore, simplifications are required to avoid a

(a)



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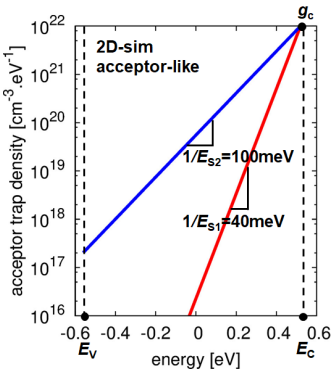

Fig. 3. (a) N_{trap} as a function of g_c for different E_s values (E_{s1}=40meV, red curve; E_{s2}=100meV, red curve), where g_c is a model parameter (see Eq. 2). (b) Schematic of acceptor like trap density distribution for different characteristics decay energy E_s. $1/E_s$ denotes rate of reduction of trap density from conduction band edge to valance band.

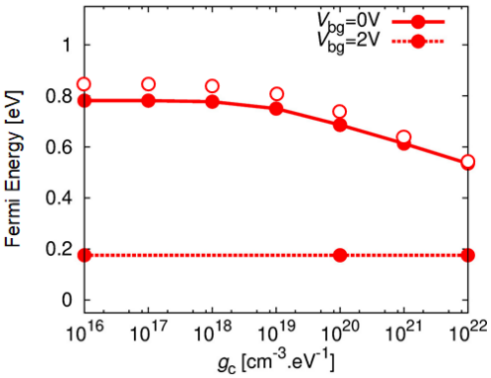

Fig. 4. Calculated Fermi energy as a function of g_c, describing the magnitude of N_{trap}. Open circles are results with TCAD and solid circles are those with HiSIM. Increased g_c causes E_f reduction to the midgap.

huge iterative simulation load. Another model parameter E_s describing the gradient of trap density within the bandgap is fixed to 40meV given in [1]. If E_s=100 meV, N_{trap} would start to increase further beyond g_c=1x10^{18} cm^{-3}eV^{-1} by the hole accumulation. One simplification is the minimum E_f value, set to be that of E_i at the maximum N_{trap}. As shown in Fig. 3, N_{trap} starts to approach to the saturation value. The reason for the saturation is the reduction of E_f approaching to the intrinsic Fermi energy, E_i. Further reduction then causes a donor-like trap-density increase, namely a positively charged trap-density increase. This results in larger HDs, which should be avoided for real applications, and can be ignored in compact modeling. Since de-trapping of trapped charge within Poly-Si is hardly observed, the trap-time constant is assumed to be infinitely long in comparison to circuit-operation time, namely E_f is pinned [9]. The Poisson equation, together with the Gauss law, derives the V_{gs} dependency of the total charge induced within the semiconductor as:

$$V_{gs} - V_{fb} - \phi_s = -\frac{Q_s + Q_b + Q_{dep} + Q_{bulk} + Q_{trap}}{C_{FOX}} \tag{3}$$

All charges are a function of the potential distribution along the device, characterized by three surface potential values ϕ_s, ϕ_b, and ϕ_{bulk} as depicted in Fig. 2. Since HDs are high-order derivatives of the drain current, they are determined by the carrier density and the velocity, which are again a function of the potential distribution. Therefore, accurate calculation of the

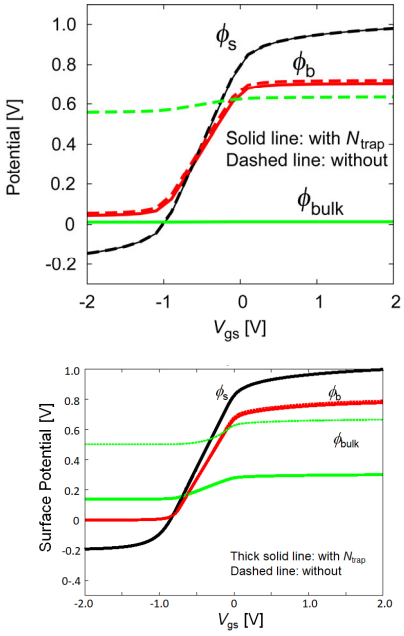

Fig. 5. Calculated three surface potential values as a function of V_{gs}, (a) obtained by TCAD and (b) HiSIM. In compact modelling, ϕ_s is chosen to zero at V_{gs}=V_{fb}, and the TCAD value was measured from the midgap level of intrinsic silicon. For easier comparison between them, the TCAD value is herewith shifted accordingly. It has to be noticed also that The deviation between two calculation results is due to no adjustment of HiSIM model parameters done, such as the built-in potential, the flat-band voltage, and N_{trap}.

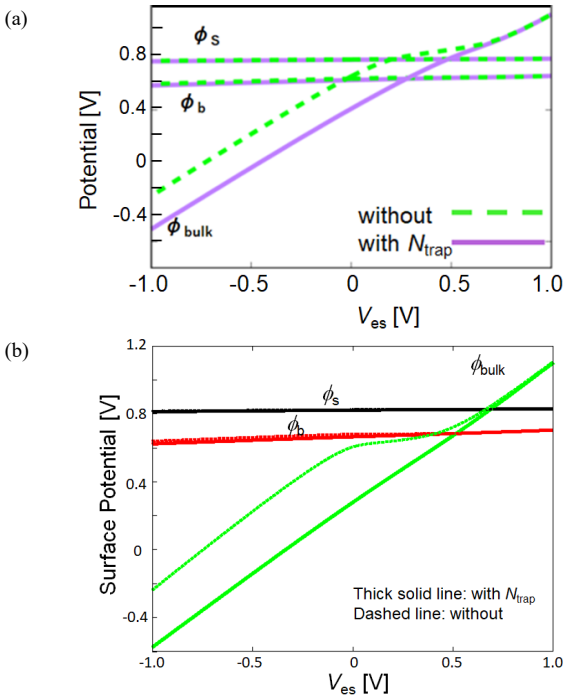

Fig. 6. Three surface potentials (ϕ_s, ϕ_b, and ϕ_{bulk}) as a function of the bulk voltage V_{es} at off-off state condition, namely at V_{gs}=0, (a) TCAD and (b) HiSIM. Solid lines are those with N_{trap} and dashed lines are without. The HiSIM built-in potential is not adjusted to that of TCAD, which might be the reason for ϕ_{bulk} shift.

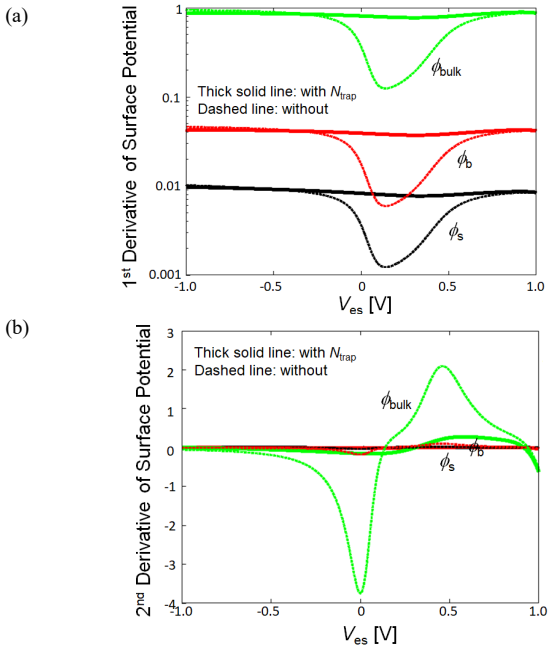

Fig. 7. Calculated of three surface potentials shown in Fig. 6 as a function of V_{es} at V_{gs}=0, (a) first derivatives and (b) second derivative of each potential with respect to V_{es}.

potential distribution is indispensable for accurate HD prediction. Obtained surface potentials are compared with those of TCAD results in Fig. 5.

III. Analysis of Trap Contribution for Device Characteristics

An evidence of HD improvement is depicted in Fig. 6 with and without N_{trap} as a function of V_{es}. Without Q_{trap}, ϕ_{bulk} shows a nonlinear feature as a function of V_{es}. It can be seen, that Q_{trap} improves the linearity of ϕ_{bulk}. The reason is that Q_{bulk} diminishes as Q_{trap} increases, the latter of which affects as a stable fixed charge. Fig. 7 depicts derivatives of the three potential values with respect to V_{es} with and without Q_{trap}. Signal propagation through the common substrate (bulk) leads to a fluctuation of the effective bulk potential. Fig. 6 depicts the fluctuation sensitivity. It can be seen that HD induced by the crosstalk comes from the reaction of Q_{bulk}, which is suppressed by Q_{trap} due to the diminishing of Q_{bulk}. To capture this feature is a modelling necessity. For this purpose, to calculate the accurate potential distribution by including Q_{trap} is a key modeling requirement. Calculated derivatives of three surface potentials-as a function of V_{gs} are shown in Fig. 8. The largest ϕ_{bulk} improvement is observed under the depletion condition, as can be expected. Calculated HD amplitude of different orders is depicted in Fig. 9 as a function of input amplitude.

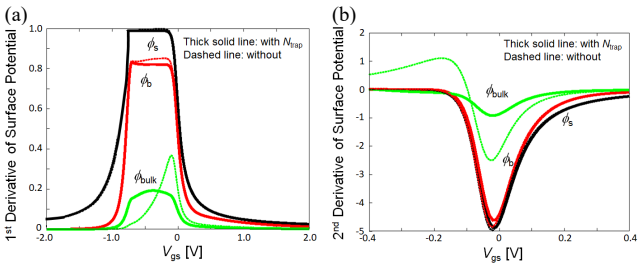

Fig. 8. Calculated derivatives of three surface potentials shown in Fig. 5 as a function of V_{gs}, (a) first derivative and (b) zoomed second derivative of each potential with respect to V_{gs}.

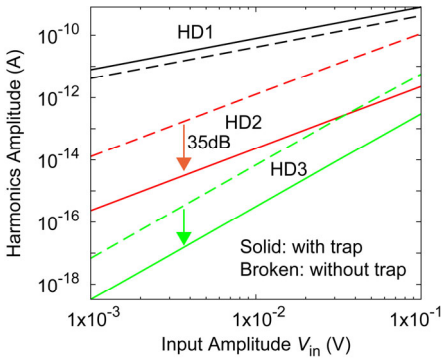

Fig. 9. Calculated HD amplitude with HiSIM under the off condition as a function of the small-signal amplitude, applied with and without N_{trap}. The axes are not converted to power, but original values are given. The horizontal axis is the small-signal amplitude, and the vertical axis is the amplitude of the drain current in different orders of derivative.

Improvements of HDs in the presence of Q_{trap} are successfully reproduced.

References

[1] B. Kazemi Esfeh, S. Makovejev, D. Basso, E. Desbonnets, V. Kilchytska, D. Flandre and J.-P. Raskin, "RF SOI CMOS technology on 1 st and 2 nd generation trap-rich high resistivity SOI wafers," *State Electronics*, vol. 128, pp. 121-128, Feb. 2017, doi: 10.1016/j.sse.2016.10.035.

[2] B. Kazemi Esfeh, M. Rack, S. Makovejev, F. Allibert and J.-P. Raskin, "A SPDT RF Switch small- and large-signal characteristics on TR-HR SOI substrates," *IEEE Journal of the Electron Devices Society*, vol. 6, pp. 543-550, 2018, doi: 10.1109/JEDS.2018.2805780.

[3] M. Rack and J. –P. Raskin, "Modeling of semiconductor substrates for RF applications: Part I—Static and dynamic physics of carrier and traps," *IEEE Transactions on Electron Devices*, vol. 68, no.9, pp. 4598-4605, Sept. 2021, doi: 10.1109/TED.2021.3096777.

[4] M. Rack, F. Allibert and J. P. Raskin, "Modeling of semiconductor substrates for RF applications: Part II—Parameter impact on harmonic distortion," in *IEEE Transactions on Electron Devices*, vol. 68, no. 9, pp. 4606-4613, Sept. 2021, doi: 10.1109/TED.2021.3096781.

[5] HiSIM_SOI User's Manual, Hiroshima University 2021.

[6] N. Sadachika, D. Kitamaru, Y. Uetsuji, D. Navarro, M. M. Yusoff, T. Ezaki, H.J. Mattausch, and M. Miura-Mattausch, "Completely surface-potential-based compact model of the fully-depleted SOI-MOSFET including short-channel effects," *IEEE Transactions on Electron Devices*, vol. 53, no. 9, pp. 2017-2024, Sept. 2006, doi: 10.1109/TED.2006.880366.

[7] M. Miura-Mattausch, U. Feldmann, Y. Fukunaga, M. Miyake, H. Kikuchihara, F. Ueno, H. J. Mattausch, T. Nakagawa, and N. Sugii, "Compact modeling of SOI MOSFETs with ultrathin silicon and BOX layers," *IEEE Transactions on Electron Devices*, vol. 61, no. 2, pp. 255-265, Feb. 2014, doi: 10.1109/TED.2013.2286206.

[8] T. Leroux, "Static and dynamic analysis of amorphous-silicon field-effect transistors," *Solid-State Electron*., vol. 29, no. 1, pp. 47-58, Jan. 1986, doi: 10.1016/0038-1101(86)90197-8.

[9] ATLAS User's Manual, SILVACO Inc.

[10] Y. Oodate, Y. Tanimoto, H. Tanoue, H. Kikuchihara, H. J. Mattausch, and M. Miura-Mattausch, "Compact modeling of the transient carrier trap/detrap characteristics in polysilicon TFTs," *IEEE Transactions on Electron Devices*, vol. 62, no. 3, pp. 862-868, Mar. 2015, doi: 10.1109/TED.2015.2388799.