Modeling Non-Uniformity During Two-Step Dry Etching of Si/SiGe Stacks for Gate-All-Around FETs

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Abstract—Selective lateral etching of the SiGe layers is one of the most critical steps in Gate-All-Around Field-Effect Transistor (GAAFET) fabrication, which is the basis for the formation of an inner-spacer. Non-uniformity of substrate surface during wet or dry selective etching of SiGe is a common sight in industry, which cannot be modeled using standard process Technology Computer Aided Design (TCAD) approaches. In this paper, we propose a method for the continuous simulation of the two-step dry etching process – anisotropic etching of the Si/SiGe stack and subsequent isotropic selective etching of SiGe – to study the mechanism behind the non-uniform profile formation. The proposed method is able to simulate the non-uniform profile accurately, which was calibrated and verified with experimental data.

Index Terms—GAAFET, SiGe Selective Etching, Non-Uniformity, Process TCAD

I. Introduction

As advanced-node semiconductor devices scaled down and more electrostatic control over the channel became essential, Gate-All-Around Field-Effect Transistor (GAAFET) became the go-to geometry to take over after Fin Field-Effect Transistor (FinFET) [1]. GAAFET devices achieve longer effective channels by providing access to multiple channel pathways and by introducing strain in the channel [2]. One of the most critical steps in GAAFET fabrication is the selective lateral etching of the SiGe layers, which is the basis for the formation of an inner-spacer [3].

The difficulty of selective SiGe etching is ensuring high control over the lateral depth and shape of the SiGe layer while minimizing Si layer loss [4]. Several studies show that there is a non-uniform profile on the substrate surface during wet or dry selective etching of SiGe, which cannot be modeled using standard process Technology Computer Aided Design (TCAD) approaches [5]–[7].

In this paper, we propose a method for the continuous simulation of the two-step dry etching process – anisotropic etching of the Si/SiGe stack and subsequent isotropic selective etching of SiGe – to study the mechanism behind the non-uniform profile formation. The proposed method is able to simulate

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the non-uniform profile accurately, which was calibrated and verified with experimental data.

II. MODELING FLOW

We devised a physical continuous two-step etching model for the generation of the Si/SiGe gate stack for GAAFETs. The model is then applied to investigate the non-uniform profile formation for the first time. The workflow consists of the following four critical steps, which are also depicted in Fig. 1.

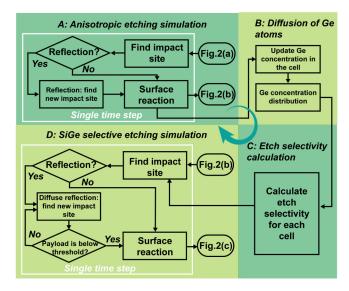


Fig. 1. Workflow of the physical model for the simulation of the continuous two-step etching process.

A. Anisotropic etching simulation

Anisotropic etching of the Si substrate in a Cl₂/Ar plasma is described in our previous work [8] and it includes the incident distribution of particles, Monte Carlo ray tracing, and profile evolution based on the cellular method. We apply this simulation method to anisotropic etching of Si/SiGe stacks.

Firstly, particles are incident from the top of the simulation domain. The incident site distribution of particles obeys a uniform distribution, which covers all plasma distribution areas. The model considers only two incident particles: chlorine neutral particle and argon ion. The ratio of Cl radical to Ar^+ is set to 10:1. The incidence angle distribution of argon ion follows Gaussian distribution and mean μ represents the center incident angle, which is normal to the substrate, while standard deviation σ represents the degree of the incident angle dispersion around the normal direction. In this study, μ is equal to 0 and σ is equal to 0.035, this corresponds to 99.7% of Ar^+ within $\pm 5.73^\circ$. The incidence angle distribution of Cl particle obeys the cosine distribution.

Once the particles enter the feature-scale region, their movement is governed by reflections from the wafer surface: the neutral radicals reflect diffusively, the ions reflect specularly as shown in Fig. 2(b). Since the entire simulation domain is divided into many cells, as shown in Fig. 3, each cell is assigned to a material, while ray tracing is used to track particle trajectories. Since the etching of the stack is mainly physical sputtering through ion bombardment, the etching rates of Si and SiGe can be assumed to be equal, while SiO₂ serves as a hard mask. During this step, the structure goes from that shown in Fig. 2(a) to Fig. 2(b).

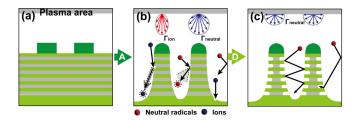


Fig. 2. (a) Initial substrate Si/SiGe stack profile, (b) Substrate profile after the anisotropic etching step (also input profile for the isotropic etching step), (c) Final substrate profile after both steps.

B. Diffusion of Ge atoms

Due to the bombardment of high-energy Ar⁺ in the Cl₂/Ar plasma while etching the Si/SiGe stack, Ge atoms will dissociate and diffuse along the surface, resulting in the formation of a Ge-containing layer along the sidewall [2], [9], which has a gradient of Ge composition near the SiGe/Si interface, as shown in Fig. 4(a). Since the etch rate depends on the Ge concentration, the Ge diffusion will affect the final etched profile.

In our model, the trajectory of these Ge atoms is considered. We assume that the SiGe layer is $Si_{0.75}Ge_{0.25}$ as-grown, so each SiGe and Si cell starts with 25 and 0 Ge atoms as shown in Fig. 4(b), respectively. The number of Ge atoms in the surface cell represents the Ge concentration. Once the Ar⁺ incidents and hits the SiGe cell at a certain angle θ , the Ge number of this cell will minus one (-1). Resulting in a Ge atom in this cell dissociates and diffuses to another cell at the same angle as the Ar⁺, the Ge number of this cell that accepts this Ge atom plus one (+1). When all the ion incident simulations

are finished, the final Ge concentration distribution is stored in the surface cells, as shown in Fig. 5.

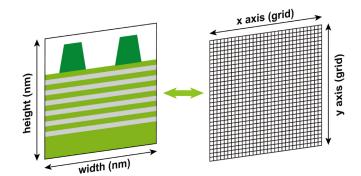


Fig. 3. The simulation domain is divided into grids using the cellular method.

C. Etch selectivity calculation

The etch selectivity between Si_{0.75}Ge_{0.25} and Si was previously shown to be about 150:1 [3]. Assuming a linear dependence between etch selectivity and Ge concentration, the selectivity of cells containing between 0 and 25 Ge atoms is given by a linear fit between 1:1 and 150:1, respectively, while all cells with more than 25 Ge atoms have a saturated selectivity of 150:1. According to section II.B, as Ge atoms are bombarded and diffused by Ar⁺, the number of Ge atoms in each cell continues to change as particles incident, and the Ge-containing layer as shown in Fig. 5 is finally formed. The number of Ge atoms in each cell of Ge-containing layer is different from that in the inner cell, which maintains the initial Ge atom number, but has a gradient change trend as shown in Fig. 4(b). Therefore, the selectivity of Ge-containing layer at different positions is different, resulting the etching rate is also different.

D. SiGe selective etching simulation

The modeling approach for the final selective etching simulation is similar to anisotropic etching. The difference is that the input plasma of CF₄/O₂/He is SiGe-selective and the neutral radical particle transport is diffuse, meaning no ion bombardment is involved. Same as anisotropic etching, particles incident from the top of the simulation domain. The incident site distribution of particles obeys a uniform distribution, which covers all plasma distribution areas. The angular distribution of the incident particles follows an isotropic uniform distribution, as shown in Fig. 2(c). Since only neutral radicals take part in the etching process, their movement inside the structure is governed by diffuse reflections from the surface. We identify the surface cells based on a 11×11 window size around the impact site first as shown in Fig. 6. Then, we use the least-square fitting to obtain a surface fitting line of these surface cells whose slope is a. The angle between the horizontal and the fitting line is $\beta = \tan^{-1} a$. Therefore, the incident angle of particle impact is $\gamma = \alpha + \beta$, the angle between the reflection line and the vertical line is $\mu = \pi - \gamma - \beta$. The particles will reflect along an angle with μ

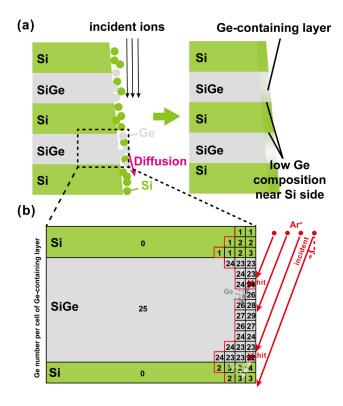


Fig. 4. (a) Formation mechanism of the Ge-containing layer on the sidewall surface of SiGe/Si stacks during anisotropic etching [2], (b) Schematic diagram of our method for dealing with diffusion of Ge atoms.

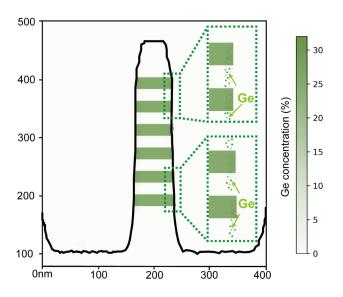


Fig. 5. Output Ge concentration distribution of part B.

as the axis and $\pm \theta/2$ as the interval range. We set a constant reflection probability R_p , and the particle will continue to reflect along the surface according to R_p until it reacts with the surface.

Similarly, SiO_2 is assumed to be a hard mask without etching loss, and the etching rates of different cells are calculated according to the etch selectivity given in section

II.C. The expected fishbone substrate structure is obtained, as shown in Fig. 2(c) using this modeling approach.

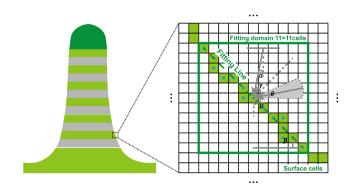


Fig. 6. Schematic diagram of particle reflection surface slope solving algorithm based on a least-square fit.

III. RESULTS AND DISCUSSIONS

We use our physical continuous two-step etching model to simulate two structures: an isolated six-layer structure (critical dimension, CD = 100nm) and a dense six-layer structure (Pitch/openCD = 200nm/100nm) as shown in Fig. 7(b) and Fig. 8(b). To validate the model, we performed experiments on the corresponding structures, and the TEM images for these bare shown in Fig. 7(a) and Fig. 8(a), respectively.

The silicon wafer used in the experiment was 8-in. Ptype monocrystalline silicon (100) with an average resistivity of 0.5-100 Ω . The Si/SiGe multilayers with six periodicities were grown wafers with reduced pressure chemical vapor deposition (RPCVD) equipment. The thickness of Si and SiGe layers were all set to 20nm for both isolated and dense structures. The pillars were patterned by electron beam lithography (EBL). Hard mask designed as a stack of SiO₂ for the subsequent anisotropic and isotropic etching was grown by plasma enhanced chemical vapor deposition (PECVD). Hard mask openings were formed by plasma etching using a gas mixture of CF₄/HBr/O₂ and the SiGe/Si anisotropic etching was performed with a HBr/O2 gas mixture. Finally, the selective etching of SiGe over Si was performed in a plasma chamber by gas mixture of CF₄/O₂/He in an inductively coupled plasma (ICP) reactor, Lam TCP 9400DFM.

We observe non-uniform profiles in both measured and simulation results. The lateral etching rate of the upper layers is higher than the lower layers, and the etch rate of inner surfaces is lower than outer surfaces in both experimental and simulated profiles. These effects are due to the non-uniform distribution of gases in the cavity. In addition, the edge rounding phenomena is observed for both Si and SiGe layers, caused by gradient changes in the Ge concentration at different locations on the surface [2].

ACKNOWLEDGMENT

This work was supported by the Strategic Priority Research Program of Chinese Academy of Sciences (Grant No.

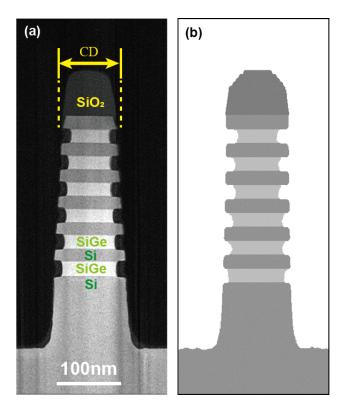
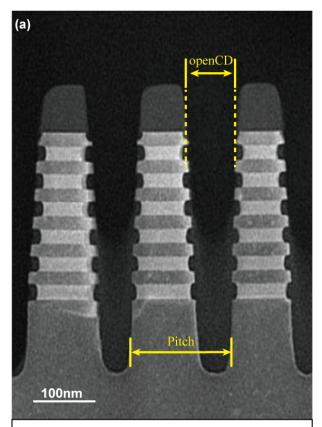


Fig. 7. (a) TEM image of an isolated 6-layer structure (CD = 100nm), (b) Corresponding simulation result.

XDA0330401) and the Youth Innovation Promotion Association of Chinese Academy of Sciences (2023129).

REFERENCES

- Mertens, Hans, et al. "Gate-all-around MOSFETs based on vertically stacked horizontal Si nanowires in a replacement metal gate process on bulk Si substrates." 2016 IEEE symposium on VLSI technology. IEEE, 2016.
- [2] Zhao, Yu, et al. "Formation mechanism of rounded SiGe-etch front in isotropic SiGe plasma etching for gate-all-around FETs." IEEE Journal of the Electron Devices Society 9 (2021): 1112-1116.
- [3] Loubet, Nicolas, et al. "A novel dry selective etch of SiGe for the enablement of high performance logic stacked gate-all-around nanosheet devices." 2019 IEEE International Electron Devices Meeting (IEDM). IEEE, 2019.
- [4] Yin, Xiaogen, et al. "Study of isotropic and Si-selective quasi atomic layer etching of $\mathrm{Si}_{1x}\mathrm{Ge}_x$." ECS Journal of Solid State Science and Technology 9.3 (2020): 034012.
- [5] Catano, Christopher, et al. "Peculiarities of selective isotropic Si etch to SiGe for nanowire and GAA transistors." Advanced Etch Technology for Nanopatterning VIII. Vol. 10963. SPIE, 2019.
- [6] Komori, Kana, et al. "SiGe vs. Si selective wet etching for Si gate-all-around." Solid State Phenomena 282 (2018): 107-112.
- [7] Oniki, Yusuke, Efraín Altamirano-Sánchez, and Frank Holsteyns. "Selective etches for gate-all-around (GAA) device integration: Opportunities and challenges." ECS Transactions 92.2 (2019): 3.
- [8] Hu, Ziyi, et al. "Modeling of microtrenching and bowing effects in nanoscale Si inductively coupled plasma etching process." Journal of Vacuum Science & Technology A 41.6 (2023).
- [9] Ditchfield, R., and E. G. Seebauer. "Direct measurement of ioninfluenced surface diffusion." Physical review letters 82.6 (1999): 1185.



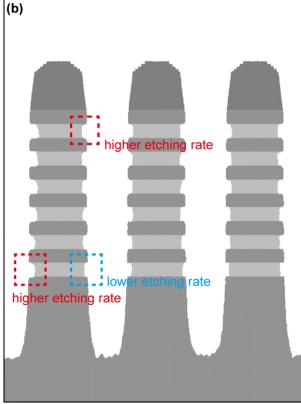


Fig. 8. (a) TEM image of a dense 6-layer structure (Pitch/openCD = 200nm/100nm), (b) Corresponding simulation result showing an excellent match with experiment.