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Modeling and Understanding Threshold Voltage and Subthreshold Swing in Ultrathin Channel Oxide Semiconductor Transistors

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***Abstract*— We present a physics-based model for ultrathin channel oxide semiconductor field-effect transistors (OSFETs) which successfully incorporates and explains several important OSFET physics: (1) threshold voltage dependence on OSFET device parameters such as channel thickness, gate dielectric capacitance, and gate metal work function, and OS material parameters such as electron affinity and channel doping, (2) impact of trap-like localized states due to the amorphous nature of the OS, (3) effect of sub-gap Gaussian states from oxygen vacancies and other point defects, and (4) the importance of enhancing gate control to alleviate the effect of traps on the subthreshold swing and threshold voltage.**

Keywords—Amorphous Oxide Semiconductors, BEOL Transistors, Low Leakage Transistors, Device Modeling and Simulations

I. Introduction

Oxide semiconductors, such as IGZO, ITO, and IWO, with bandgaps > 3 eV, have paved the way for ultra-low leakage transistors, rendering them highly sought-after for applications, such as 2T gain-cell memory [1, 2] that require leakage currents far below the level provided by silicon transistors. Furthermore, their low fabrication temperature (< 300 °C) makes them back-end-of-line (BEOL) compatible, enabling monolithic 3D integration with Si CMOS technology [1]. Achieving good I_{ON} and I_{OFF} with logic-compatible supply voltages (~ 1 V) is a critical requirement that the oxide semiconductor field-effect transistors (OSFETs) must meet to be viable for such applications [1]. This requires optimal control of their threshold voltage (V_{TH}) and subthreshold swing (SS), necessitating OSFET models that capture the underlying physics of OS films.

The low process temperature means that the OS films deposited are amorphous, making them disordered and rich in point defects such as oxygen vacancies (V_O) and interstitials (O_i) **[Fig. 1(a)]**. The amorphous disorder causes trap-like exponential band tail states, while the point defects can be treated as acceptor- or donor-type Gaussian states inside the bandgap **[Fig. 1(b)]**, which can adversely impact V_{TH} and SS.

While previous works modeled OSFETs, including sub-gap trap states [3,4], these models do not hold for ultrathin channels ($t_{CH} \leq 3$ nm), which show quantum confinement effects [5], and they did not incorporate the V_{TH} dependence on t_{CH} for highly doped channels [1]. Although the oxide semiconductor technology is quite matured within the display industry, borrowing the knowledge for logic and memory applications isn't straightforward as display applications enjoy the luxury of operating at larger supply voltages, with much thicker channel and gate dielectric, and relatively relaxed constraints on the OSFET performance and variability requirements. The desire to operate OSFETs at ~ 1 V, necessitating thin channel (< 5 nm) and gate dielectric (< 10 nm), requires a better understanding of the impact of channel thickness t_{CH}, gate dielectric capacitance C_{DE}, channel doping N_{CH} (donor V_O concentration), gate metal workfunction (Φ_M), OS electron affinity (X_S), band tail states and other point defects on the V_{TH} and SS, which is the subject of this paper.

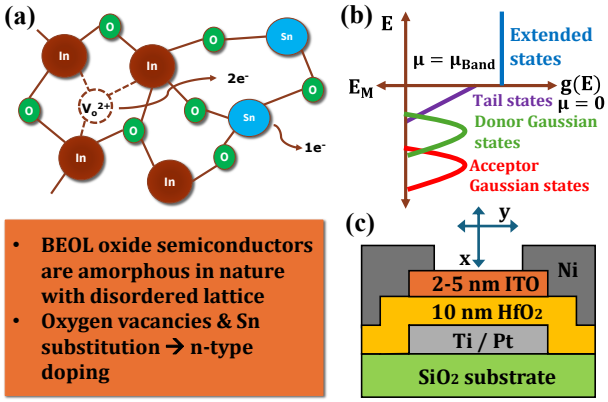

Fig. 1. **(a)** Schematic of an oxide semiconductor (Indium Tin Oxide in this case) depicting its amorphous structure, along with the presence of defects such as oxygen vacancies (V_O). The oxygen vacancies and the substitutional Sn act as donors, leading to n-type doping in ITO. **(b)** Model DoS considered in this study, including amorphous exponential band tail states, acceptor, and donor Gaussian defect states [6]. E_M is the mobility edge. The carriers in states above E_M are assumed to undergo band-like transport with $\mu = \mu_{Band}$, whereas those in states below E_M are assumed to be trapped with zero mobility. **(c)** Schematic device structure of a bottom-gated ITO FET considered for this study.

II. OSFET Model Description

To develop our model, we consider a bottom-gated Indium-Tin-Oxide (ITO) FET **[Fig. 1(c)]** and focus on the long-channel case, ignoring short-channel effects to gain a basic understanding. This allows us to reduce this to a series of one-dimensional problems at different locations along the channel by invoking the gradual channel approximation. All the solutions are then combined under the current continuity requirement to finally compute the drain current (I_D), as summarized in **Fig. 2**. Although we focus only on bottom-gated devices, the model, and also the analysis presented later, can easily be extended to the more complicated dual-gated and

nanosheet/nanowire device structures. These complicated device structures enhance the gate control and can be thought of as having higher C_{DE} in the analysis presented later. Coming to boundary conditions, the top surface of the channel is kept floating; thus, the corresponding potential is not fixed and varies with gate voltage (V_{GS}). Instead, we need to invoke the Neumann boundary condition of zero perpendicular field. The (quasi-)fermi level is dictated by the source and drain voltages (V_{DS}) combined with the current continuity requirement.

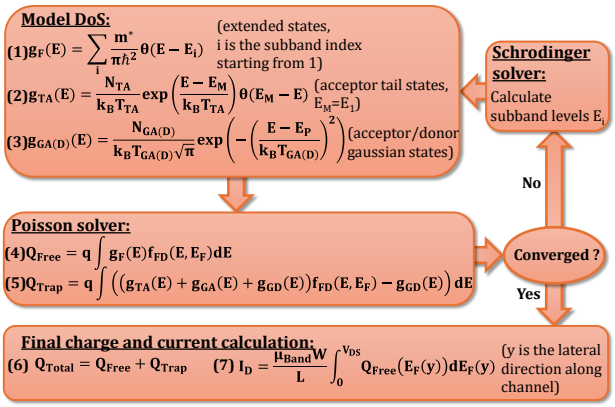

Fig. 2. Flowchart describing the OSFET model. A 1D coupled Schrodinger-Poisson solver incorporating the subgap defect states is considered.

To incorporate the disorder and point defects in the low-temperature amorphous OS films, we employ the model density of states (DoS) shown in **Fig. 1(b)** [6]. For the amorphous tail states, we assume that an exponential DoS connects to the extended states above the conduction band mobility edge (E_M), and the defect states are modeled using Gaussian DoS. These subgap trap DoS are characterized by parameters such as the total trap concentration and a characteristic temperature that denotes the energy width of the trap states. The Gaussian defect DoS also has an additional parameter, Ep, that corresponds to the energetic location inside the bandgap and is defined with respect to E_M.

Furthermore, the pursuit of OSFET technology for logic and memory applications imposes additional requirements on the device design. As will be elaborated later, ultrathin OS films ($t_{CH} \leq 3$ nm) are necessary to achieve sufficiently positive V_{TH} and minimize off-state leakage in highly doped channels, which is typically the case with OS channels. Thus, the model needs to account for the quantum confinement due to our choice of ultrathin OS films. Here, we assume that the quantum confinement only affects the extended states, creating sub-band levels, and hence, we assume a staircase-like DoS for the extended states (Fig.**1(b)** only shows the first sub-band). The sub-band levels for the extended states are calculated by a Schrodinger solver coupled with a Poisson solver in 1D, with the total charge from all the DoS considered.

Coming to the effect of quantum confinement on subgap DoS, the deep Gaussian DoS is due to the point defects, and we assume they are localized within a region much smaller than t_{CH} and thus unaffected by the channel confinement. We also assume they are uniformly distributed throughout the channel with a 3D volumetric trap density independent of t_{CH}. On the other hand, the exponential band tail states are typically delocalized over regions larger than t_{CH} and would be impacted by channel confinement. Thus, we consider a 2D areal density for the tail states, which is a complicated non-linear function of t_{CH}. The t_{CH}-dependence of tail states is an additional complexity that this work has not considered. Also, it is worth mentioning that the point defects, such as V_O, might be delocalized over a few Angstroms, which is not too small compared to a t_{CH} of, say 2nm, which raises questions on the assumptions made for the effect of confinement on point defects. A more detailed study, coupled with first principles DFT calculations, is needed to address the above complexities, which is out of the scope of this work and will be considered in future extensions of this paper.

Finally, the corresponding potential profile is solved using the 1D Schrodinger-Poisson solver for a given DoS. To calculate the current, we only consider the contribution from the extended states with the band mobility $\mu = \mu_{Band}$ under the assumption of multiple-trap-and-release (MTR) transport. This assumption is reasonable at room temperature and higher, with sufficient thermal energy for the electrons to release from the trap and undergo band-like transport. The model equations are all summarized in **Fig. 2**. The model can successfully fit existing experimental results [1] from 2nm ALD ITO FET, as illustrated in **Fig. 3(a-e)**.

III. Analysis and Discussion

After describing our OSFET numerical model in the previous section, we move on to a rigorous analysis of the OSFET physics in this section. Here, we derive simple analytical equations to illustrate the effect of various device and material parameters on the OSFET V_{TH} and SS.

A. Understanding OSFET V_{TH}

Starting with the OSFET V_{TH}, we derive an analytical expression of V_{TH} (see **Fig. 4(a)**) corresponding to a constant drain current level I_{Ref} in the subthreshold region. Now, there would be a corresponding channel potential φ_{Ref} for which this current level is achieved, as illustrated by the band diagram in **Fig. 4(b)**. Suppose the I_{Ref} is in the subthreshold region. In that case, we can assume the channel to be fully depleted of carriers, thus greatly simplifying the solution of the Poisson equation, and we arrive at the expression in **Fig. 4(a)**. All the V_{TH} expressions presented in this paper correspond to a constant current level I_{Ref} in the subthreshold region.

The OSFET V_{TH} is dissected into several contributing terms: the first is the mismatch between Φ_M and X_S. OSFETs are junctionless transistors typically "on" in flatband mode for high N_{CH}. Hence, high Φ_M gate metal and low X_S OS are critical for achieving a positive V_{TH}. The second term corresponds to the negative V_{GS} required to deplete the channel in the presence of a fixed positive N_{CH}, primarily due to donor V_O **[see Fig. 1(a)]**. The gate control over the channel dictates this term, giving a strong dependence on t_{CH} and C_{DE} ($= \epsilon_{DE}/t_{DE}$). An N_{CH} of ~ 10^{19} cm^{-3} (common in OS channels) typically requires a film thickness of around 2 nm to have a positive V_{TH} [1]. This ultrathin channel leads to quantum confinement, which causes an additional positive V_{TH} shift with approximately a t_{CH}^{-2}

dependence. **Fig. 4(c)** summarizes the OSFET V_{TH} dependence on t_{CH} and t_{DE} for high N_{CH}. In addition, there is also a V_{TH} shift due to the sub-gap traps, which is V_{GS}-dependent (as the occupation of trap states changes with V_{GS}) and will be described in subsections II.C & II.D.

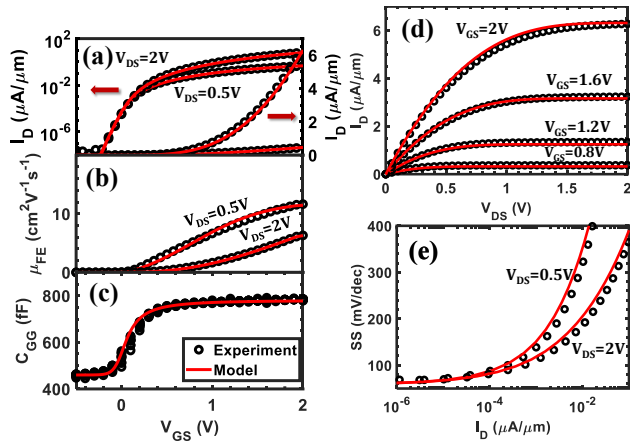

Fig. 3. The model (solid lines) fits experimental results (symbols) quite well, as shown in **(a)** I_D vs. V_{GS}, **(b)** μ_{FE} vs. V_{GS}, **(c)** C_{GG} vs. V_{GS}, **(d)** I_D vs. V_{DS}, **(e)** SS vs. I_D. ALD ITO FET with t_{CH} = 2 nm, t_{DE} = 10 nm, L = 2 µm, and W = 12 µm has been considered for experimental data [1].

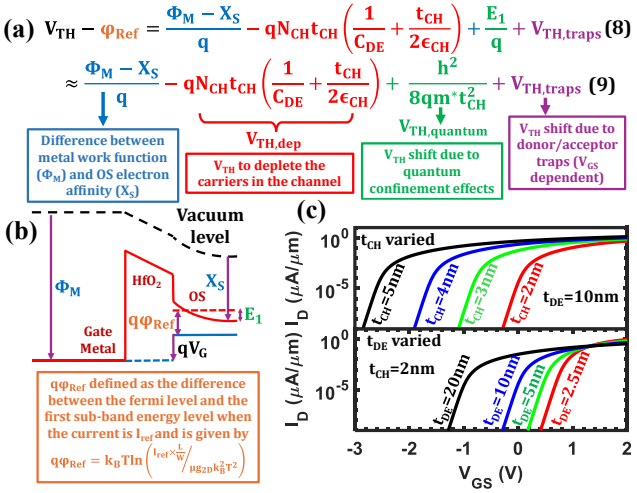

Fig. 4. **(a)** Analytical expression derived for V_{TH} extracted at a current level of I_{Ref} (φ_{Ref} and E_1 described in the adjoining band diagram), **(b)** band diagram explaining the derivation of the V_{TH} expression. The Poisson equation has been solved under the assumption of a fully depleted channel at the threshold condition. **(c)** Simulated OSFET transfer curves illustrating V_{TH} dependence on channel (t_{CH}) and gate dielectric (t_{DE}) thickness. The rest of the parameters are the same as the experimentally extracted parameters from **Fig. 3.**

B. *Choice of OS Material*

Understanding the physical significance of the abovementioned parameters and how they translate to various OS materials being investigated is also crucial. Cations / cationic compositions impact (1) the conduction band (E_C) level, i.e., different electron affinity X_S, and (2) the V_O concentration, which in turn, impacts the channel doping N_{CH} [7]. To understand this, we consider two cases with different X_S and N_{CH} in **Fig. 5(a)** with the same I_D-V_{GS} curves **[Fig. 5(b)]**. Upon investigating the corresponding band diagrams **[Fig. 5(c)]**, we can clearly understand the difference between having a lower E_C (high X_S) and a lower E_C-E_F difference (high N_{CH}). X_S causes a V_{TH} shift due to band misalignment without a thickness dependence. On the other hand, high N_{CH} alters the band bending due to space charge from the fixed positively-charged dopants, also leading to a V_{TH} shift. Hence, the high N_{CH} case has a strong t_{CH} dependence, as shown in **Fig. 5(d)**. Here, one can note that, despite having the same V_{TH}, the two cases have very different gate dielectric fields solely because of the absence/presence of fixed ionized dopants.

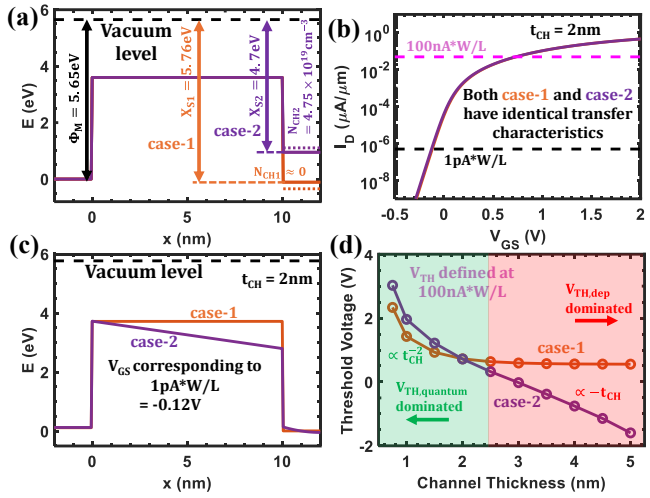

Fig. 5. Different OS material choices **(a)** Two OS cases considered one with high X_S & low N_{CH}, and vice-versa, giving same V_{TH} (case-1 in orange, case-2 in purple), **(b)** corresponding I_D-V_{GS} curves showing perfect overlap, **(c)** band diagrams in the OFF regime (at 1pA*W/L) for both the cases, case-2 with higher N_{CH} shows band bending due to space charge from unoccupied donor states, **(d)** V_{TH} dependence on t_{CH}, case-2 shows stronger t_{CH} dependence.

C. *Effect of Band Tail States*

To study the effect of band tail states. We consider the model DoS extracted from the experimental data in **Fig. 3**, plotted in **Fig. 6(a)**. The tail states are localized; thus, the charge carriers (electrons) in the tail states are assumed to be trapped with zero mobility. The proportion of free vs. trapped carriers for different V_{GS} is shown in **Fig. 6(b)**. While the free carrier concentration increases with V_{GS}, the trapped carrier concentration saturates at higher V_{GS}, when the tail states are entirely occupied. Next, we compare the I_D, μ_{FE} (field-effect mobility), and C_{GG} (total gate capacitance) vs. V_{GS} for the cases with and without tail states **[Fig. 6(c-e)]**. The tail states are shallow and do not affect the SS and V_{TH} in the "off" state; instead, they affect the SS in the transition region from "off" to "on." Also, for high V_{GS}, the tail states are fully occupied, which causes a V_{TH} shift in the "on" state. The effect of the tail states is well captured by the equations derived in **Fig. 6(f)**, where $C_G^{-1} = C_{DE}^{-1} + t_{CH}/2\epsilon_{CH}$.

D. *Effect of Gaussian Defect States*

The Gaussian states correspond to the point defects that can act as acceptor-type or donor-type traps. Their effect primarily depends on their energetic location in the band gap and their energy width, as illustrated by **Fig. 7(a,b)**. Although both the acceptor and donor states have identical effects on the SS, the V_{TH} shifts are opposite in sign because of their different charged and neutral modes. Like the fixed channel doping N_{CH}, the

impact of trap states also shows a strong dependence on the gate control [**Fig. 7(c, d)**]. The effect of the Gaussian traps is well-captured by the equations derived in **Fig. 8**.

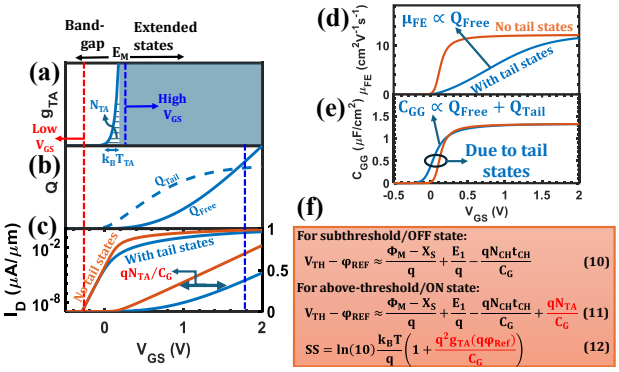

Fig. 6. **(a)** Tail state DoS considered, **(b)** charges trapped (C/cm^2) in tail states vs free carrier charges, **(c, d, e)** impact on I_D, μ_{FE}, and C_{GG}, due to tail states, **(f)** analytical equations summarizing the effect of tail states on V_{TH} and SS.

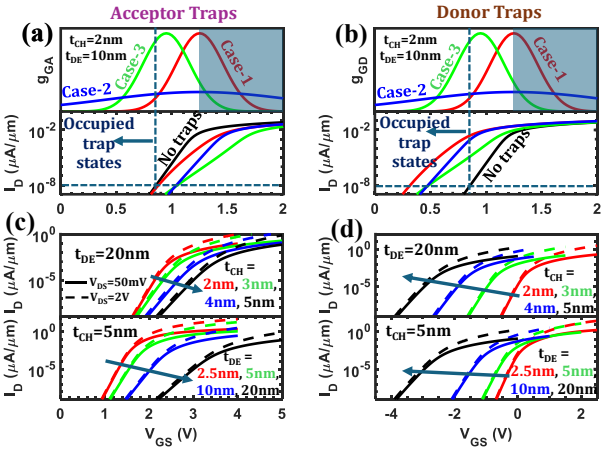

Fig. 7. **(a, b)** Effect of acceptor and donor Gaussian traps on I_D-V_{GS} based on their location in bandgap and their width, **(c, d)** t_{CH} & t_{DE} dependence in the presence of acceptor and donor defect states, showing better gate control alleviates the effect of traps. While the donor traps cause a negative shift, the acceptor traps cause a positive shift on increasing t_{CH} or t_{DE}.

Finally, we provide experimental signatures of our understanding of the effect of sub-gap defect states by comparing an ITO FET before and after annealing in Ar [1] (**Fig. 9**). The device characteristics after anneal show a negative V_{TH} shift accompanied by SS degradation, which can be well explained by the inclusion of donor Gaussian traps into the OSFET model.

IV. Conclusion

The model and the accompanying analysis in this paper make significant strides in understanding the OSFET physics, particularly targeting logic and memory applications requiring reduced supply voltages ~ 1 V along with thin channel (< 5 nm) and gate dielectric (< 10 nm), as opposed to existing studies on OSFETs for display applications operating at larger supply voltages, with much thicker channel and gate dielectric, and relatively relaxed constraints on the OSFET performance and variability requirements.

$$C_G\left(V_G - \frac{\Phi_M - X_S}{q} - \varphi_{CH}\right) = q\left(\int_{-\infty}^{q\varphi_{CH}-E_P} g_{GA}(E)dE - \int_{q\varphi_{CH}-E_P}^{\infty} g_{GD}(E)dE\right)t_{CH} \quad (13)$$

Occupied Acceptor Traps; Unoccupied Donor Traps

$$= qN_G(q\varphi_{CH} - E_P)t_{CH}$$

$$N_G(E_0) = \int_{-\infty}^{E_0}\{g_{GA}(E) + g_{GD}(E)\}dE - N_{GD} \quad (14)$$

N_{GD} is the total donor concentration

$$V_{TH} - \varphi_{Ref} = \frac{\Phi_M - X_S}{q} + \frac{E_1}{q} + \frac{qN_G(q\varphi_{Ref} + E_1 - E_P)t_{CH}}{C_G} \quad (15)$$

$$SS = \ln(10)\frac{k_BT}{q}\left(\frac{d\varphi_{CH}}{dV_G}\right)^{-1}_{\varphi_{CH}=\varphi_{Ref}}$$

$$= \ln(10)\frac{k_BT}{q}\left(1 + \frac{q^2(g_{GA}(q\varphi_{Ref} + E_1 - E_P) + g_{GD}(q\varphi_{Ref} + E_1 - E_P))t_{CH}}{C_G}\right) \quad (16)$$

Fig. 8. Equations summarizing the effect of Gaussian traps on V_{TH} and SS. Note that, here g_{GA} and g_{GD} are Gaussian functions centred around E = 0.

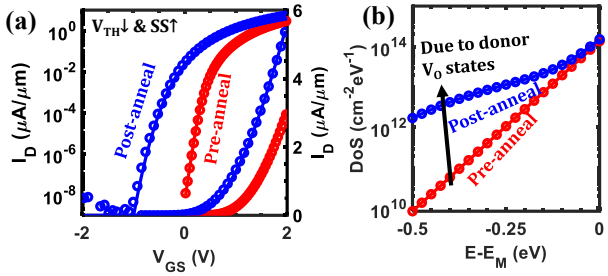

Fig. 9. **(a)** Model fit to experimental I_D-V_{GS} corresponding to 2 nm ALD ITO FET before and after annealing in Ar at 300 °C [1] (symbols-experiment, solid lines-model), **(b)** the corresponding DoS showing an increased deep trap state density due to additional donor V_O states created by M-O bond dissociation during annealing, leading to worse SS and negative V_{TH} shift.

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