Improved Compact Modeling of Snapback Behaviour in ESD MOSFETs

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***Abstract*—In this work, we present an improved physics-based ESD compact model to capture the snapback triggering voltage (V_{t1}) and the snapback triggering current (I_{t1}) which defines the on-set of the ESD protection device. The proposed model is designed to capture snapback behavior in both MOSFETs and HV-MOSFETs, without relying on parameters extracted solely from measurement data. The proposed model is successfully validated through extensive TCAD simulations and experimental data for HV-MOSFETs. The proposed model is simple and can be easily integrated with industry standard compact models.**

I. Introduction

Electrostatic discharge (ESD) poses a significant threat to the reliability and performance of integrated circuits (ICs). As semiconductor technology advances towards smaller geometries and higher densities, the susceptibility of devices to ESD events has increased markedly. These events can induce catastrophic failures or cause latent damage that may not be immediately evident but can lead to long-term reliability issues [1]–[4]. Consequently, accurate modeling of ESD phenomena is critical for the development of robust ICs.

One of the key challenges in ESD protection design is accurately modeling the snapback behavior observed in MOSFET devices during an ESD event. Snapback refers to the phenomenon where, after the device enters breakdown, the voltage across the device drops sharply while the current through the device increases exhibiting the negative resistance behavior [5], [6]. This behavior is crucial in defining the ESD protection characteristics of MOSFETs, as it determines the onset of effective current diversion away from sensitive circuitry and into the protection device.

Several ESD models have been developed over the years, focusing on various device structures such as diodes, silicon-controlled rectifiers (SCRs), and NMOS transistors [7]. These models often rely on empirical approaches to capture the snapback and fundamental ESD parameters [8]. While empirically derived models can accurately capture the device behavior based on measurement data, they often lack the underlying physical accuracy required for a comprehensive understanding and prediction of ESD performance across different operating conditions and device geometries.

* Equal Contribution

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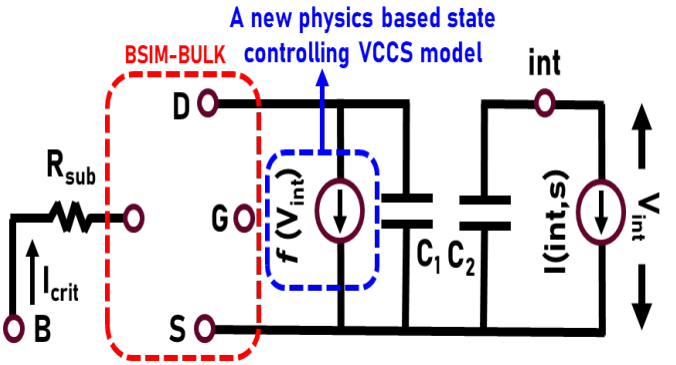

Fig. 1. Schematic of the improved ESD FET model: R_{sub} represents the substrate resistance, current source between drain and source is a function of internal voltage V_{int} [8]. C_1 and C_2 are the parallel capacitances of the subcircuit, which can be utilized for transient analysis.

In this paper, we present an improved physics-based ESD compact model specifically designed to capture the snapback triggering voltage (V_{t1}) and snapback triggering current (I_{t1}) that define the onset of ESD protection in MOSFET devices. Unlike traditional empirical models, our approach is rooted in the fundamental physical mechanisms governing snapback behavior, thereby enhancing the predictive capability and robustness of the model across a wide range of scenarios. Our proposed model is versatile and applicable to both standard MOSFETs and high-voltage MOSFETs (HV-MOSFETs) [9], addressing the need for a unified modeling framework that can be seamlessly integrated into industry-standard compact modeling tools. The model's accuracy and effectiveness are validated through extensive Technology Computer-Aided Design (TCAD) simulations and experimental data, demonstrating its ability to replicate observed snapback characteristics with high fidelity. The proposed improved compact model offers a significant advancement in the accurate representation of ESD snapback behavior in MOSFET devices. Its simplicity and integration capability make it a valuable tool for ESD protection design in modern semiconductor technologies. Rest of the paper is organized as follows: Snapback modeling is discussed in setion II followed by results and discussion in section III. Conclusion is drawn in section IV.

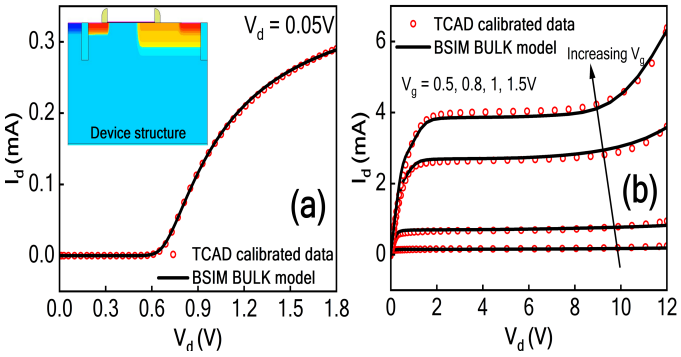

Fig. 2. (a) $I_d - V_g$ and (b) $I_d - V_d$ characteristics of TCAD simulated DEMOS calibrated with [12]. Inset shows the device structure ($L = 250nm$).

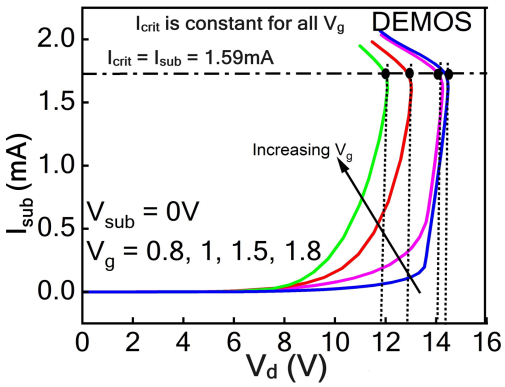

Fig. 3. Impact of V_g on V_{t1}: Plot of $I_{sub} - V_d$ shows I_{crit} remains constant for different V_g at the onset of snapback.

II. Snapback Modeling

Fig. 1 shows the schematic of the circuit implementation of the ESD FET model where, V_{int} represents an internal state variable physically modeled to capture the snapback [8]. The voltage-controlled current source (VCCS) is applied between the drain-source terminal of the device where the current is determined by the combination of instantaneous voltage and the on/off state of the subcircuit. $f(V_{int})$ characterizes the ESD snapback behavior, utilizing triggering voltage (V_{t1}) and triggering current (I_{t1}). In this work, we develop a new physics based compact model of V_{t1} and I_{t1} as a function of gate and substrate doping (N_{sub}). During device operation, as the drain-source voltage increases, breakdown occurs due to impact ionization, resulting in a high current flow through the substrate terminal. This voltage surge triggers the parasitic BJT effect in the device, leading to a significant increase in the source current. The voltage at which the parasitic BJT turns on is defined as the snapback triggering voltage (V_{t1}) and the corresponding current as I_{t1} [3].

These snapback parameters have been modeled using the impact ionization (II) components such as substrate current, peak electric field and electron density. The proposed model is implemented in BSIM-BULK HV compact model [10] and is validated with experimentally calibrated numerical simulations as well as with experimental data. As we discuss in the next section, accurate modeling of substrate current is crucial and therefore we have used recently developed improved II model for calibration [11]. Fig. 2 shows the TCAD and BSIM-BULK calibration with experimental DEMOS [12].

A. V_{t1} modeling

The total drain current constitutes of channel current, parasitic bipolar current and the avalanche generation current ($I_d = I_{ch} + I_{BJT} + I_{sub}$) [13]. The critical substrate current (I_{crit}) caused by impact ionization (II) is required to create a sufficient voltage drop across the emitter and base terminals of the parasitic BJT, leading to the onset of snapback. For different gate voltages, I_{crit} remains constant (see Fig. 3). I_{crit} depends on the peak electric field (E_m) and the electrons participating in impact ionization, which can be correlated to the channel current (I_{ds}) [11]. At a larger gate voltage, electron density increases, and a lower electric field or drain voltage is required to achieve the same critical substrate current. This explains the decrease in V_{t1} with increasing V_g. A brief model development of V_{t1}, derived from physics-based equations of impact ionization (II), is presented in the following equations.

$$\frac{I_{sub}}{I_{ds}} = E_m \cdot exp\Big(\frac{-\beta}{E_m}\Big) \tag{1}$$

Using Taylor series expansion,

$$exp\Big(\frac{-\beta}{E_m}\Big) = 1 - \frac{-\beta}{E_m} + \frac{-\beta^2}{2E_m^2} + ... \tag{2}$$

Neglecting higher order terms,

$$\frac{I_{sub}}{I_{ds}} = E_m \cdot exp\Big(1 - \frac{\beta}{E_m}\Big) \tag{3}$$

BJT turn on: $I_{sub} = I_{crit}$ and $V_d = V_{t1}$

$$E_m = \frac{V_d - (V_g - V_{th})}{\Delta L} \tag{4}$$

Here, ΔL represents the effective length over which electron-hole pairs are generated by impact ionization.

$$\frac{I_{crit}}{I_{ds}} \approx E_m - \beta \approx \frac{V_{t1} - (V_g - V_{th})}{\Delta L} - \beta \tag{5}$$

$$V_{t1} \approx \Delta L \cdot \frac{I_{crit}}{I_{ds}} + (V_g - c) \tag{6}$$

$$V_{t1} \approx \frac{I_{crit}}{k(V_g - c)^2} + (V_g - c) \tag{7}$$

Here, β is II model parameter, k is a constant which includes channel length, low field mobility and other process parameters and c is a voltage-based constant.

Compact model for V_{t1}

$$V_{t1} \approx p1 \cdot V_g + \frac{p2}{V_g^2} + p3 \tag{8}$$

Here p1, p2 and p3 are model fitting parameters. We have ensured there is no discontinuity at V_g = 0V by using a continuous quadratic polynominal function. As shown in Fig. 4, the proposed model captures the variations with V_g accurately.

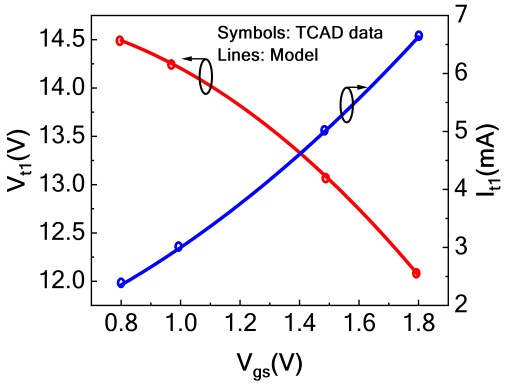

Fig. 4. Model validation for V_{t1} and I_{t1}: The model captures the variations with V_g accurately. The model have been developed keeping in mind the continuity and differentiability for higher order derivatives.

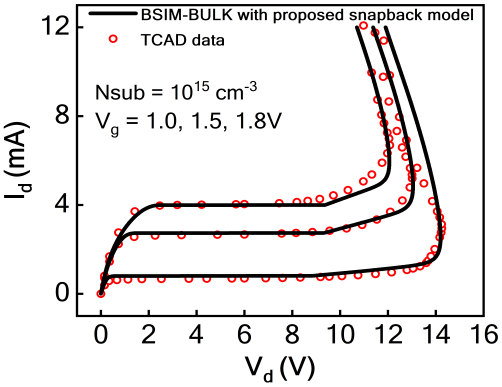

Fig. 6. Model validation: Snapback characteristics of TCAD simulated DEMOS having $N_{sub} = 10^{15} cm^{-3}$. The model is able to capture the snapback accurately for different gate voltages.

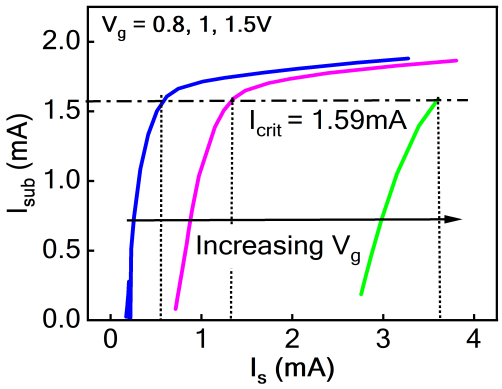

Fig. 5. Impact of V_g on I_s: At constant I_{crit}, increasing V_g leads to higher I_s. Hence, I_{t1} increases with high V_g. I_s starts to dominates on the onset of snapback.

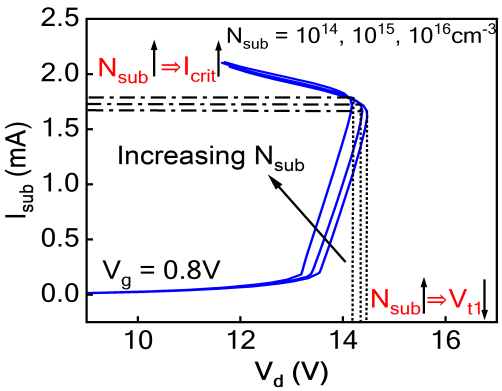

Fig. 7. $I_{sub} - V_d$ characteristics for different substrate doping (N_{sub}). I_{crit} increases with increasing N_{sub} (indicating decreased substrate resistance).

B. I_{t1} modeling

For high V_g, I_{t1} increases. As discussed above, the total current I_d is the sum of three components: I_{ch}, I_{BJT}, and I_{sub}. Before snapback, the source current component (I_s) is equivalent to channel current (I_{ch}). At high gate voltages, the BJT turns on early because I_{sub} reaches to critical substrate current (I_{crit}) level earlier. This increases the source current and makes it primarily determining factor of the total current as shown in Fig. 5. Hence, the magnitude of I_{t1} increases with the gate voltage (see Fig. 4).

III. Results and Discussions

Fig. 6 shows the snapback characteristics for the TCAD simulated DEMOS experimentally calibrated with [12]. The model accurately captures V_{t1} and I_{t1} for different gate voltages. The impact of substrate doping (N_{sub}) on snapback characteristics is also examined. As N_{sub} increases, the substrate resistance (R_{sub}) reduces since it is inversely proportional to the doping concentration. At a lower R_{sub}, reduced V_{t1} and a slightly increased I_{t1} are observed at the same gate voltage as shown in Fig. 7. Reduced R_{sub} requires higher critical substrate current to get sufficient forward bias of base-emitter junction. Now, at same gate voltage, electron density increases further due to which a lower peak electric field is needed to achieve the same increased I_{crit}. Hence, V_{t1} reduces. As the gate voltage remains constant, the relationship between electron density and peak electric field becomes evident, highlighting the interplay between these factors in maintaining the critical substrate current. Similarly, as I_{crit} increases, the total current I_d (comprising the channel current I_{ch}, the BJT current I_{BJT}, and the substrate current I_{sub} also rises, resulting in a higher I_{t1}. This increase in total current corresponds to the rise in the critical substrate current, as shown in Fig. 7. The elevated I_{crit} enhances the overall current through the device, indicating a direct correlation between I_{crit} and I_{t1}. As the critical current increases, it drives higher contributions from I_{ch}, I_{BJT}, and I_{sub}, leading to a significant rise in I_d and consequently in I_{t1}. This relationship is essential for understanding the impact of critical substrate current on the device's overall performance. To validate the model for different N_{sub}, experimentally calibrated DEMOS [12] has been tested for $N_{sub} = 10^{16} cm^{-3}$. Fig. 8 shows the snapback characteristics in which the proposed model accurately captures the snapback behaviour. To ensure a comprehensive validation of the model, it has been tested for the DEMOS experimental data

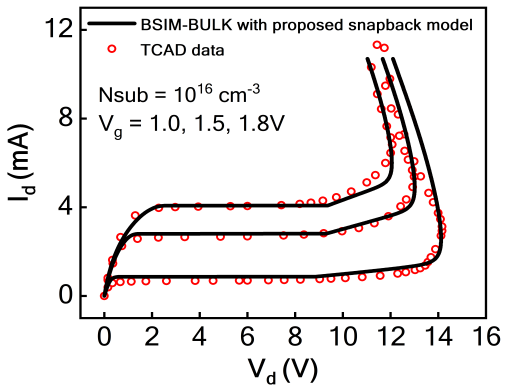

Fig. 8. Snapback model validation at different substrate doping concentration ($N_{sub} = 10^{16} cm^{-3}$). The model is able to capture the variations due to change in doping concentration accurately.

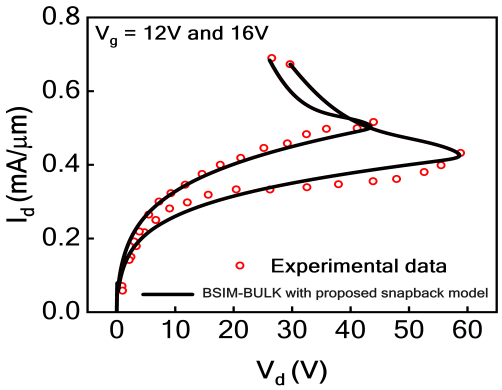

Fig. 9. Model validation with experimental DEMOS data [14]. Model accurately captures V_{t1} and predicts the snapback behavior for gate voltages (V_g = 12 and 16V).

[14], as presented in Fig. 9. This thorough validation process confirms the model's reliability and precision in replicating the observed experimental phenomena, thereby underscoring its robustness. The consistency between the simulated results and the experimental data further validates the effectiveness of our model in accurately predicting snapback behavior under various conditions.

IV. Conclusion

We have proposed an improved physics-based ESD compact model tailored to accurately capture snapback behavior in both MOSFETs and HV-MOSFETs. The model accurately captures doping and gate-bias dependency on both the triggering voltage V_{t1} and the triggering current I_{t1}. It is implemented in BSIM-BULK industry standard compact model, and is validated with numerical as well as experimental data. The proposed model represents a significant advancement in the precise modeling of ESD phenomena, contributing to improved device design and performance optimization in semiconductor technologies.

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References

[1] L.R. Avery, "A review of electrostatic discharge mechanisms and on-chip protection techniques to ensure device reliability," Journal of Electrostatics, vol. 24, no. 2, pp. 111-130, 1990, doi: 10.1016/0304-3886(90)90003-E.
[2] K. L. Kaiser, "Electromagnetic Compatibility Handbook," Electrical engineering handbook series, CRC press, 2005.
[3] C. Duvvury, and H. Gossner, "System Level ESD Co-Design," IEEE Press, John Wiley & Sons, 2015.
[4] Electrostatic Discharge (ESD) Technology Roadmap, EOS/ESD Association, Inc. 218 West Court Street Rome, NY 13440, January 2024.
[5] S. M. Sze, Y. Li, and K. K. Ng, "Physics of Semiconductor Devices," Hoboken, NJ, USA: Wiley, 2021.
[6] Y. Tsividis, "Operation and Modeling of the MOS Transistor," New York, NY, USA: McGraw-Hill, 1987.
[7] E. Rosenbaum, S. Huang, M. Drallmeier and Y. Zhou, "Compact Models for Simulation of On-Chip ESD Protection Networks," in IEEE Transactions on Electron Devices, vol. 71, no. 1, pp. 151-166, Jan. 2024, doi: 10.1109/TED.2023.3320093.
[8] T. Wang and C. C. McAndrew, "A Generic Formalism to Model ESD Snapback for Robust Circuit Simulation," 2018 40th Electrical Overstress/Electrostatic Discharge Symposium (EOS/ESD), Reno, NV, USA, 2018, pp. 1-8, doi: 10.23919/EOS/ESD.2018.8509752.
[9] H. Agarwal et al., "BSIM-HV: High-Voltage MOSFET Model Including Quasi-Saturation and Self-Heating Effect," in IEEE Transactions on Electron Devices, vol. 66, no. 10, pp. 4258-4263, Oct. 2019, doi: 10.1109/TED.2019.2933611.
[10] H. Agarwal, C. Gupta, Y. S. Chauhan, and C. Hu, "BSIM-Bulk MOSFET Model for IC Design—Digital, Analog, RF and High-Voltage." Woodhead, 2023.
[11] G. Gill, A. Singhal, G. Pahwa, C. Hu and H. Agarwal, "Compact Modeling of Impact Ionization in High-Voltage Devices," in IEEE Transactions on Electron Devices, vol. 70, no. 5, pp. 2389-2394, May 2023, doi: 10.1109/TED.2023.3253101.
[12] R. A. Bianchi, C. Raynaud, F. Blanchet, F. Monsieur and O. Noblanc, "High voltage devices in advanced CMOS technologies," 2009 IEEE Custom Integrated Circuits Conference, San Jose, CA, USA, 2009, pp. 363-370, doi: 10.1109/CICC.2009.5280839.
[13] S. H. Voldman, "ESD: Circuits and Devices", John Wiley & Sons, 2015.
[14] M. P. J. Mergens, W. Wilkening, S. Mettler, H. Wolf, A. Stricker and W. Fichtner, "Analysis of lateral DMOS power devices under ESD stress conditions," in IEEE Transactions on Electron Devices, vol. 47, no. 11, pp. 2128-2137, Nov. 2000, doi: 10.1109/16.877175.