Hierarchical Transport Modeling for Path-Finding DTCO

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***Abstract*—We present a hierarchical flow for predictive TCAD device simulation in DCTO applications. Using a thoroughly calibrated sub-band Boltzmann transport equation (SBTE) solver, TCAD device simulation parameters for the technology under investigation are generated automatically. This flow enables predictive accuracy of the SBTE solver at turn-around-times of SPICE simulations. It is demonstrated here for an A14 nanosheet technology, i) showing all intermediate calibration details and ii) highlighting a considerable improvement in the accuracy of ring-oscillator performance.**

***Index Terms*—Advanced CMOS logic, nanosheets, DTCO, TCAD, transport simulation**

I. Introduction

With increasing diversity in upcoming process nodes of the technology roadmap, path-finding design technology co-optimization (DTCO) has become an indispensable tool for semiconductor-technology equipment vendors, foundries, and design houses. While a considerable share of area and performance gain is attributed to various scaling booster and vertical integration schemes, improvements of the active transistors are still crucial. These include gate-length scaling, performance booster, and alternative channel materials. Since path-finding relies on accurate and predictive results, transport modeling in the active transistor is an essential component of the DTCO flow.

II. Calibration Flow

In this work, we follow a hierarchical calibration procedure (Fig. 1) that builds on characterization data and utilizes intermediate phases to accurately predict transistor performance and key-performance indicators (KPI) of logic cells with acceptable simulation turn-around-times (TAT).

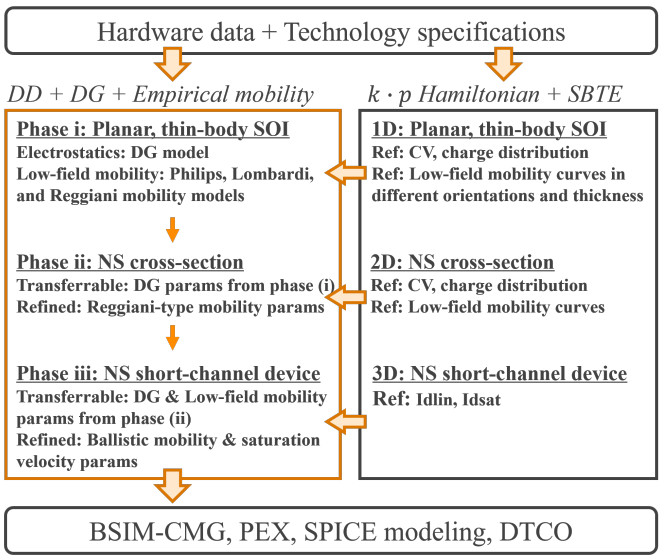


Fig. 1: Hierarchical calibration strategy used in this work.

A. Advanced Transport Simulation (Physical Device Simulation)

In previous work [1], the sub-band Boltzmann transport equation (SBTE) has been proven accurate for advanced CMOS short-channel devices, capturing all relevant physical effects. It allows for meaningful parameter sets that are transferable between technology nodes and test vehicles.

Here, the GTS Nano-Device Simulator [2] with $\mathbf{k}\cdot\mathbf{p}$ Hamiltonian is used. All relevant scattering processes: Coulomb, acoustic phonon, optical phonon, and surface roughness, have been precisely calibrated against hardware data. An exponentially decaying acoustic phonon deformation potential from surface to bulk, suggested in [3], has been calibrated for (100) and (110) thin-body SOI to account for the orientation and thickness dependencies of the channel.

B. TCAD Device Simulation

Our drift-diffusion (DD) simulator MinimosNT [4] uses the density gradient (DG) model [5], as well as Matthiessen's rule to combine a Philips mobility [6] for bulk lattice and impurity scattering, a Lombardi mobility [7] for acoustic phonon scattering at the surface, and a Reggiani-type surface roughness mobility [8].

Mobility degradation in thin layers is modeled using the modified phonon mobility of the Reggiani model [8]. High-field transport is described by a Canali-type high-field mobility with constant saturation velocity [9] and a ballistic mobility correction [10]. The parameters of surface orientation-dependent models at each point are assigned from the orientation of the closest surface (auto-orientation).

Planar MOS and planar thin-layer SOI hardware data are the basis for the calibration of both the SBTE and the DD simulations. The calibration proceeds in three phases:

i. The CV curves and charge distributions of DD are calibrated against those of SBTE for each orientation using DG model. Then the scattering parameters of the SBTE and the empirical mobility parameters from DD are calibrated against the measured low-field mobility curves from literature for bulk Planar and for the ultra-thin body SOI [11–15], as shown in Fig. 2.
ii. We then use the SBTE to calculate the charge distribution, CV curve, and low-field mobility for a 2D channel cross-section of the target technology, e.g., nanosheet (NS) technology as shown in Fig. 3 and Table I. By comparing the electrostatics and low-field mobility from SBTE to those from DD using phase **i** parameters, we found a good transferability of the DG parameters. On the other hand, strong improvements were obtained from the refinement of Reggiani-type surface roughness and phonon mobility parameters as illustrated in Fig. 4.

iii. Finally, we use the SBTE to calculate the full linear and saturation transfer characteristics for the 3D short-channel device using the same NS technology spec as phase **ii**. The effective ballistic mobility as well as the saturation velocity of DD are calibrated to SBTE, see Fig. 5.

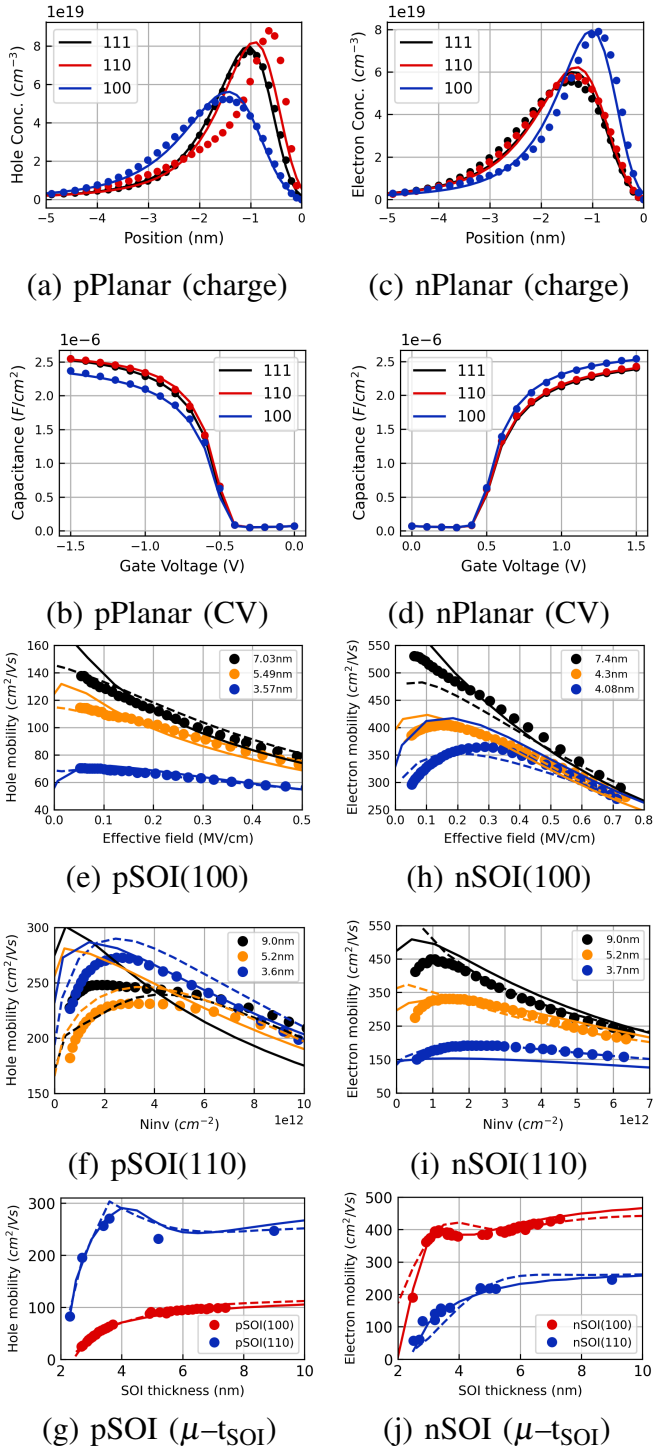


Fig. 2: Calibration phase **i**: Charge distributions at $|V_G|$ = 1 V and CV curves of (a–b) pPlanar and (c–d) nPlanar from DD (lines) and SBTE (symbols). Low-field (e–g) hole and (h–j) electron mobility curves of thin-layer SOI from both DD (solid) and SBTE (dashed) have been calibrated to literature data (symbols) to account for orientation and thickness dependencies.

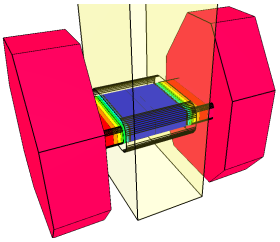


Fig. 3: NS structure used in calibration phases **ii** and **iii**.

TABLE I: NS technology spec

(100) Substrate & [110] Channel	
NS Height [nm]	5
NS Width [nm]	20
SiO_2/HfO_2 [nm]	0.7/1.5
L_{Spacer} [nm]	7
L_{Gate} [nm]	10, 20, 30
$N_{Channel}$ [cm^{-3}]	2×10^{16}
N_{Epi} [cm^{-3}]	2×10^{20}

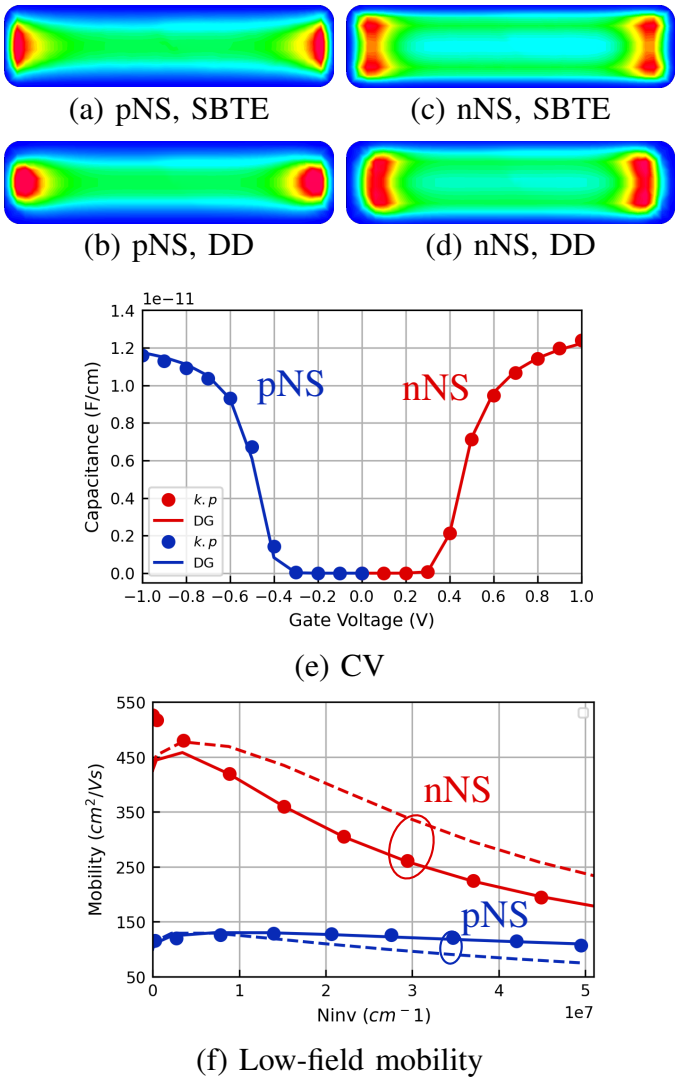
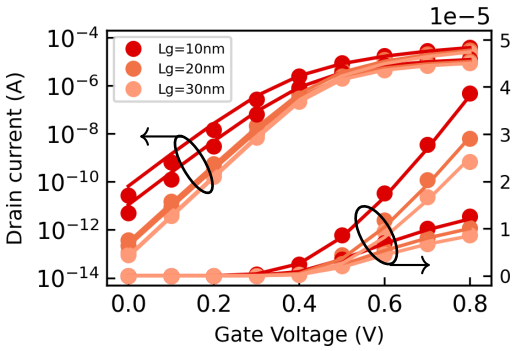
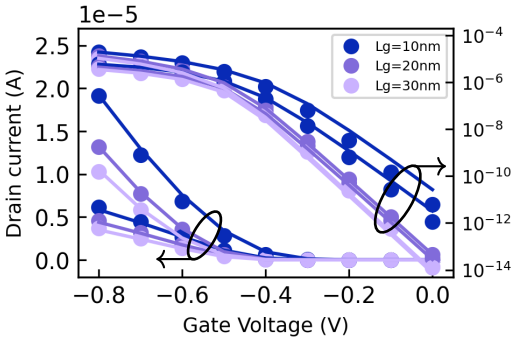


Fig. 4: Calibration phase **ii**: (a–d) Charge distributions at $|V_G|$=1 V and (e) CV curves of pNS and nNS cross-sections from SBTE and DD, showing well transferability of phase **i** DG parameters. (f) Low-field mobility curves from DD and SBTE, in which phase **i** parameters (dashed) are further refined (solid) against SBTE results (symbols).

The calibrated SBTE scattering parameters and phase **iii** DD parameter set are shown respectively in Table II and Table III. This procedure yields a distinct predictive DD transport parameter set reproducing both electrostatics and carrier mobility for a specific technology implementation.



(a) nNS



(b) pNS

Fig. 5: Calibration phase **iii**: Linear (V_D = 0.05 V) and saturation (V_D = 0.8 V) transfer characteristic curves of (a) nNS and (b) pNS from DD (lines) versus SBTE (symbols) with L_G = 10, 20, and 30 nm.

TABLE II: Calibrated SBTE scattering parameters

{100} Surface		Electron	Hole	Unit
Acoustic Phonon	$D_{ac,bulk}$ / $D_{ac,surf}$	9.0 / 18.0	5.4 / 21.0	eV
	λ_{ac}	3.2	4.0	nm
Surface Roughness	Δ_{RMS}	0.3	0.24	nm
	L_{corr}	1.0	1.0	nm

TABLE III: DD phase **iii** mobility parameters

{100} Surface		Electron	Hole	Unit
Acoustic Phonon	B	1.0×10^6	1.0×10^7	cm^2/Vs
	C	440	1450	cm^2/Vs
Bulk Phonon	$\mu_{ph,1}$	1434.8	407.9	cm^2/Vs
	$\mu_{ph,2}$	37.4	10.0	cm^2/Vs
	p_1	0.26	0.0	-
	p_2	427	21.2	-
	p_3	1.7	5.0	-
	m_{z1}	0.916	0.29	-
	m_{z2}	0.196	0.25	-
	W_{T01}	5.4×10^{-10}	0.0	cm
	W_{T02}	3.6×10^{-11}	0.0	cm
Surface Roughness	μ_{sr0}	142.6	694.1	cm^2/Vs
	δ	1.61	0.62	-
Thickness Fluctuation	$\mu_{\delta t0}$	0.55	0.06	cm^2/Vs
	E_{eff0}	4.0×10^4	4.0×10^4	V/cm
Surface Phonon	μ_{sp0}	1.4×10^{-8}	1.2×10^{-10}	cm^2/Vs
	t_{sp0}	0.1	0.1	nm
Ballistic Mobility	v_T	2.7×10^7	2.1×10^7	cm/s
	V_b	0.8	0.8	V
	p	0	0	-
Saturation Velocity	v_{sat}	2.3×10^7	1.3×10^7	cm/s
	β	1.0	1.0	cm^2/Vs

C. DTCO (Full-Cell)

Using a full DTCO [16] flow, the effect of the device calibration as outlined is demonstrated on a NS technology targeting A14 design rules (see Fig. 6). V_{DD} roll-off is shown for three different gate lengths (see Fig. 7) and compared using default versus calibrated phase **iii** DD parameters. Although trends are captured qualitatively, a deviation in the ring oscillator KPI of up to 76% can be observed for the uncalibrated case as demonstrated in Fig. 8.

III. Conclusion

The importance of accurate modeling of the active device for path-finding DTCO is highlighted. A fully automated flow based on a hierarchical device model calibration methodology is proposed and demonstrated on an A14 NS technology. A marked shift up to 76% of the performance metrics is observed between uncalibrated and calibrated transport parameter sets which further emphasizes the relevance of thorough calibration for accurate performance prediction.

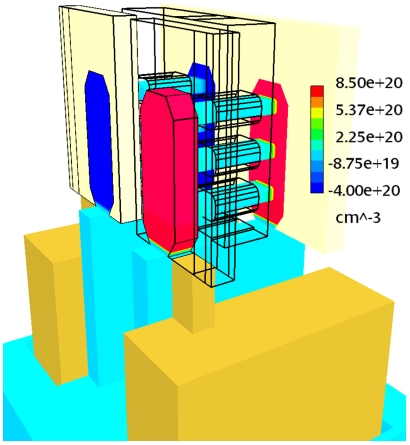


Fig. 6: A14 inverter with 3 stacked NS and buried power rails. Base technology: Lowest horizontal metal pitch: 18 nm, contacted gate pitch: 42 nm, gate length: 20 nm, NS height: 5 nm, NS width: 15 nm.

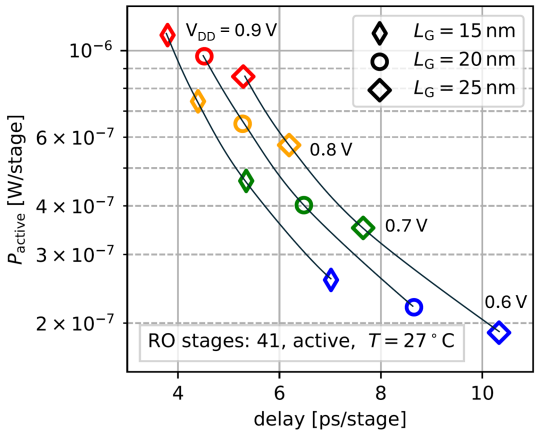


Fig. 7: Power performance of 41 inverter stages (see Fig. 6) chained for an active ring-oscillator (RO). V_{DD} roll-off is shown for three different gate lengths. The tradeoff between power and delay allows short L_G for this technology.

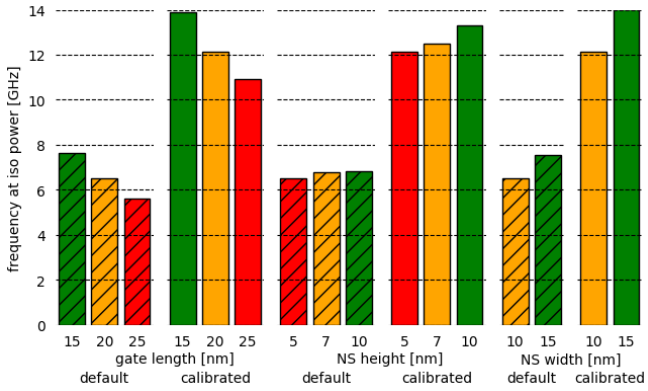


Fig. 8: Simulation of RO frequency at a fixed total power of 10 μW using default (dashed) and calibrated (solid) transport parameters. For default, trends are qualitatively captured, however, a significant discrepancy in the absolute value of the result is apparent.

IV. Acknowledgment

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References

[1] Z. Stanojević, C.-M. Tsai, G. Strof, F. Mitterbauer, O. Baumgartner, C. Kernstock, and M. Karner, "Nano Device Simulator-Practical Subband-BTE Solver for Path-Finding and DTCO," *IEEE Transactions on Electron Devices*, vol. 68, no. 11, pp. 5400–5406, 2021.

[2] *Nano-Device Simulator (NDS). Available online: https://www.globaltcad.com/products/gts-nano-device-simulator.*

[3] T. Ohashi, T. Tanaka, T. Takahashi, S. Oda, and K. Uchida, "Experimental study on deformation potential (D_{ac}) in mosfets: Demonstration of increased D_{ac} at mos interfaces and its impact on electron mobility," *IEEE Journal of the Electron Devices Society*, vol. 4, no. 5, pp. 278–285, 2016.

[4] *Minimos-NT. Available online: https://www.globaltcad.com/products/gts-minimos-nt.*

[5] A. Wettstein, A. Schenk, and W. Fichtner, "Quantum device-simulation with the density-gradient model on unstructured grids," *IEEE Transactions on Electron Devices*, vol. 48, no. 2, pp. 279–284, 2001.

[6] D. Klaassen, "A unified mobility model for device simulation-i. model equations and concentration dependence," *Solid-State Electronics*, vol. 35, no. 7, pp. 953–959, 1992.

[7] C. Lombardi, S. Manzini, A. Saporito, and M. Vanzi, "A physically based mobility model for numerical simulation of nonplanar devices," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 7, no. 11, pp. 1164–1171, 1988.

[8] S. Reggiani, E. Gnani, A. Gnudi, M. Rudan, and G. Baccarani, "Low-field electron mobility model for ultrathin-body soi and double-gate mosfets with extremely small silicon thicknesses," *IEEE Transactions on Electron Devices*, vol. 54, no. 9, pp. 2204–2212, 2007.

[9] C. Canali, G. Majni, R. Minder, and G. Ottaviani, "Electron and hole drift velocity measurements in silicon and their empirical relation to electric field and temperature," *IEEE Transactions on Electron Devices*, vol. 22, no. 11, pp. 1045–1047, 1975.

[10] A. Erlebach, K. H. Lee, and F. M. Bufler, "Empirical ballistic mobility model for drift-diffusion simulation," in *2016 46th European Solid-State Device Research Conference (ESSDERC)*, pp. 420–423, 2016.

[11] S. Takagi, A. Toriumi, M. Iwase, and H. Tango, "On the universality of inversion layer mobility in si mosfet's: Part i-effects of substrate impurity concentration," *IEEE Transactions on Electron Devices*, vol. 41, no. 12, pp. 2357–2362, 1994.

[12] S. Takagi, A. Toriumi, M. Iwase, and H. Tango, "On the universality of inversion layer mobility in si mosfet's: Part ii-effects of surface orientation," *IEEE Transactions on Electron Devices*, vol. 41, no. 12, pp. 2363–2368, 1994.

[13] K. Uchida, H. Watanabe, A. Kinoshita, J. Koga, T. Numata, and S. Takagi, "Experimental study on carrier transport mechanism in ultrathin-body soi nand p-mosfets with soi thickness less than 5 nm," in *Digest. International Electron Devices Meeting,*, pp. 47–50, 2002.

[14] G. Tsutsui, M. Saitoh, T. Saraya, T. Nagumo, and T. Hiramoto, "Mobility enhancement due to volume inversion in [110]-oriented ultra-thin body double-gate nmosfets with body thickness less than 5 nm," in *2005 IEEE International Electron Devices Meeting IEDM Technical Digest.*, pp. 729–732, 2005.

[15] G. Tsutsui, M. Saitoh, and T. Hiramoto, "Experimental study on superior mobility in [110]-oriented utb soi pmosfets," *IEEE Electron Device Letters*, vol. 26, no. 11, pp. 836–838, 2005.

[16] G. Rzepa, K. K. Bhuwalka, O. Baumgartner, D. Leonelli, H.-W. Karner, F. Schanovsky, C. Kernstock, Z. Stanojevic, H. Wu, F. Benistant, C. Liu, and M. Karner, "Performance and variability-aware sram design for gate-all-around nanosheets and benchmark with finfets at 3nm technology node," in *2022 International Electron Devices Meeting (IEDM)*, pp. 15.1.1–15.1.4, 2022.