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First Simulation of the Effects of Metal Sidewall Source/Drain and Channel Number on the Output Characteristics of Current Mirror Formed by Vertically Stacked GAA Si NS MOSFETs

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***Abstract*—In this work, we study the effect of metal sidewall (MSW) source/drain (S/D) on the circuit performance of current mirror (CM) formed by vertically stacked gate-all-around (GAA) nanosheet (NS) for the first time. Device DC characteristics and output current of CM with (w/) and without (w/o) MSW S/D are explored by using an experimentally calibrated 3D numerical device-circuit simulation. Electrostatic potential distribution in the explored CM changes significantly because of serious parasitic resistance of S/D. The CM w/ MSW S/D reduces the parasitic resistance of S/D and has great influence on output characteristics relying on the channel number of GAA devices of the CM circuit.**

***Keywords*—Current mirror, Metal sidewall source and drain, Vertically stacked GAA Si NS MOSFETs, Device Simulation, Circuit Performance, Mixed device and circuit simulation.**

I. Introduction

Vertically stacked gate-all-around (GAA) Si nanosheet (NS) MOSFETs have been proposed and advanced to be a candidate to replace FinFET architecture for sub-3-nm device technologies [1]-[7]. Modeling studies of GAA Si NS MOSFETs including machine learning approach attract a lot of attention for IC design and simulation based on GAA Si NS MOSFETs [5]-[7]. Vertical stack is one of promising techniques to further increase the density of devices in chip fabrication, which has been applied to logic, memory and analog circuits [8]-[18]. Researchers have reported that metal sidewall (MSW) source and drain (S/D) can suppress parasitic effect; in particular, for parasitic resistance in 3D device due to the tall S/D, making it possible for us to further increase the number of vertically arranged devices [14]-[15].

In this work, we firstly explore vertically stacked GAA Si MOSFETs current mirror which is an essential part of analog IC. We study the effect of MSW S/D on reducing parasitic resistance of S/D has a limit, where optimal channel number is discussed based on the current conducted by each channel.

II. The GAA Si NS MOSFETs Current Mirror

To provide the best accuracy of device simulation, the transfer characteristics of a three-channel GAA NS device is calibrated based on the measurement data of IBM® by Loubet et al. [1], as shown in Fig. 1. The device simulations are performed intensively, where the carrier mobility considers

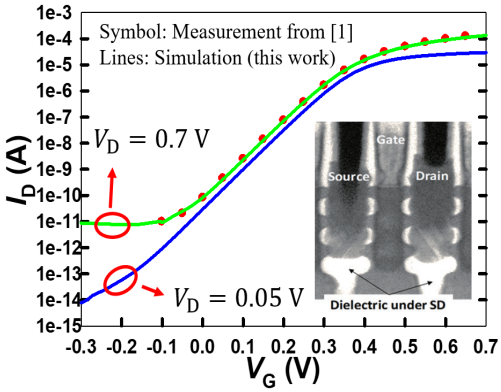

Fig. 1. Accuracy calibration with the measured transfer characteristics of a three channel NS FET. The inset shows the TEM of sample [1]. The extracted $V_{th,lin}$ and $V_{th,sat}$ are 0.319 and 0.294 V, respectively.

Philips' unified model, high field saturation model and thin layer mobility model together with the Matthiessen's rule. Band-to-band tunneling model and Auger tunneling model are applied to better capture the device characteristics. Regarding the calibration with the measured I_D–V_G data, first, the work-function (range: 4.4~5.0 eV) of gate metal was tuned so that the simulated curve can approach to the measurement. Second, the interface trap density (range: 10^{11}~10^{12} cm^{-2} eV^{-1}) was calibrated to align the measurement.

Fig. 2(a) illustrates the explored three-channel NS structure, whose section view is shown in Fig. 2(b); it has 12-nm channel length, 1.52-nm effective oxide thickness and 180-nm effective channel width. Figs. 2(c) and (d) show the normalized V_{th} and I_{off}, respectively. The current of devices is expected to be linear to the number of channel, N_{ch}, and the threshold voltage is expected to be independent of N_{ch}. The V_{th} and I_{off} obeys the trend, but the normalized I_{on}, as shown in fig. 2(e), cannot meet the trend w/o the MSW S/D when N_{ch} increases.

Fig. 3 shows the 2-D cut-plane of the current density in each channel of eighteen-channel devices w/ and w/o MSW S/D. The current density of bottom channels are significantly smaller than upper channels. For example, the channel 1 of the 18-stacked NS w/o MSW is only one fourth of that in the channel 18. This

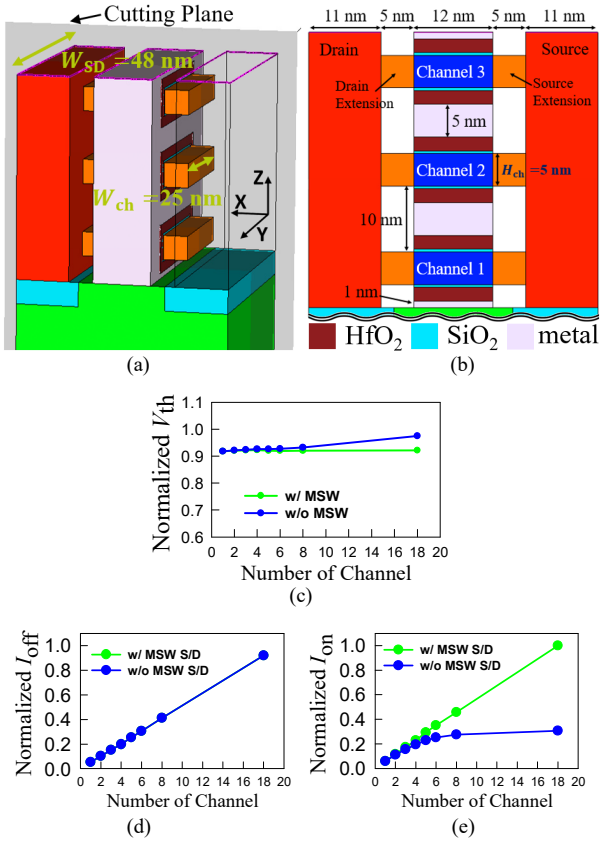

Fig. 2. (a) A 3D illustration and (b) a cross-sectional plot of the simulated three-channel GAA NS FET along the cutting plane. The channels are numberd from the bottom to the top, starting by one. The normalized (c) V_{th} is almost independent of number of channel and (d) I_{off} is linear to number of channel, showing that these characteristics are not affected by number of channel. However, the (e) I_{on} of devices w/o MSW S/D fail to stay linear to number of channel, indicates that they suffer from parasitic resistance, having positive relation to device height, more.

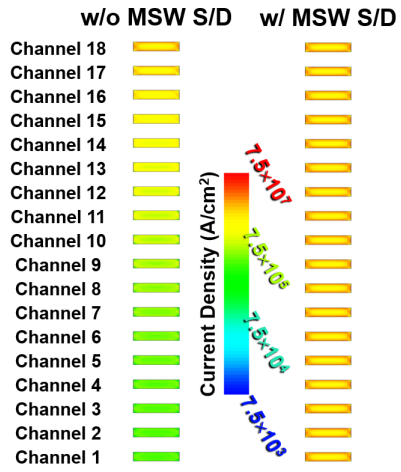

Fig. 3. A 2-D cut-plane of the current density of the simulated eighteen-channel GAA devices w/ and w/o MSW S/D perpendicular to the channel near drain side, showing channels only. The current density of bottom channels of devices w/o MSW S/D (the left figure) is reduced because of the parasitic resistance of S/D. The right one shows very uniform high current density distribution among all channcels when devices are with MSW S/D. The current density has no difference from the top channel 18 to the bottom channel 1.

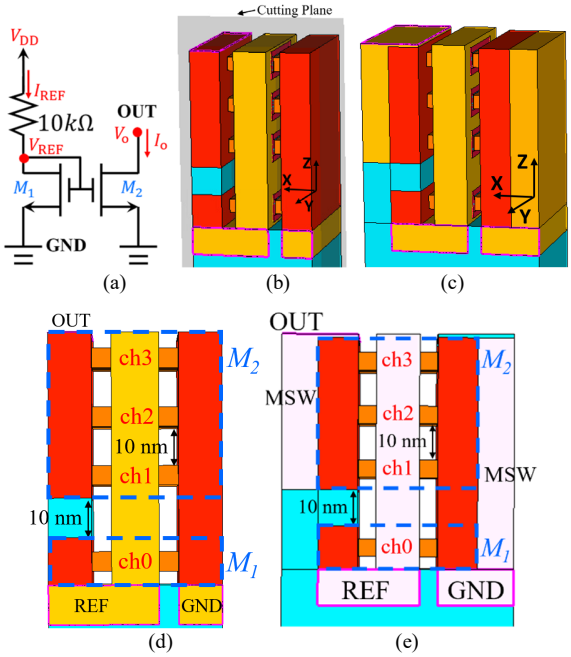

Fig. 4. (a) The CM circuit diagram. 3D structure of CM (b) w/o and (c) w/ MSW S/D. Lateral views of CM (d) w/o and (e) w/ MSW S/D. The channel number of the transistor M_1 is fixed here.

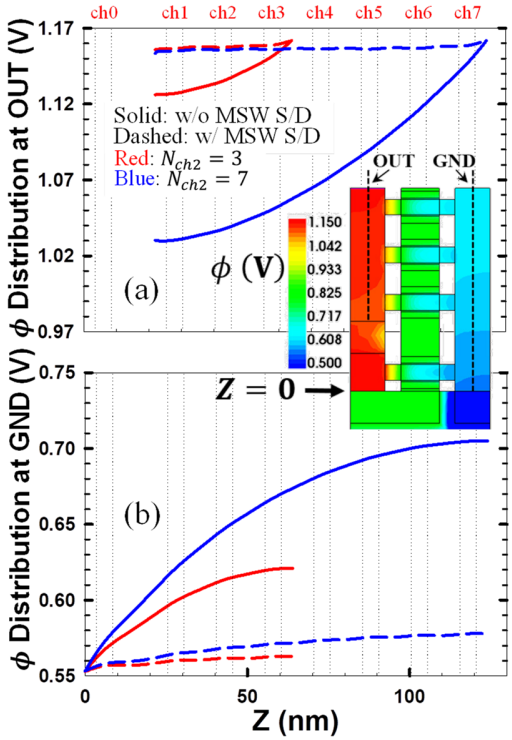

Fig. 5. Electrostatic potential distributions (ϕ) at nodes (a) OUT and (b) GND, corresponding to Fig. 4(a), from the top to substrate along the cut lines of inset, respectively, when $V_{OUT} = V_{REF, Ideal}$. Refering to 3D plots of Figs. 4(b) and (c) or 2D cross sections of Figs. (d) and (e), the inset is the assocated simulated potential of the GAA devices inside the CM circuit. Notably, the GAA device of CM w/ MSW S/D shows much more uniform ϕ with different N_{ch2}. The distribution of potential determines the circuit performance of CM constructed by vertically stacked GAA Si MOSFETs.

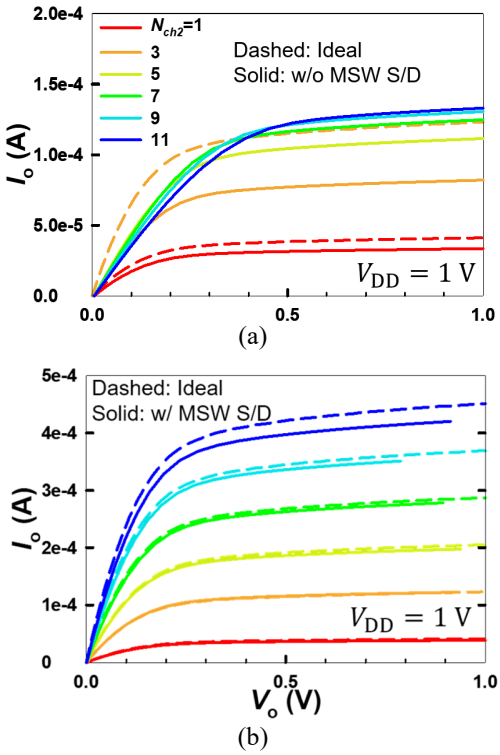

Fig. 6. Comparison of I_o among the ideal CM, (a) CM w/o MSW S/D and (b) CM w/ MSW S/D. The I_o of CM w/ MSW S/D almost reaches ideal level, while the I_o of CM w/o MSW S/D does not.Potential distributions (ϕ) at nodes (a) OUT and (b) GND from the top to substrate along the cut lines of inset, respectively, when V_{OUT} = $V_{REF,\ Ideal}$. CM w/ MSW S/D shows more uniform ϕ with different N_{ch2}.

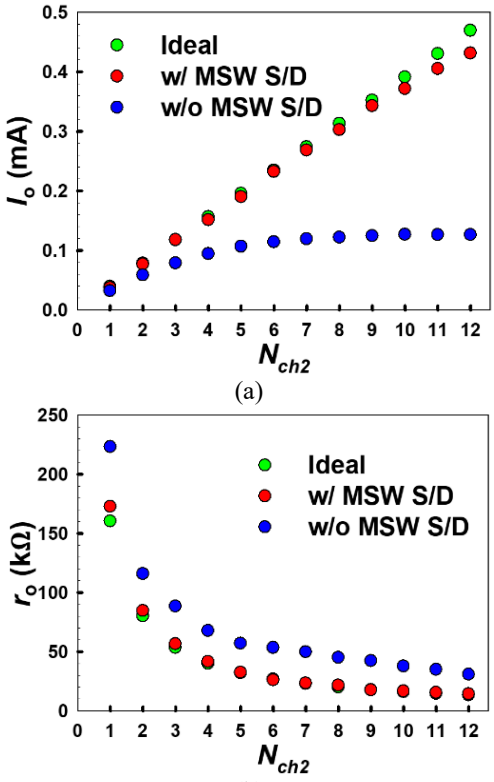

Fig. 7. (a) I_o and (b) r_o of CM versus N_{ch2}. CM w/o MSW S/D has smaller I_o and larger r_o owing to nonlinear potential distribution of S/D. Both I_o and r_o of CM w/ MSW S/D still close to the ideal case when the N_{ch2} increases; however, the I_o difference appears when $N_{ch2} > 7$.

phenomenon occurs not only in tall vertically stacked GAA devices w/o MSW S/D but also in CMs w/o MSW S/D.

Fig. 4(a) is the circuit diagram of CM, along with the name of each transistor, signal and node. The CM reference current is calculated by

$$I_{REF} = \frac{V_{DD} - V_{GS1}}{10\ k\Omega}, \quad (1)$$

where V_{GS1} is the gate-to-source voltage of M_1, shows that M_1, V_{DD} and the 10-kΩ resistor determines I_{REF}. The ideal relationship between the CM output current, I_o, and I_{REF} when all of the transistors work in saturation mode is given by

$$\frac{I_o}{I_{REF}} = \frac{\frac{1}{2}\mu_n C_{ox}(W/L)_2(V_{GS2}-V_{th})^2}{\frac{1}{2}\mu_n C_{ox}(W/L)_1(V_{GS1}-V_{th})^2} = \frac{(W/L)_2}{(W/L)_1} = \frac{N_{ch2}}{N_{ch1}}, \quad (2)$$

where μ_n is electron mobility in silicon and C_{ox} is the channel oxide capacitance per unit area. In (2), μ_n is material parameter and C_{ox}, L as well as V_{th} are decided by the process, while the circuit ensures that $V_{GS1} = V_{GS2}$. Hence, the ratio of N_{ch}, equal to the width ratio, of M_2 and M_1 decides the magnitude of I_o / I_{REF}. The topology of CM w/ and w/o MSW S/D is revealed in Figs. 4(b) and (c), placing M_2 on the top of M_1. Source regions of M_1 and M_2 are connected directly as the GND region. We number the channels from the bottom to the top, including one channel for M_1 (fixed here in this work) and various number of channels for M_2. Figs. 4(d) and (e) are 2D lateral views of CM w/o and w/ MSW S/D, respectively.

III. Results and Discussion

Fig. 5 shows the electrostatic potential distribution along the Z-axis in the GND and OUT regions, respectively, when V_{OUT} equals to V_{REF} of the ideal case. Having higher potential in GND region or lower potential in OUT region indicates that the voltage drop between the channels is lower, which reduces I_o. For the CM w/o MSW S/D, the potential changes significantly with the height of device since the parasitic resistance of S/D is large. This phenomenon is especially significant for the devices of CM with larger N_{ch2}. For example, the potential at the third channel of the case of N_{ch2} = 7 is higher than that of the case of N_{ch2} = 3. Potential difference of the devices in the CM w/ MSW S/D is a lot lower than that of the CM w/o MSW S/D. In particular, potential difference in the OUT region of different N_{ch2} is identical. The result supports that the structure of MSW S/D effectively suppresses the potential difference in both regions. Fig. 6 shows the output characteristics of CM. The ideal value is given by the result of pre-sim composed of single-channel devices. The devices of CM w/o MSW S/D suffer from the parasitic effect and the I_o is far from the ideal case, while the devices of CM w/ MSW S/D almost reach the ideal I_o when N_{ch2} < 7. Fig. 7 compares I_o and r_o, the incremental output resistance, of the CM w/ and w/o MSW S/D with the ideal case at V_{OUT} = V_{REF} = 0.6092 V. The I_o of CM w/o MSW S/D saturates with

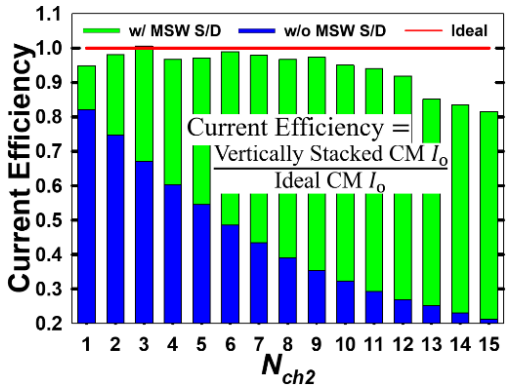

Fig. 8. Current efficiency of the channels versus N_{ch2} when $V_{OUT} = V_{REF, Ideal}$. Notably, the current efficiency of CM w/o MSW S/D is away from the ideal value when the N_{ch2} increases.

N_{ch2} and fails to remain linear to N_{ch2} because of the potential drop in S/D region. The CM w/ MSW S/D has I_o proportional to N_{ch2} when $N_{ch2} < 7$. For a larger N_{ch2}, I_o of CM starts to drop from the ideal case even with MSW S/D because MSW cannot reduce potential drop well enough to maintain the ideality. In the circuit diagram, M_2 channels are parallel with each other, leading to the inversely proportional trend of r_o and N_{ch2}. Parasitic effect increases the r_o of devices w/o MSW S/D in the CM circuit, and MSW S/D suppresses parasitic resistance well when N_{ch2} is large, making r_o of the devices w/ MSW S/D in the CM circuit matches the ideal case.

Fig. 8 discloses the current efficiency of output channels versus N_{ch2} at $V_{OUT} = 0.6092$ V. The devices of CM circuit w/o MSW S/D do not have high current efficiency even when $N_{ch2} = 1$, which affected by the parasitic effect the least. For the devices of CM w/ MSW S/D, the current efficiency reaches the ideal level with marginal error from numerical calculation, but the current efficiency starts to drop when N_{ch2} increases. Notably, the simulation and analyzing results discussed here can be employed for exploring the cascode CM formed by GAA devices w/ MSW S/D accordingly. No matter how, to further stabilize I_o of the CM circuit, more robust GAA device design should be addressed.

IV. Conclusion

In summary, we have studied output characteristics of vertically stacked GAA Si MOSFETs based CM circuit. The vertically stacked GAA Si NS MOSFETs w/ and w/o MSW S/D have been explored to assess the circuit performance. Parasitic resistance of S/D results in the significant potential difference in a single node of the CM circuit, taking its toll on the circuit performance of CM. The explored devices of CM w/ MSW S/D have shown their immunity to parasitic resistance of S/D when N_{ch2} increases up to seven, which is a suitable N_{ch2} having r_o matches the ideal case and maximized I_o without losing proportional relation between I_o and N_{ch2}.

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