DTCO of advanced FDSOI CMOS technology by process emulation

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***Abstract*—this paper presents a methodology of DTCO (Design-Technology Co-Optimization) for advanced FDSOI CMOS technology based on process emulation. By combining process emulation for the generation of 3D structures, TCAD and SPICE simulations, integrated circuit (IC) performance can be estimated. This work, based on realistic devices taking into account integration flow and interconnects topologies (multilayer dielectrics, contact etching form, etc.) offers a large range of technological and device parameters study. We illustrate the interest of this approach by specifically studying the effect of interconnect oxides permittivity on the performance of a ring oscillator (RO).**

Keywords: Virtual integration, Ring Oscillator, Parasitic capacitances extraction.

I. Introduction

Since decades, the MOSFET scaling offered performance enhancements and increase of transistor density, but short channel effects became the limiting factor for bulk MOSFETs devices. In the semiconductor industry, the introduction of FinFET [1] or FDSOI [2] technologies was the answer to this bottleneck. However, in order to scale FDSOI devices [3] down to 10 nm technology node and below, the need to set up a performance analysis is mandatory. Establishing a Process Design Kit (PDK) and utilizing extraction tools, even for a basic circuit like the ring oscillator RO, is crucial. This involves the use of a complete suite of CAD tools including Parametrized cells (Pcells), Layout Versus Schematic tool (LVS), Parasitic EXtraction (PEX). For DTCO, these tools require a significant and complex programming effort. This involves developing sophisticated algorithms and scripts to automate and optimize various aspects of the design and verification process. Our work introduces a simpler approach that operates without the need for a complete integrated circuit (IC) design environment. This methodology relies on dedicated simple circuits such as RO and it starts from layout file and chains virtual integration, TCAD and SPICE simulations (Fig. 1). The capability of this method is illustrated by the evaluation of the impact of interconnections properties on RO performance. By integrating circuit design with process optimization and utilizing a comprehensive suite of CAD tools, we can analyze and enhance the performance of the RO with a particular focus on its interconnections.

In this paper in section II, we focus on the process emulation itself through structure description and layout of RO. Then, in section III, we detail transistor specification relative to 10nm FDSOI node. Finally, we describe the parasitic extraction and the corresponding RO performances by modifying CESL, inter metal and via dielectrics permittivity.

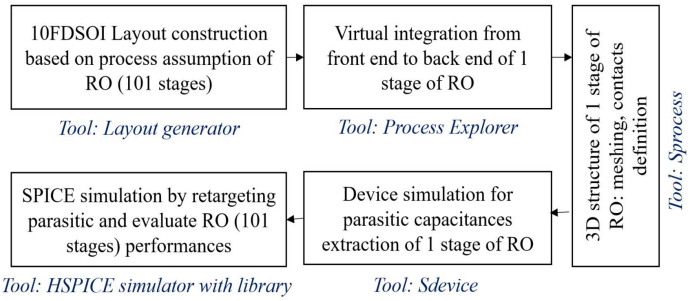

Fig. 1. Main steps of the proposed methodology

II. Process Emulation for Integrated Circuit Simulation

A. Structure description

The ring oscillator is used to benchmark the performance of the FDSOI devices down to 10 nm technology node and below. The circuit is composed of 101 stages. The fan-out number is 4

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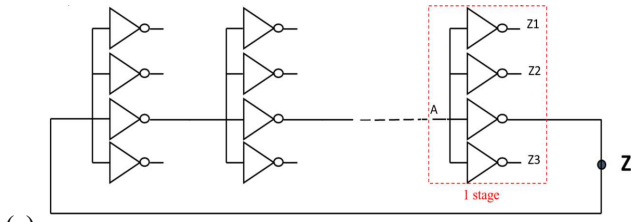
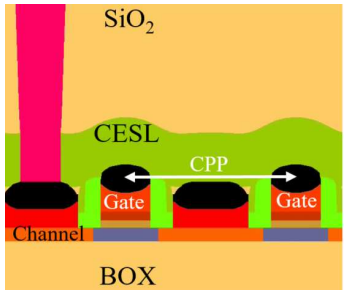
corresponding to 3 parallel inverters placed on each stage with an open output (Fig. 2a).

The sizing of N and P transistors was the nominal L equal to 20 nm. The Contact Poly Pitch (CPP, see Fig 2.b) and the metal 1 & 2 (M1/M2) pitch are 68nm and 48nm, respectively. The instance parameters of the MOSFET models are configured to include parasitic capacitances induced by the (middle-of-line) MOL and (back-end-of-line) BEOL level.

In this work, the goal is to develop DTCO methodology described in Fig. 1 to evaluate the contribution of contacts and interconnects on the performance of RO by using CAD tools.



(a)



(b)

Fig. 2. (a) Schematic of ring oscillator with 101 stages of inverters, (b) main process information relative to 10FDSOI technology.

B. 101-stage ring oscillator layout

Following the main steps, we start with the layout of the 101-stage ring oscillator as illustrated in Figure 3. Initially, the Design Rules Check (DRC) is applied to the layout to ensure that it complies with the guidelines specified in the Design Rule Manual (DRM) for 10nm FDSOI technology. This verification step is crucial as it ensures that the layout adheres to the manufacturing constraints and design standards necessary for the successful fabrication of the circuit.

From this layout, one RO stage is extracted to perform the virtual process flow as succinctly described by Fig 4, by using Synopsys' Sentaurus Process Explorer (PE) [4].

C. Process emulation of one stage ring oscillator

Virtual integration provides the ability to create detailed three-dimensional (3D) representations of structures and circuits. It also allows testing and verifying the geometric feasibility of new technologies before moving on to the manufacturing phase. In addition, virtual integration plays a fundamental role in parasitics extraction (PEX) and more broadly in Design Technology Co-Optimization (DTCO).

In this work, we simplified the process integration flow to efficiently generate 3D structures from layouts while adhering to process assumptions. This flow is dedicated to parasitic capacitances extraction (PEX) where there is no need for SADP by simplifying the etching steps.

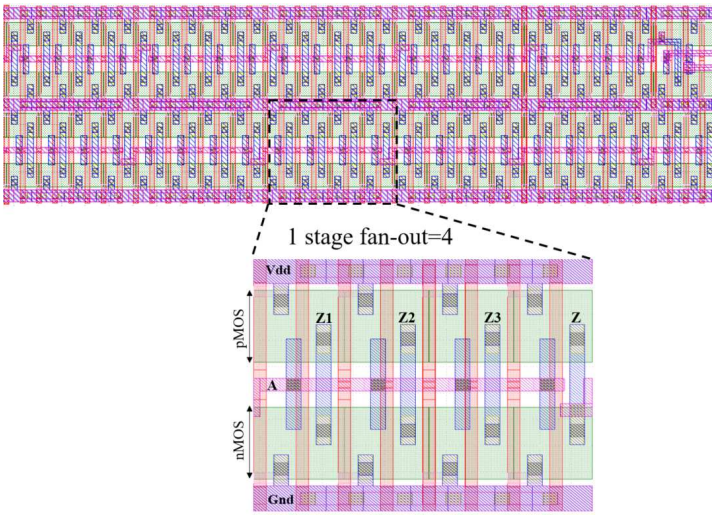


Fig. 3. Layout view of RO with 101 stages of inverters with fan-out 4

The Z cut of the 3D structure of one stage of the RO circuit is presented in Fig. 6b and 6c, with the different layers annotated (M1 & M2: metal levels, R0 and V1: via metals). This structure (Fig 6.a) is generated using the layout and process flow described above. It illustrates the high-fidelity topographical 3D transistors structures unlike the standard PEX tools that generate rectangular geometries (2.5 D) [5]. Therefore, with realistic geometries, the parasitic capacitances of the BEOL and MOL can be calculated more precisely.

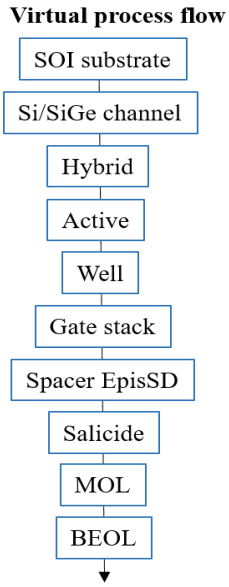


Fig. 4. Simplified virtual process flow

D. TCAD simulation of one stage ring oscillator

The generated 3D structure is imported into Synopsys' Sentaurus Process [6] in order to build a suitable mesh to carry out electrical simulations. The mesh contains around 4.6 million of points.

In order to simulate and analyze the effects of parasitic capacitances in the circuit, the one stage of RO structure is summarized only by contacts (metals) and insulators.

Therefore, M1/M2 interconnects, silicide domains, gate stack polysilicon and epitaxial source/drain domains are considered as perfect conductors. Following that, the contacts are arranged through a recursive procedure, to connect to same contact the entire "conductor" region touching M2. Fig. 6.b and 6.c illustrate the final structure that is composed of seven nodes: stage input (A), ground (INHGND), supplied voltage (INHVDD), inverters outputs (Z1, Z2, and Z3) and stage output (Z).

III. Case Study: Advanced FDSOI CMOS

A. Transistor specifications

The initial process assumptions are based on previous FDSOI developments including mechanical stress mobility boosters [3, 7]. In view of 10nm node, the devices are optimized by TCAD simulation and using the carrier transport properties from hardware. As the gate length is reduced down to 20nm, the equivalent gate oxide and the film thickness are chosen to be 0.8nm and 5.5nm, respectively for limiting short channel effects. For evaluation at circuit level, a model library, based on these assumptions, was generated by using L-UTSOI compact model [8]. Generally, we used SPICE (Simulation Program with Integrated Circuit Emphasis) tools to simulate parasitic effects in integrated circuits. SPICE allows designers to define the electrical characteristics of transistors. Fig. 5 shows the IV characteristics of nMOS (nFET) and pMOS (pFET) transistors.

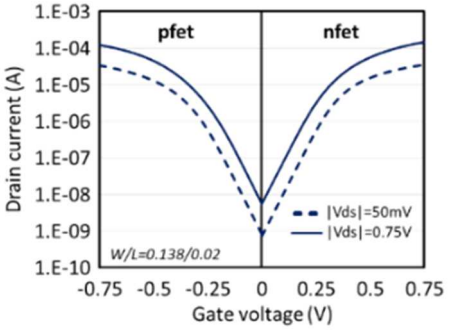


Fig. 5. HSPICE simulation of Id(Vg) curves for nFET and pFET

B. Interconnects parasitic capacitance extraction

Once the structure has been simulated, Sentaurus Device from Synopsys [9] is used to simulate the electrical behavior of interconnects. Consequently, parasitic capacitances which is one of the most important impact on the transistor delay, are extracted from BEOL and MOL.

To remove intrinsic parasitic capacitances and currents, the contributions from the channel MOS transistors in our generated structure are removed and replaced by SPICE model for the RO simulations. Therefore, in this case, we include just the contribution of contacts and interconnects in the technology benchmarking. To this end, the permittivity of the spacers, gate stack oxides, buried oxide, shallow trench isolation oxides and that of the channel of MOSFET replaced by insulator are set to zero (Fig. c).

In addition, as the structure is composed of only metals and insulators, there is no need to solve the semiconductors equations but only the Poisson's equation. The metals are not included in the resolution; their interfaces with insulators define the fixed potential boundary conditions. In addition, a small-signal AC analysis is performed to extract the total capacitances between nodes.

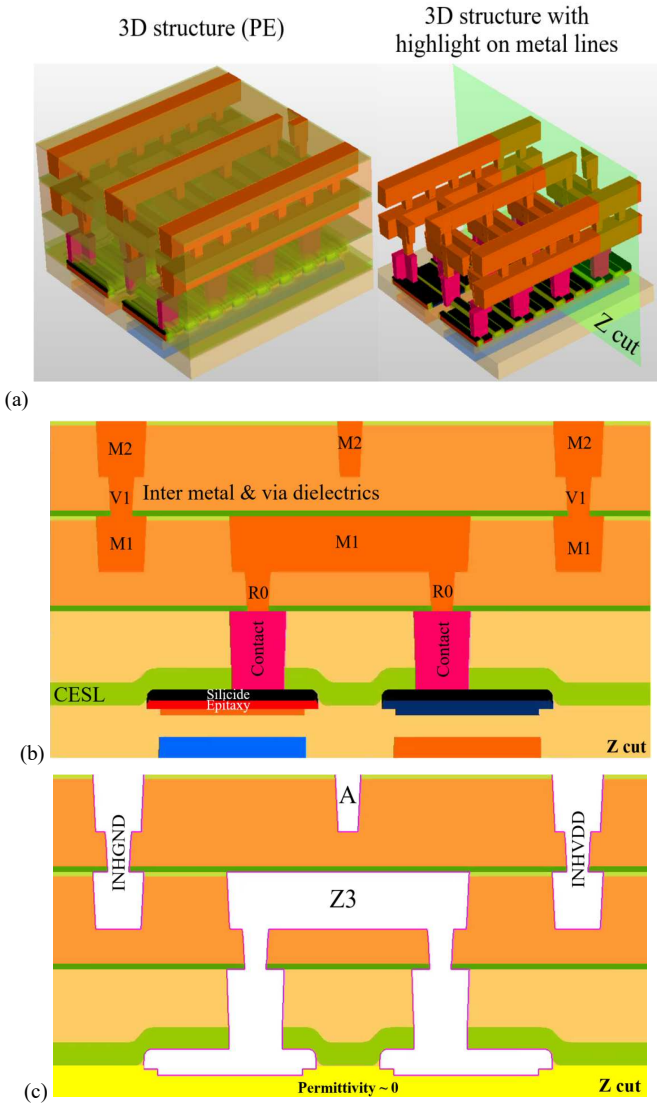


Fig. 6. From Process Explorer to access contacts area and BEOL M1/M2 definition and meshing: (a) 3D structure, (b, c) cut 2D of structures before and after contacts area and M1/M2 definition.

A complete capacitance matrix between the seven contacts is obtained. However, by considering the capacitance reciprocity, only 21 capacitances are identified for SPICE simulation of RO. Despite the high number of mesh points, we could use the Pardiso solver, which proved more accurate. The CPU time is 1h17mn for simulations running on 8 Intel(R) Xeon(R) Gold 5218R processors.

C. Evaluation of ring oscillator performance

We coupled our capacitances extraction methodology to the simulation of ring oscillator with 101 stages using SPICE model library. Through this simulation, we can analyze the impact of parasitic capacitances on circuit performance metrics such as frequency and power consumption. This analysis helps in

identifying potential design improvements to minimize parasitic effects and optimize overall circuit performance.

First simulations are done with and without contribution of the contacts and the interconnects. Fig. 7 summarizes a comparaison between these two simulations. These simulations are done by sweeping the supply voltages Vdd from 0.5V to 0.75V. At a fix Vdd of 0.75V, the decrease of RO frequency with parasitic interconnections is about 38% highlighting the significant impact of interconnects. That explains that the capacitance with interconnects becomes higher which leads to lower performance.

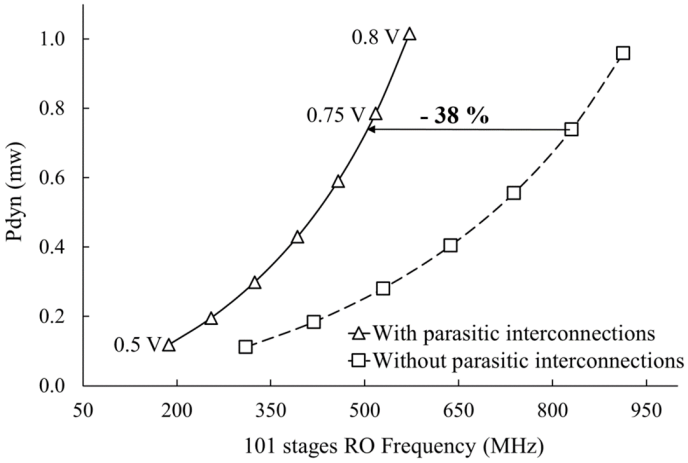


Fig. 7. Power consumption (Pdyn) versus frequency of 101-stage RO with and without interconnections for different Vdd.

Thanks to this approach, we studied the effect of interconnect oxides permittivity on the performances of RO. The impact of the CESL permittivity, inter metal and via dielectrics is estimated. For example, in Fig. 8, we observe that at a same thickness, the CESL permittivity has a significant impact on the RO frequency as compared to inter metal and via dielectrics. By reducing the permittivity value of CESL from 7.5 to 3.5 and keeping the permittivity of Inter metal and via dielectrics at 3.1, the circuit performance can be increased by 11%.

Thanks to this methodology, we can systematically refine and optimize various process assumptions to enhance circuit performance while aligning with the capabilities of the manufacturing process, focusing particularly on Design Technology Co-Optimization (DTCO) aspects. This approach involves a detailed analysis and adjustment of fabrication parameters such as lithography, etching, and material properties to achieve specific performance goals. By leveraging advanced simulation tools and iterative design cycles, engineers can explore different process scenarios, assess their impact on circuit performance metrics (such as speed, power consumption, and reliability), and iteratively refine the design to achieve optimal results.

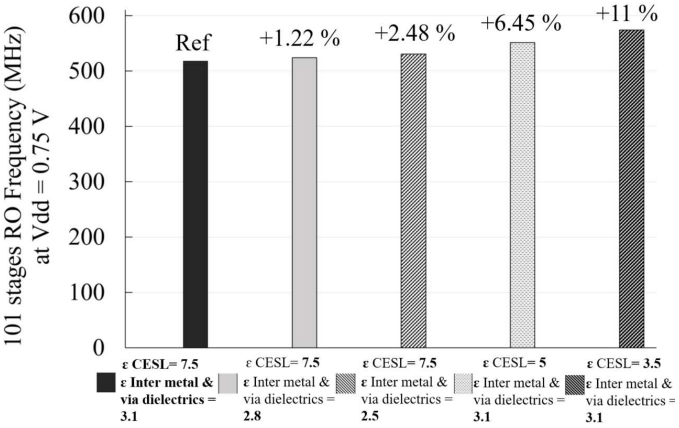


Fig. 8. Impact of permittivity of CESL, inter metal and via dielectrics on RO performances.

IV. Conclusions

In this work, we propose a complete flow for DTCO approach by combining process emulation, TCAD simulation of interconnects contributions and SPICE simulations. The effectiveness of this approach is demonstrated using a first set of 10nm FDSOI process assumptions to analyze 101-stage ring oscillator performances. This example demonstrates that by integrating circuit design with process optimization capabilities, we can enhance overall circuit performance, including improvements in speed and power consumption. This integrated approach not only boosts performance but also addresses the growing need for energy-efficient solutions in modern electronics. Thus, the synergy between circuit design and process optimization paves the way for significant advancements in the field.

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