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D2D Variation Aware DTCO for Novel Vertical a-IGZO-FETs in Large-Scale M3D 2T0C DRAM Bit Cell Evaluation via Statistical Modeling Methodology

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***Abstract*—Device nonuniformity of ultra-scaled novel vertical a-IGZO-FETs is induced by multi-sources, such as dimension variation and material disorder, limiting large-scale DRAM design. Particularly, fluctuation of disorders in an amorphous channel exhibits a great impact on density of states (DOS) contributing to statistical effects on gate controllability and transport mechanisms. To clarify this issue, TCAD simulations are conducted by adjusting geometric dimensions and DOS, and corresponding statistical characteristics (e.g., on-voltage and on-current etc.) are extracted from up to 80 samples of down to channel length of 50nm. Such effects are further incorporated into a surface-potential based physics compact model via calibration to experiments. Using this model, the vertical a-IGZO-FET-based 2T0C DRAM is firstly investigated with the statistical analysis of Write/Read performances, supporting device variation aware DTCO flow of future extremely large-scale and high-density M3D memory.**

Keywords—Channel-all-around, IGZO, Statistical Model

I. Introduction

Novel vertical (Channel-All-Around, CAA) a-IGZO-based FETs support capacitor-less DRAM beyond $4F^2$ through monolithic stacking [1], as shown in **Fig. 1**. In terms of higher-density requirement, the trend of scaling [2, 3] contributes to critical device uniformity issues in a-IGZO devices sensitive to variations of geometric dimension and material disorder, exhibiting limitation to large-scale of DRAM design. Consequently, underlying mechanisms of statistical effects demand further exploration for reliability-aware DRAM design. In this work, performances of novel vertical FET are simulated by TCAD with critical effects of gate-contact-overlapping, localized state distribution and scaling etc., and thus the relationship between physics-based parameters and characteristics is explored. Furthermore, key statistical features are extracted from multi-samples and facilitate device to device (D2D) variation analysis. With incorporation of device-level nonuniformity, the surface-potential based compact model is further calibrated to experiments; statistical effects on write and read performance of 2T0C DRAM cells can be explored in awareness of D2D variations supporting Design Technology Co-Optimization (DTCO) flow.

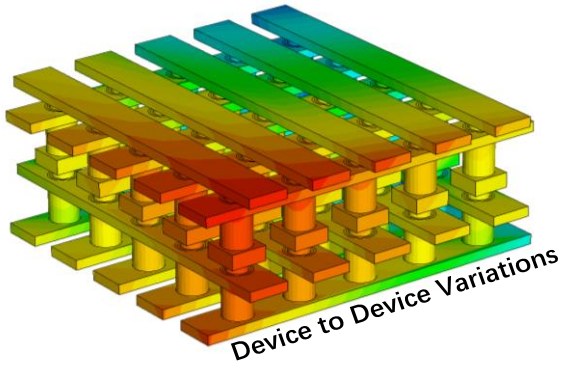


Fig. 1. 3D structure of $4F^2$-per-bit capacitor-less DRAM array with D2D variations.

II. Dominated Variation Sources

Fig. 2 demonstrates the 2T0C DRAM array diagram and semi-cross-section of CAA-IGZO-FET. Lengths of the overlap regions along the channel direction of the top and bottom electrodes and gate are defined as ΔContact and Depth, respectively. To better study performance variation source, a 3D TCAD device model is established with IGZO material properties. **Fig. 3** shows a TCAD-fitted experimental transfer curve when drain voltage is 1 V, which is mainly achieved by controlling DOS parameters such as tail acceptor-like states, tail

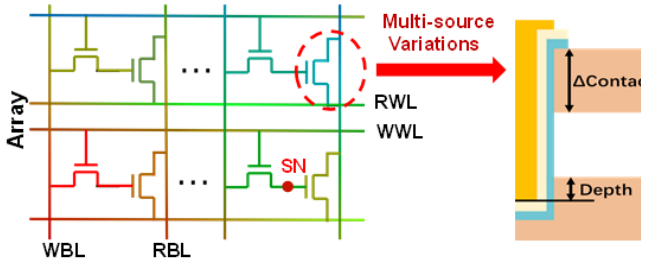


Fig. 2. 2T0C DRAM array diagram and semi-cross-section of CAA-IGZO-FET. ΔContact (Depth) represents the overlap area between top (bottom) electrode and gate, which is a probable source of device performance variation.

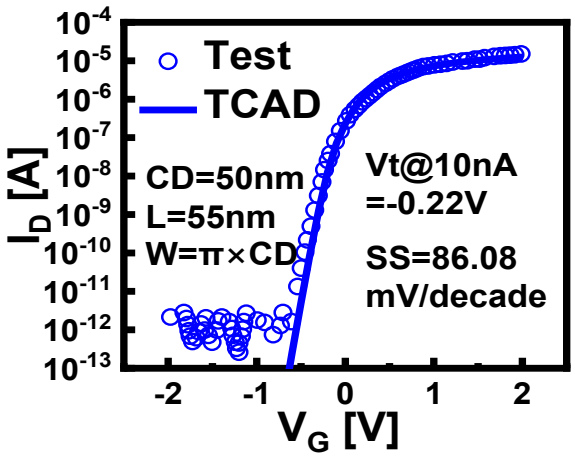
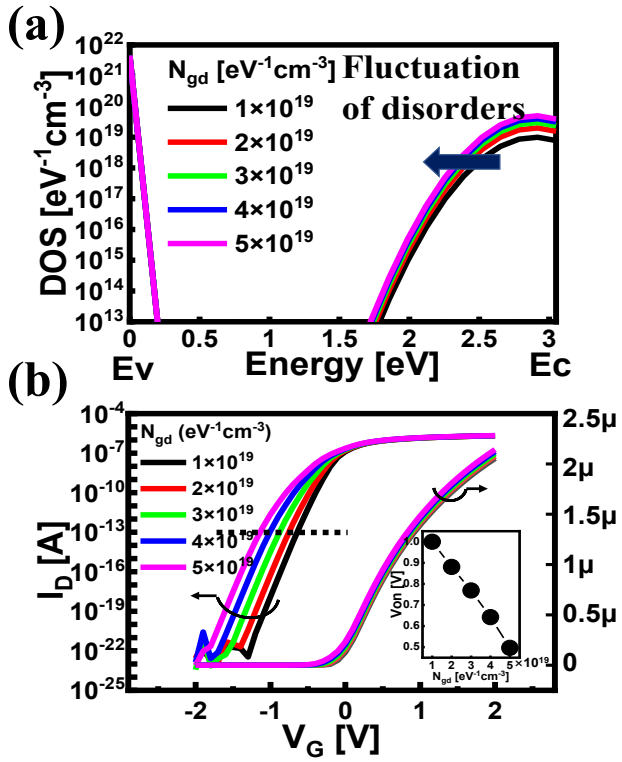


Fig. 3. TCAD Simulation calibration to experiments for CAA a-IGZO FETs with V_{ds} = 1 V and L= 50 nm.

donor-like states, Gauss acceptor-like states, and Gauss donor-like states in amorphous material [4].

During fitting this transfer curve, density of Gauss donor-like states (N_{gd}) contributes to an obvious effect on performances such as a bad subthreshold slope and negative-shift V_t as shown in **Fig. 4(a)** and **Fig. 4(b)**. Moreover, the impact of dimension factor like gate-contact overlap on device performance, and the corresponding simulation results are depicted in **Fig. 4(c) (d)**. A longer overlap area between gate and contact means a reduced series resistance for electrodes, leading an increased drain current. Variation around sub-threshold primarily results from DOS distribution, whereas above-threshold variation source is mainly from geometric dimensions such as gate-contact overlap.



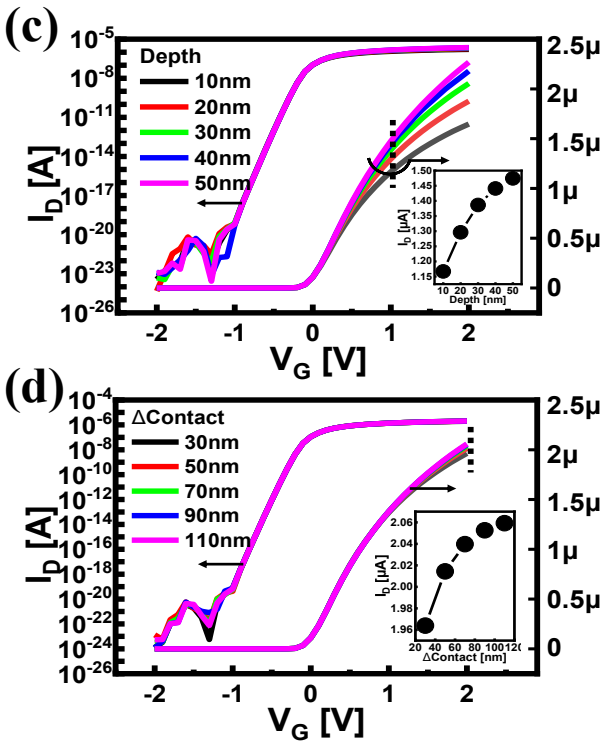


Fig. 4. (a) Gauss donor-like states distribution in IGZO material. (b) Transfer curves under N_{gd} from 1×10^{19} to 5×10^{19} $eV^{-1}cm^{-3}$. The increase of N_{gd} induce negative shift of V_t and degradation of the subthreshold slope. Transfer curves under (c) depth from 10nm to 50nm and (d) ΔContact from 30nm to 110nm. As the length increases, the on-state current becomes larger.

III. Statistical Modeling

Key device features indicated in TCAD simulations, such as threshold voltage and on-current, are extracted from multiple sets of experimental data. And the coverage range of its process corner is determined. Furthermore, a statistical model has been developed to describe the process deviation between different wafers to take the fabrication nonuniformity into consideration for design. On the basis of introducing device-level nonuniformity, several sets of experimental data are used to calibrate and corner the novel CAA IGZO FETs compact model based on surface potential which is shown in **Fig. 5(a) and (b)** [5]. It can be clearly observed that the subthreshold characteristics and on-state current both vary significantly from device to device. Besides, the modulated model is simulated by using Monte Carlo statistics, incorporating the main disorder parameters characteristic temperature T_0, trap density N_t determining DOS, based on variable range hopping (VHR) and percolation with the finite-size effects of mobility [6]. **Fig. 6(a-d)** shows statistical characteristics of compact model data after Monte Carlo simulation. It can be seen that the distribution data is relatively concentrated within the process corner range from FF(Fast) to SS(Slow), presenting the Gauss distribution. Based on the above simulations, the variation of the devices can be well incorporated into the model and used for circuit evaluation. Subsequent circuit simulations demonstrate that D2D variation influences the performance of 2T0C DRAM Bit cell to some degree.

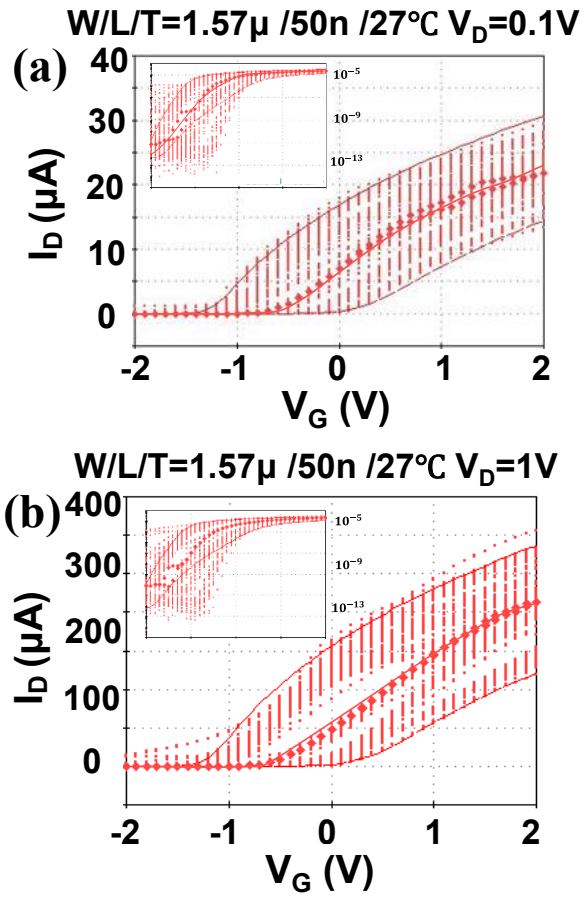
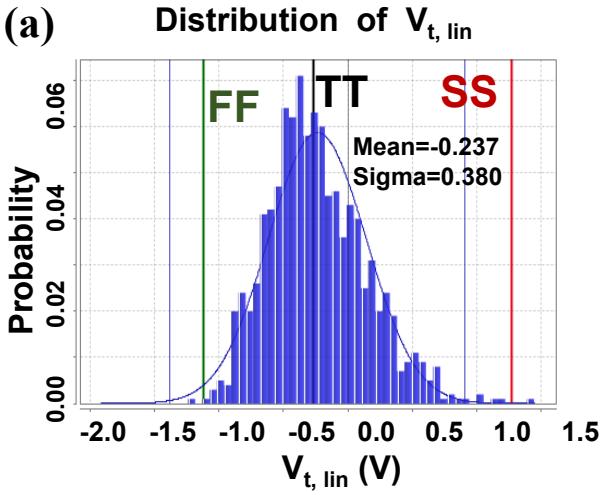


Fig. 5. Experimental data of 80 groups of CAA IGZO FETs transfer characteristic curves at V_D = 0.1V (a) and 1V (b). The inserts show I_D on logarithmic coordinates. Both subthreshold characteristics and on-state current vary significantly from device to device. Red lines represent statistical compact model fitting results. The upper line is the calibrated result of FF, the lower one is SS, and the middle one is a typical case.



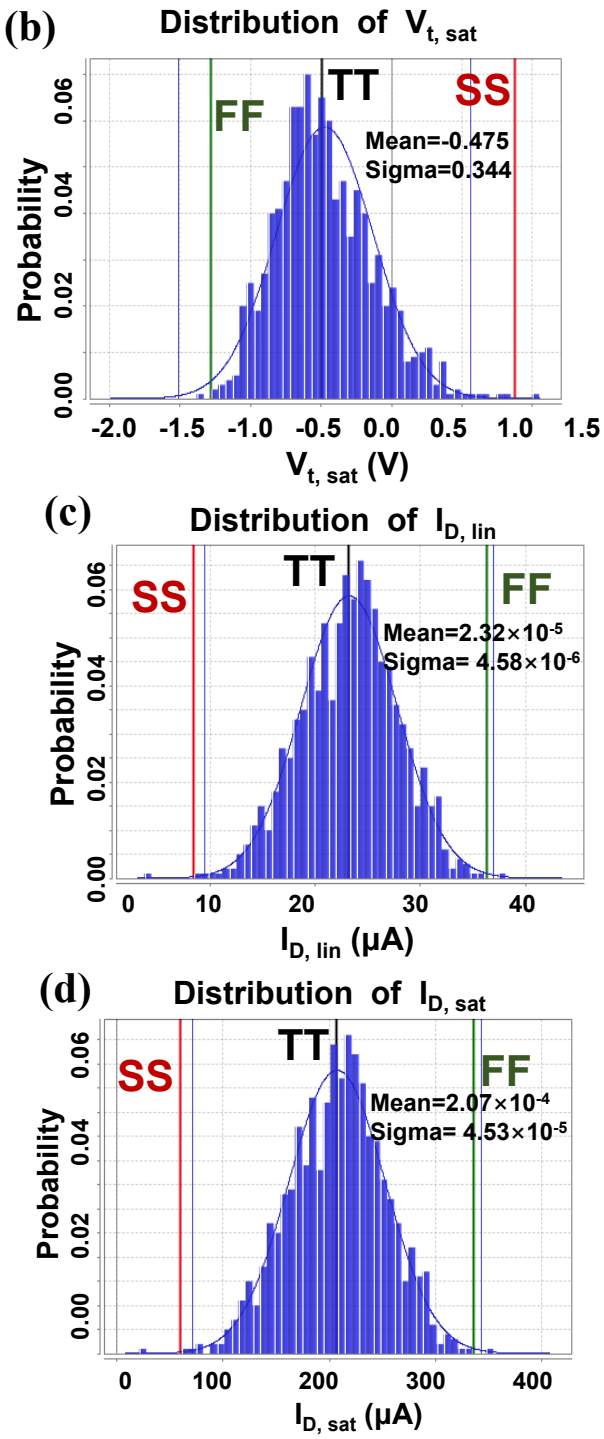
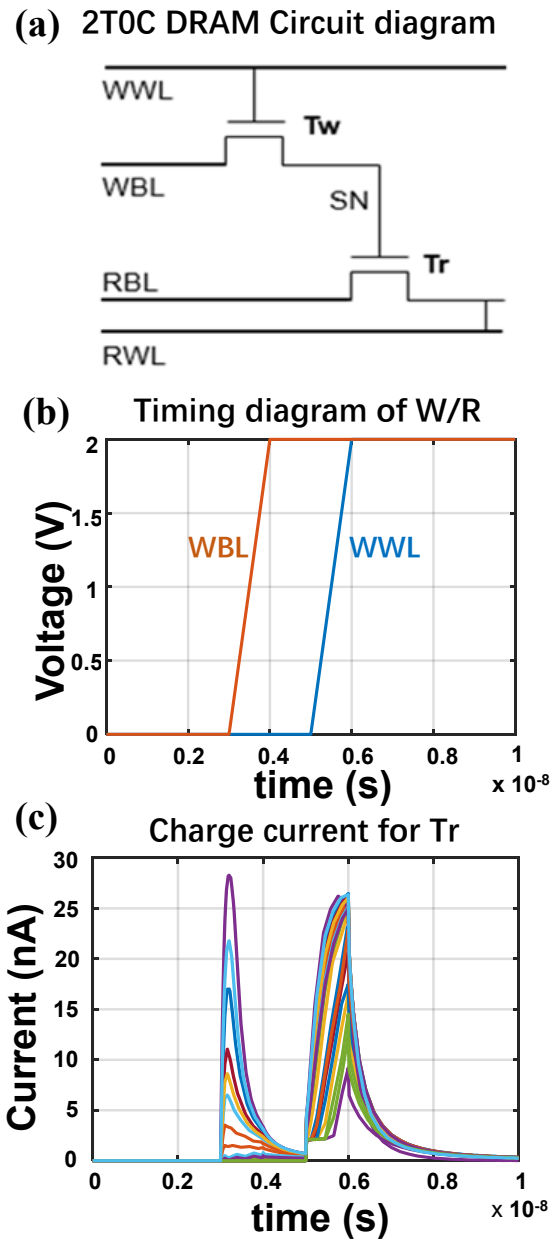


Fig. 6. Statistical characteristics of the compact model data for $V_{t, lin}$ (a), $V_{t, sat}$ (b), $I_{D, lin}$ (c) and $I_{D, sat}$ (d) by using Monte Carlo simulation. The corners of the experimental data FF-TT-SS are covered within the distribution range. Based on these simulations, the variation of devices can be well incorporated into the model and used for circuit evaluation.

IV. Circuit Evaluation

Fig. 7(a) illustrates the schematic diagram of 2T0C DRAM cell based on CAA FETs. In such cells, the gate capacitor of the read-transistor is regarded as a storage node (C_{SN}). WBL charges

the SN through the write-transistor (Tw) during write operation. During read operation, the charge stored in SN is released due to leakage of Tw. Benefiting from the extremely low leakage current of IGZO devices, such a DRAM cell can typically achieve a retention time of hundreds of seconds after a single charge, greatly reducing the power consumption required for refreshing the SN. The timing diagram of write and read operation is shown in **Fig. 7(b)**. Using the compact model which elaborates above to simulate a write/read cycle of 2T0C DRAM bit cell in the way of Monte-Carlo modeling methodology, statistical analysis of Write/Read performances. As shown in **Fig. 7(c)**, I_D values of the Tw range from 61nA to 265nA when both WWL and WBL signals are high, resulting in fluctuations of the charging time for the SN. SN voltages also vary from 195mV to 1.72V due to the V_t variation of Tw (**Fig. 7(d)**). Meanwhile, considering the variations in V_t and I_D of Tr, the performance of DRAM cell will be extremely uncontrollable,



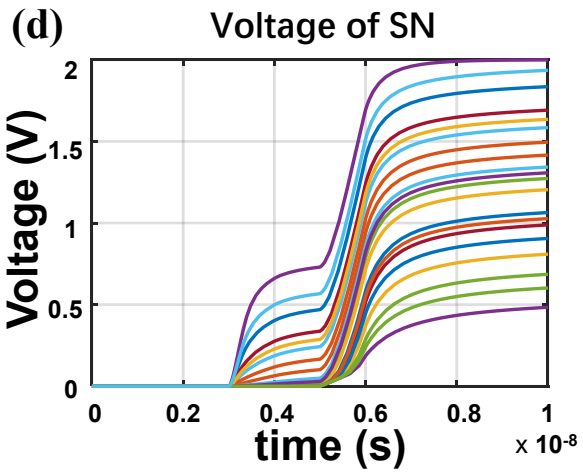


Fig. 7. (a) Circuit diagram of the CAA-IGZO-FET-based 2T0C DRAM (W = 1570nm, L = 50nm). (b) WWL and WBL timing diagram of write and read operation. (c) Simulations of charge current for the read transistor (Tr) using 20 sample points Monte Carlo simulation analysis method. Statistical analysis results show that the currents range between 61nA and 265nA. (d) V_{SN} varies from 195mV to 1.72V. The simulation results indicate that the D2D variation significantly impacts the performance metrics of 2T0C DRAM cells.

resulting in misreading of stored data. These results validate the adverse impact of D2D on 2T0C DRAM performance and operation.

V. Conclusion

Device nonuniformity issue of novel CAA-IGZO-FETs is successfully explored for large-scale and high-density DRAM applications. As device performance strongly correlated with DOS and contact overlapping properties, TCAD simulations are conducted for parametric analysis. Key statistical features are then extracted from experiments, and the compact model is further calibrated for Write/Read evaluation of the 2T0C DRAM, supporting the variation-aware DTCO flow in terms of D2D for large-scale BEOL-compatible 3D integration.

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