Cryogenic Modeling of 22nm FDSOI MOSFET

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***Abstract*—In this work, we introduce a TCAD modeling approach for 22nm ultra-thin body and buried oxide fully depleted silicon on insulator (UTBB-FDSOI) MOSFETs, tailored to operate at cryogenic temperatures ranging from 300 K down to 4.5 K. Incorporating relevant physical effects, this TCAD model is calibrated using experimental data from a test vehicle. On-chip bootstrapping is employed to mitigate leakage currents from the device test arrays, ensuring precise low current measurements (in the order of a few nA). Our results provide insight in the behaviour of the threshold voltage, subthreshold swing, and back gate bias effect at cryogenic temperatures, offering valuable guidance for low-power circuits and quantum computing readout IC design.**

***Index Terms*—Device modeling, cryogenic, UT-FDSOI MOSFET, quantum computing**

I. Introduction

The growing interest in quantum computing requires qubits and readout circuits that operate at cryogenic temperatures,(CT) down to 4 K [1] and below. In order to predict and optimize the behavior of analog and digital circuits, it is important to understand the behavior of devices at CT [2] [3] [4]. For the metal–oxide–semiconductor field-effect transistor (MOSFET) operating at CT, the subthreshold swing reduces, the threshold voltage increases, and its cut-off ratio is improved when MOSFETs are used for digital and analog circuits [5].

However, limited papers are dealing with the TCAD model of MOSFETs at CT. The related incomplete ionization and mobility models are calibrated for bulk CMOS technology at CT [10] [11]. Similarly, for FDSOI MOSFETs, some physical phenomena and theories should be considered in the TCAD model, and also some effects occurring at temperatures below 70 K are still unknown. Considering the effects below 70 K, the freeze-out effect is dominating, causing the active electrons or holes to decrease drastically under the low electric field [6]. The freeze-out effect describes two aspects: (i) incomplete dopant ionization and (ii) bandgap widening. Furthermore, the various scattering mechanisms impact the device parameters at CT: Phonon scattering, surface scattering, and lattice scattering reduce with decreasing temperature, enhancing the mobility at cryogenic temperature. Coulomb scattering is the main limitation of charge carrier mobility at CT, which is caused by the increase of interfacial trapping between the channel and gate oxide [7]. Finally, the presence of a high electric field can activate the frozen charge carriers, which can also increase the saturation current at cryogenic temperatures and improve the current on/off ratio simultaneously [11].

In this work, an accurate TCAD model for 22nm UTBB-FDSOI MOSFET is proposed that addresses convergence issues at CT and is calibrated by introducing temperature-dependent trap concentrations at CT. The PDK SPICE models were used to calibrate the initial TCAD geometries and corresponding doping concentrations at room temperature (RT), then trap concentrations are calibrated to match the I_{ds}-V_{gs} characteristics at CT by the measurement results from our bootstrapping test vehicle.

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II. Modeling and Simulation

A. Chip Design and Test Structure

A test vehicle was manufactured that features several device arrays and a diode for on-chip temperature calibration. Each array contains 400 transistors, which are arranged in rows with variable sizes W/L(160n/20n∼3200n/800n) while all devices in each row have equal sizes. Different arrays contain varying devices including LVT/RVT NFET/PFET. The architecture and layout are shown in Fig.1 and Fig.2. A bootstrapped switch compensates the leakage current from adjacent rows directing the leakage current into the drain leakage node by bootstrapping the drain input voltage. When applying the same voltage at the drain input and the drain leakage input node, the inactive rows' leakage current flows from the drain leakage input node since the voltage across the main drain switch is zero. As such, the main drain input only carries the current from the active row. The switches are controlled by a on-chip shift register. The kelvin sensing is used for calibrating the measured voltage to cancel the resistance of the wires of the test setup. The cryogenic measurement employed the CRX-4K probe station for temperature measurements ranging from 300 K to 4.5 K. The cryo-probe station and system setup are illustrated in Fig. 3.

B. TCAD Model and Simulation

UTBB-FDSOI MOSFET device structures, featuring lightly doped drains (LDD), silicon-on-insulator (SOI), and buried wells, are implemented in TCAD, while considering temperature-related physical mechanisms such as incomplete

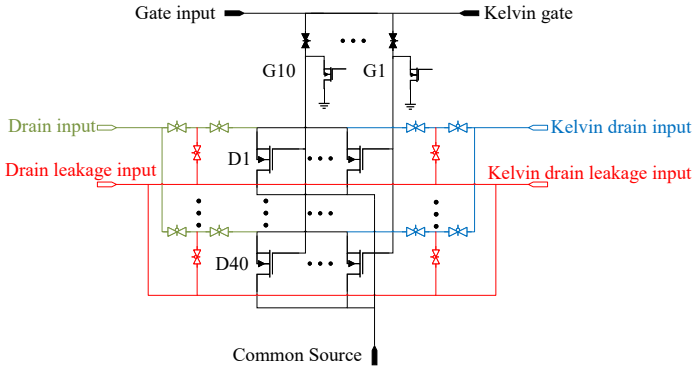

Fig. 1. The circuit schematic of the device array.

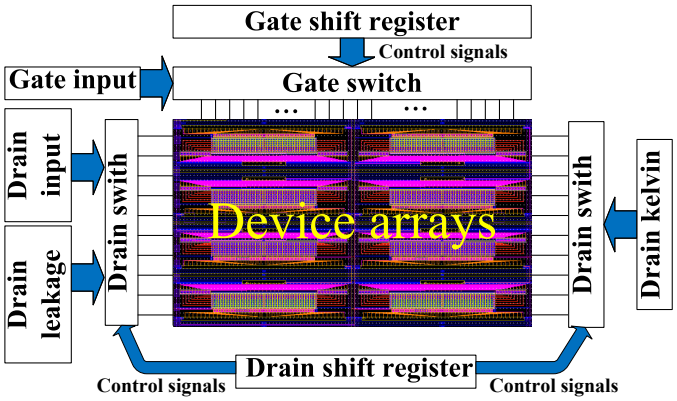

Fig. 2. The whole layout and topology structure of the device arrays.

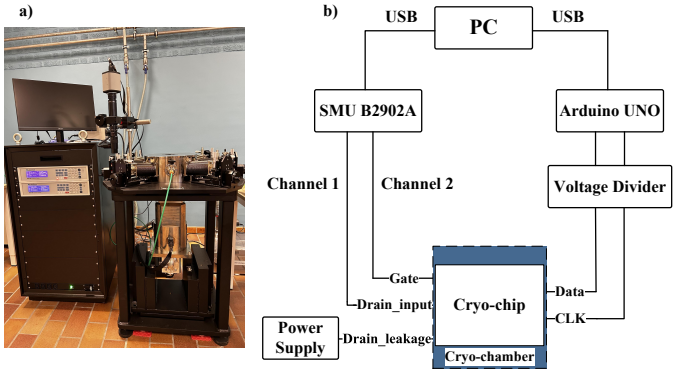

Fig. 3. The cryo-probe station and measurement system setup, a) the the CRX-4K probe station, b) the messurement setup for the device arrays chip.

ionization, scattering mechanisms, and high electric field-assisted effects [8]. However, convergence issues may lead to TCAD simulation failures due to extremely low electron/hole densities at low temperatures. The convergence problem is optimized by changing the DensLowLimit below 1E-350 and improving calculated precision in TCAD.

The Freeze-out effect is important to consider reduced electron or hole carrier densities when MOSFET work at CT. To model dopant freeze-out, the complete simulated doping

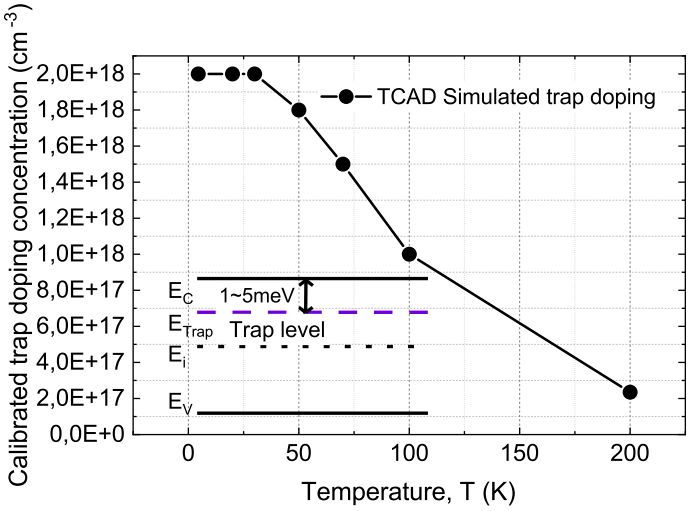

Fig. 4. Calibrated TCAD Trap doping from 300 K to 4.5 K.

concentration can be corrected as the previous research [9]:

$$N_{dop} = N^{+}_{don} + N^{0}_{don} \tag{1}$$

$$b = \frac{1}{1 + (N_{dop}/N_b)^d} \tag{2}$$

$$N^{0}_{don} = \frac{b}{1 + ge^{-(E_{Fn}+E_{dop}-E_c)/kT}} N_{dop} \tag{3}$$

N_{dop} is the total doping concentration. N^{+}_{don} is the complete ionized doping concentration. N^{0}_{don} is the frozen doping concentration that is not ionized completely. b is the fraction factor.

To model the mobility enhancement, as reported in the previous work [10], the Philips unified mobility model in (4), (5) and the Lombardi model in (6) are adjusted through the temperature coefficients θ and k to match the mobility characteristics of UTBB-FDSOI transistors at CT. The interface charge scattering model in (7) is used to constrain the mobility enhancement at CT. As such, the total mobility in the TCAD model is shown in (8). Other parameters in the below equation are default in TCAD.

$$u_{i,L} = u_{i,max} \left(\frac{T}{300K} \right)^{-\theta} \tag{4}$$

$$\theta = \theta_0 + \theta_T \left[\tanh\left(\frac{T}{T_0} \right) - 1 \right] \tag{5}$$

$$\theta_0 = 2.285, \theta_T = 0.55, T_0 = 250K$$

$$u_{ac} = \frac{B}{F_\perp} + \frac{C(N_{A,0} + N_{D,0} + N_2)/N_0)^\lambda}{F_\perp (T/300)^k} \tag{6}$$

$$u_c = \frac{u_1 (T/300)^k \left(1 + \left(\frac{c}{(N_{charge}/N)} \right)^{\eta_1} \right)}{(N_{charge}/N_0)^{\eta_2}} \tag{7}$$

$$\frac{1}{u_{total}} = \frac{1}{u_{i,L}} + \frac{1}{u_{ac}} + \frac{1}{u_c} \tag{8}$$

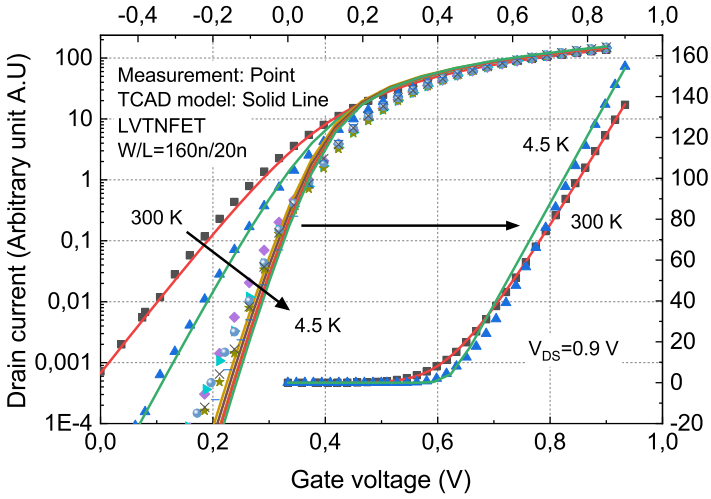

Fig. 5. The measurement results and model of Id-Vg curves for LVTNFET.

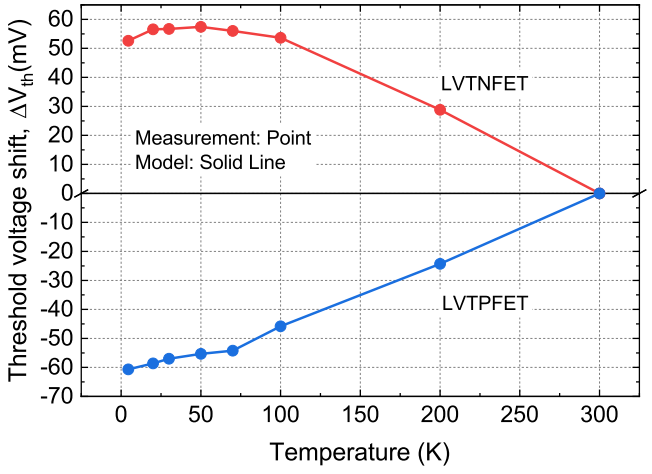

Fig. 7. The V_{th} comparing our model and measurements with temperatures.

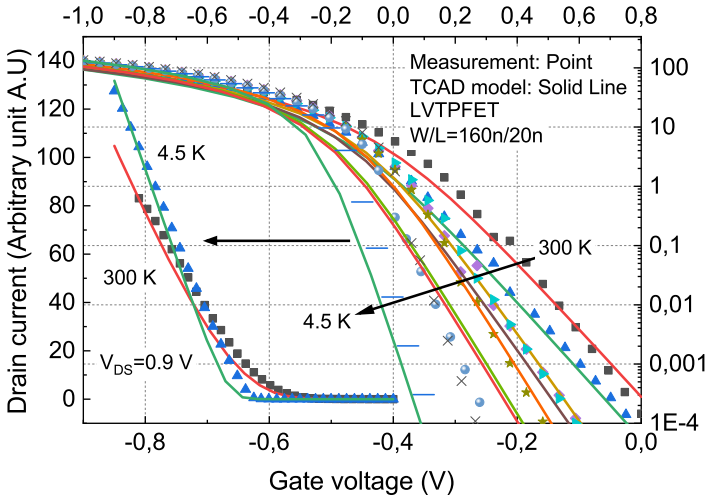

Fig. 6. The measurement results and model of Id-Vg curves for LVTPFET.

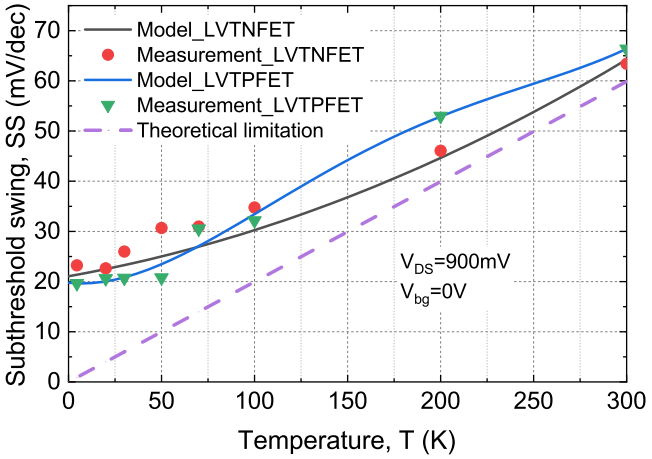

Fig. 8. The SS changes with temperatures down and could be saturated..

To model freeze-out dopant ionization at high electrical field and interface charge scattering, temperature-dependent interface trap doping is proposed which is calibrated by using the saturation current and SS extracted from the measured Id-Vg curves to match the experimental data in Fig. 4 [9]. With an increasing simulation trap charge density, the interface charge scattering will be stronger and limit the saturation current at cryogenic temperatures. The calibrated trap can also be seen as the impurity that will impact the ionization, which could cause larger SS.

Furthermore, field-assisted ionization including Poole-Frenkel ionization and tunneling is activated in TCAD to enhance the frozen donor trap ionization [11].

III. Measurement Results

For the proposed TCAD model, the I_{ds}-V_{gs} curves of NMOSFET and PMOSFET are depicted in Fig. 5 and Fig. 6, along with experimental data. It can be seen that the SS

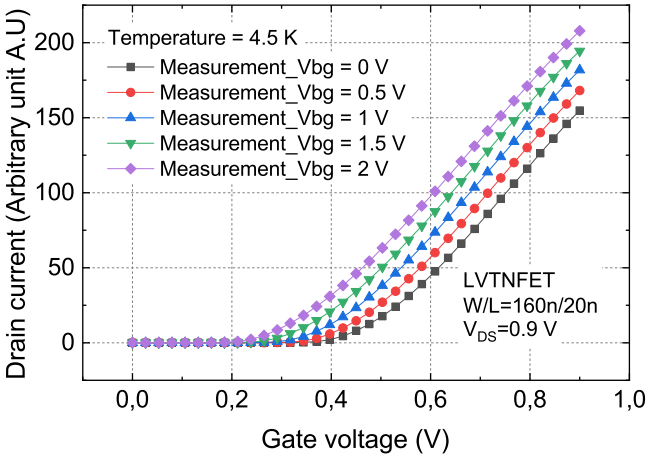

Fig. 9. The back gate effect measurement when applying back gate voltage from 0 to 2 V at 4.5 K.

decreases and threshold voltage increases as the temperature reduces. The leakage current of NMOSFET and PMOSFET at 4.5 K reduce by a factor 10^8 and 10^{12} respectively, compared to room temperature. The saturation current at 4.5 K of NMOSFET and PMOSFET becomes 1.13x and 1.26x higher than at room temperature. The extracted V_{th} shift and SS change are shown in Fig. 7 and Fig. 8. V_{th} reduces around 60 mV from 300 K to 4,5 K both for NMOSFET and PMOSFET. The SS decreases closer to 20 mV/dec when the temperature is down to 4,5 K. Measurements show that the SS saturates below 20 K compared to the theoretical limit ($\approx \ln(10)\frac{KT}{q}$), which can be attributed to crystalline disorder and trap enlargement at CT [12] [13]. The body bias measurement is shown in Fig. 9, showing that the back-gate voltage can equalize the V_{th} to room temperature values.

IV. Conclusion

The proposed TCAD model resembles the electrical characteristics of the 22nm UTBB-FDSOI MOSFET at CT and was calibrated with measurements. As the temperature descends to 4.5 K, a consistent increase in V_{th} and a decrease in SS are observed, ultimately reaching saturation. Other transistor parameters such as transconductance, off-state leakage current and transient dynamics can be extracted from our model. The back gate effect clearly demonstrated it has sufficient range to compensate V_{th} shifts at CT. The model can be used to predict the DC and transient behavior of circuit operating at CT.

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