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Chip Reliability Improvement by Designing Re-Distribution Layer (RDL) Pattern for Thermal Cycle in Wafer Level Packages (WLP)

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***Abstract*—We investigate the re-distribution layer (RDL) design effect on the Vref, the output voltage of band gap reference (BGR) circuit, during the reliability test by temperature cycling (TC). The TC failure mechanism is analyzed using TCAD simulation and verified with the experimental data. We reveal that the mechanical stress of deposited polyimide between RDL films during TC can influence the device performance. The local stress caused by RDL patterns induces the mismatch between the transistors in relations of the current mirroring in BGR circuit and the Vref can shifted. Therefore, for reliability of the chip performance in wafer level package (WLP), we should consider the position of the stress-sensitive circuits such as BGR when designing the RDL.**

Keywords— WLP, RDL, BGR, mechanical stress, thermal cycle

I. Introduction

As the feature size of IC and I/O pitch on chips continues to decrease, wafer level package (WLP) has received significant attention due to its lower costs, higher performance as well as high space efficiency [1]. The WLP not only combines the advantages of BGA and Flip Chip, but also makes it possible to manufacture, test and package on a whole wafer. The key technologies for WLP are the ball and the re-distribution layer (RDL) as a substitute for wire bonding [2]. Reliability issues related to the RDL have particularly been paid attention in the WLP [3, 4]. However, the reliability of WLP has mainly focused on the mechanical stress at the RDL pattern and its neighboring structure, such as a ball and a pad, to give rise to failures like crack and plastic damage during bonding process [5, 6]. It is well-known that the mechanical stress has a strong influence on the mobility and the current of transistors [7]. According to such a relation of stress-mobility, the mechanical stress may cause a change of a device performance from an upper BEOL structure including RDLs and balls. The band-gap reference (BGR) is used in a wide variety of integrated systems where accurate and precise voltage references with excellent line regulation and temperature-drift performance are required [8]. Since BGR plays an important role in determining the accuracy of integrated systems, designers employ different types of trimming techniques and algorithms to compensate for process variations, temperature, and complex second-order and third-order effect [9]. However, in spite of trimming technology, BGR in WLP exhibit a characteristics shift in voltage during reliability test due to plastic materials.

In this paper, we investigate the stress impact of the different RDL shapes in view of the reliable device performance in BGR circuit known as being sensitive to stress [10]. The stress source to examine the RDL impact on reliability is self-induced stress between materials (e.g. Cu and polyimide) with the different coefficient of temperature expansion (CTE) by temperature cycling (TC) instead of applying an external stress. The stress shows local variations over the chip area and changes over time or during TC [11]. The Vref by RDL shapes is measured before and after the TC reliability test, and the stress is analyzed on basis of the stress and mobility properties using TCAD simulation [12, 13]. Our work reveals that design of the RDL pattern make a change in electrical output after reliability test.

II. Approach for Simulation and Experiment

A. Piezo-resistive Effect

The mechanical stress improves or degrades the device performance by changing minority-carrier mobility due to the Piezo-resistive effect [14]. The change of the carrier mobility is extracted by using the stress and the piezo-coefficients that

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depend on the minority-carrier type, the current direction of the minority carrier-flow in channel region and the temperature. The mechanical stress effect on the device performance is assumed by the variation of the mobility. The mobility variation (MV) by the stress is calculated as

$$MV\ [\%] = S_{xx} * P_x + S_{yy} * P_y + S_{zz} * P_z \qquad (1)$$

Where S components are the stress values and P components are piezo-coefficients of silicon in x, y and z directions. Here, x, y, and z are the channel, width, and depth directions of the device, respectively.

Table 1. Piezo-coefficients of <110> channel in (100) silicon at room temperature

[%/GPa]	P_x	P_y	P_z
NMOS	**31.6**	**17.6**	**-53.4**
PMOS	**-71.8**	**66.3**	**1.1**

Table 1 shows piezo-coefficients in (100) Silicon with <110> channel orientation at room temperature [15]. In view of the x direction, the tensile and compressive stresses increase the current of NMOS and PMOS, respectively.

B. WLP Structure

The ball and under bump metal (UBM) are used in standard WLP technology similar to a typical flip chip one. The ball connects to the I/O cell through the UBM and pad structures. Because all I/O cells are difficult to be directly located under balls, the RDL has an important role to connect I/O cells and balls. As illustrated in Fig. 1, the RDL re-routes the signal path from the die peripheral I/O to the new desired bump locations and covered with the passivation of polyimide as the stress buffer.

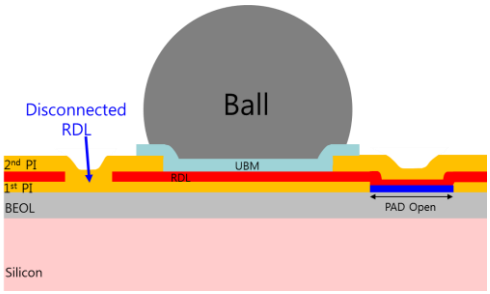

Fig. 1. The vertical structure of WLP

Table 2. The material and thickness of each layer in WLP

Layer	Material & Thickness	Thickness [um]
1st PI	Polyimide	8
RDL	Copper, Titanium/Copper	6 , 0.1 / 0.2
2nd PI	Polyimide	10
UBM	Copper/Nickel, Titanium/Copper	5 / 2 , 0.1 / 0.2
Ball	Sn98.25/Ag1.2 (198um)	198

Table 3. The material properties adopted for TCAD simulation

Material	Elastic Modulus [GPa]	Poisson Ratio	Coefficient of Temperature Expansion(CTE) [ppm/℃]
Polyimide (HD4100)	3.5	0.28	35.0
Copper	111.5	0.34	16.5
Titanium	111.3	0.33	6.5
Nickel	186.0	0.34	12.5
Ball (Sn98.25/Ag1.2)	15.0	0.35	21.5

Table 2 and 3 indicate the material composition and the thickness of the etch layer and material properties of WLP adopted in this work. During TC reliability test, the CTE mismatch between packaging materials induces the mechanical stress. Especially, the large stress occurs between copper and polyimide as a stress buffer because the CTE and elastic modulus of polyimide are over two times larger and smaller than that of the copper, respectively.

C. BGR Circuit

Fig. 2 shows the BGR circuit with two transistors, A and B PMOS, in relations of the current mirroring each other. The variation of the output of BGR circuit, Vref, managed by maximum +/-1% for high accuracy of integrated system. The performance mismatch between two transistors controls the Vref.

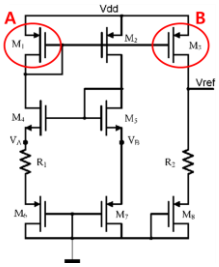

Fig 2. BGR circuit with transistors in relations of the current mirroring

D. Conditions for Reliability Testing and Simulations

We simulated with three different RDL designs of type 1, 2, and 3 illustrated in Fig. 3. Rectangles with the dotted line are the block of BGR circuit. The RDLs are drawn considering the position of A and B PMOS transistors. All transistors in three cases are fully covered with the RDL while RDLs on B transistors are designed, differently. The B transistor in type 1 is located under polyimide between RDL films while those in type 2 and 3 are fully covered and not covered with the RDL, respectively.

The window of the simulation is 570um * 830um and the thickness of substrate, silicon, is 205.96um. The diameter of the ball is 250um and the thickness information of other materials is in Table 2. The length and width of both A and B transistors are 50.5um and 73.56um, respectively. The simulation window has the periodic boundary condition for realistic simulations. The channel and wafer orientations of silicon are <110> and (100), respectively.

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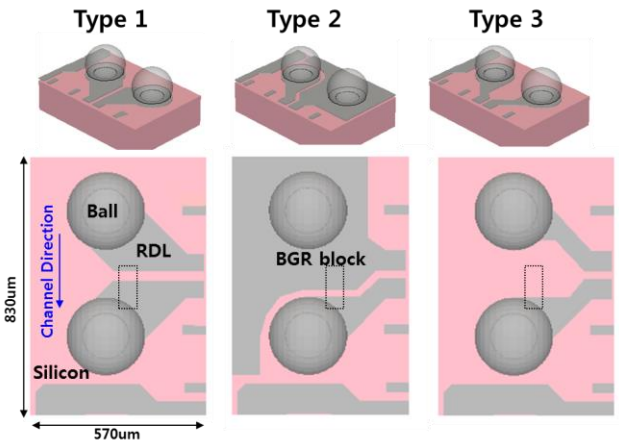

Fig. 3. Three types with different RDL designs on BGR circuit block

III. Results and Discussion

A. Stress Distribution

Fig. 4 shows the simulation results of type 1 and the stress distribution on silicon in channel direction (a) and width direction (b), respectively. The compressive stress is induced between RDLs in both channel and width directions. As the RDLs closes, the stress increases as shown in Fig. 4 (a). Under the ball and RDL, silicon has the tensile stress in both channel and width directions. However, the MV of PMOS under the ball and RDL is very small because the stress effect on the MV is compensated in both x and y direction as shown in Fig. 5(a). The stress effect on PMOS devices is large in the channel and width directions while the vertical stress has no effect on silicon due to the piezo effect. The silicon under polyimide between RDL films has the large positive mobility increase due to the concentrated compressive stress in the channel directions.

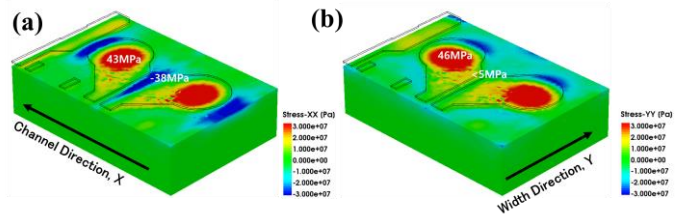

Fig 4. Stress distributions on silicon in (a) channel and (b) width direction

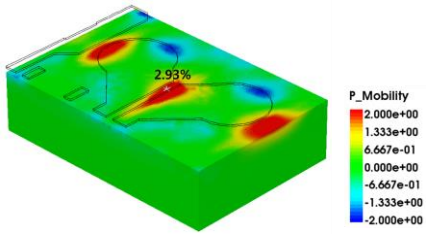

Fig 5. Mobility Variation of PMOS in type 1 after TC

Fig. 6 shows the stress distribution in channel direction of the region with polyimide between RDL films. The RDL has the large compressive stress by the TC test but this stress does not affect the silicon below the RDL unless the RDL is disconnected. The compressive stress induced between polyimide and RDL films affects the silicon and increases the mobility of PMOS as shown in Fig. 5.

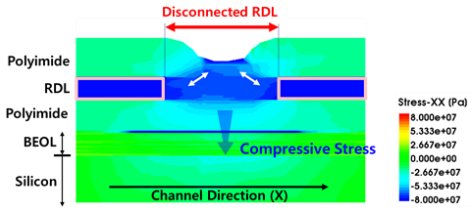

Fig 6. The side view of the region with polyimide between RDL films

B. RDL Design Effect on BGR Reliability

The stress mismatch induces the current mismatch in two transistors in a relation of the current mirroring by the local stress at polyimide between RDL films. Accordingly, the design of the RDL affects the silicon stress and the Vref of BGR.

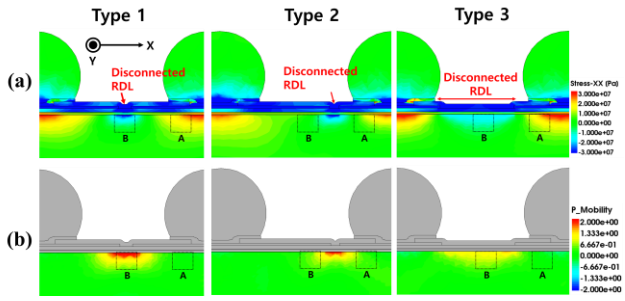

Fig 7. The simulation results of three types (a) the stress distribution in channel direction, x (b) MVs of PMOS after TC.

Fig. 7 shows the stress distributions and MV of three types with the different RDL designs. The polyimide between RDL films in type 2 is not located on the B transistor and the RDLs in type 3 are a great distance away as if the RDL does not cover the B transistor. The stress in the channel direction is dominant on the MV. Accordingly, the B transistors in type 1 and 3 have large and small positive MV respectively while the RDL in type 2 has little impact on the B transistor as shown in Fig. 7(b).

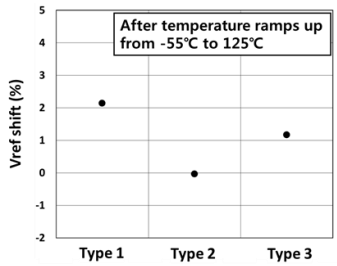

Fig 8. Extracted Vref shifts from simulation results of three types

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Fig. 8 shows the Vref shift of BGR circuit in types with the different RDL designs. The Vref shift is the difference between the average MV of A and B transistors. As the RDL fully covers the transistors, the mismatch and Vref shift minimize like type 2. Increasing distance between RDLs is an effective way for the Vref shift to decrease.

C. Validation with Experimental Results

Fig. 9 show the simulated and measured Vref shift after 300 TCs. The Vref shift dependence on RDL designs in experimental data is in accord with that of the simulation. As the experiment, type 1 failed in TC test while type 2 and 3 passed because the Vref shift is under 1% that is the limit for TC pass. The difference between the simulation results and the measured data can decrease by tuning TC conditions of the simulation.

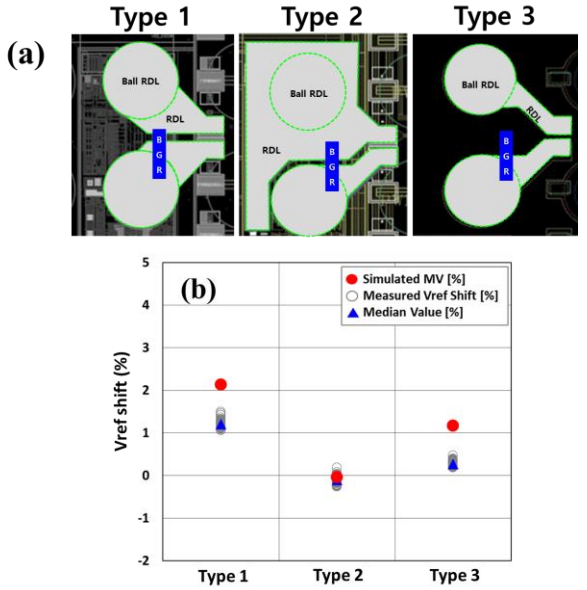

Fig 9. (a) Three samples with different RDL designs for the experiment and (b) the simulated and measured Vref shift after 300 TCs

As a result, the RDL designs have impact on the device performance in silicon during TC reliability test and the normal operation of circuits can be disturbed or failed. Fully covering the RDL on the sensitive transistors in the BGR circuit can minimize the mismatch of the device performance by the concentrated local stress. Above this, the mismatch can decreases by optimizing the distance between disconnected RDLs.

IV. Conclusions

The RDL of the plastic material is the key technology in WLP and covered with the polyimide with high CTE. Thus, we investigates the mechanical stress induced by the CTE mismatch between packaging materials during TC reliability test and the impact on the device performance during the reliable chip operation. We analyze the failure mechanism in WLP using TCAD simulations and it found that the mechanical stress between the polyimide and RDLs influences the device performance on the silicon during TC. In other words, the design of RDL can affect the stress of the silicon and be locally concentrated. This local stress induces the mismatch between the transistors in relations of the current mirroring and the Vref shift in BGR circuit. For validity of our research, we verify TCAD results with the experimental data.

Therefore, we should design the RDLs in WLP considering the position of the sensitive circuit on the stress like BGR for the reliable chip performance.

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