Calibration Insights of Phosphorus Diffusion Model for NMOS FDSOI : Pathway to advanced technology nodes

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***Abstract*— This paper evaluates the lateral dopant diffusion for source and drain junction profiles of NMOS FDSOI devices. Parameters of the phosphorus diffusion model in an in-situ doped epitaxial Source/drain are calibrated using TCAD simulations, and validated against experimental data, which vary with spike anneal temperatures, epitaxy concentrations, and gate lengths. After carefully adjusting these parameters, we incorporate them into a global simulation approach for device scaling. This enables the transition from current baseline FDSOI technology to even advanced FDSOI technology nodes.**

Keywords— Advanced FDSOI structures, dopant diffusion models, TCAD simulations, device scalability.

I. Methodology to calibrate TCAD simulation

When assessing FDSOI technologies, accurately forecasting lateral dopant diffusion stands as a critical step in understanding its influence on the electrical performance, particularly in terms of electrostatic characteristics. This work presents preliminary results of simulations mandatory for any technological optimization. In a first step, a source/drain junction calibration on 28 nm FDSOI technology has been realized by simulating NMOS devices using TCAD Synopsys Sentaurus tools. For this purpose, dopant diffusion in silicon (Si) is studied and simulated electrical results are compared with experimental ones. Then, these extracted diffusion model parameters are incorporated in a complete process and electrical simulation flow to build the most relevant pathways to reach sub-10 nm FDSOI technology node.

II. Lateral S/D junction diffusion optimization

Starting from the simulation of a 28 nm FDSOI process flow, Table 1 and Fig. 1 summarize the main geometries and the good agreement between Transmission Electron Microscopy (TEM) vs. Sprocess morphological simulation result.

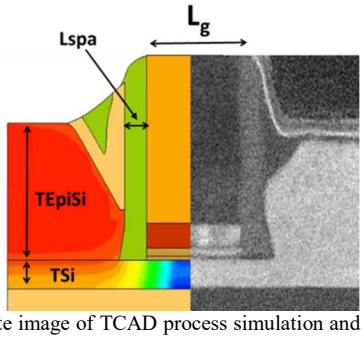

Fig. 1: Composite image of TCAD process simulation and TEM of CEA-Leti's 28FDSOI NMOS

TABLE I. Main process geometries

Process parameter	28FDSOI (nm)	Advanced node (nm)
T_{Si}	7.5	5.5
T_{EpiSi}	30	30
T_{BOX}	25	20
L_{spa}	7	7
EOT	1.02	0.78

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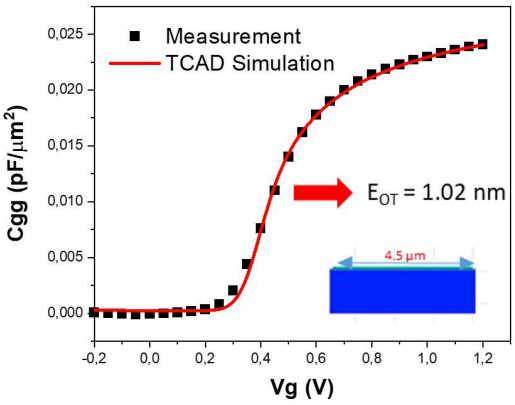

Fig. 2: Cgg vs Vg: measurements (dots) and simulation (solid line) for long and wide device (W=L=4.5um).

To calibrate S/D junction, 2 phosphorus concentrations and 3 different spike temperatures (T_{Spike}) are experimentally investigated. Note that the S/D parts are realized by an in-situ doped epitaxial step with facetted sides [2]. The P concentration will vary while remaining below solubility limit of P in silicon. To evaluate the lateral P diffusion into silicon, the best electrical parameter that directly depends on the electric length (L_{el}) of the channel is the Drain-Induced Barrier Lowering (DIBL) which can be written as [3]:

$$DIBL \approx \left(1+\frac{T_{Si}^2}{L_{el}^2}\right)\left(EOT \times \frac{T_{Si}}{L_{el}^2}\right)\mathrm{D} \qquad (1)$$

and $$L_{el} = L_g + \Delta L_j \qquad (2)$$

where ΔLj is the part of the channel determined by S/D jonctions length which could be positive or negative. To extract accurately the DIBL, we firstly extracted the Equivalent Oxide Thickness (EOT) and gate stack permittivity (interfacial oxide and HfO_2) with both TEM and wide and large capacitances.

Fig. 2 illustrates the comparison between measurement and simulation results using EOT=1.02nm on $C_{gg}(V_g)$. Note that all simulations take into account the 2D quantum confinement model with corresponding parameters according to [4].

As presented in Fig. 3, "charge pair" model available in Sentaurus Sprocess tool is chosen for diffusion [5]. This model takes into account both the variations of dopant concentrations described by the elementary Fick law and the defects present in the crystal (vacancies and interstitials), and therefore electric field generated by these defect charges and P displacements thanks to the dopant-defect pairs diffusion these ones being considered at equilibrium. In addition to this aspect of diffusion, dopant transport by kick out mechanism is taken into account in the diffusivity model.

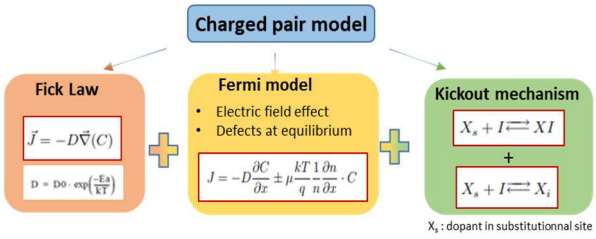

Fig. 3: Physical mechanisms and equations included in "charged pair" model in Sprocess tool. J is dopant flux, D and C are respectively the diffusion coefficient and concentration of Phosphorus, E_a is the activation energy and n is the number of charges

The adjusted diffusion coefficients are those controlling the mechanisms mentioned above including temperature dependency (T_{Spike}). The TCAD simulations results are shown in Fig. 4 with DIBL variations with Lg. DIBL vs Lg simulations are in a very good agreement with experimental DIBL for all temperature range and 2 S/D epitaxy generation 1.6×10^{20} cm^{-3} (Gen A) and 2×10^{20} cm^{-3} (Gen B).

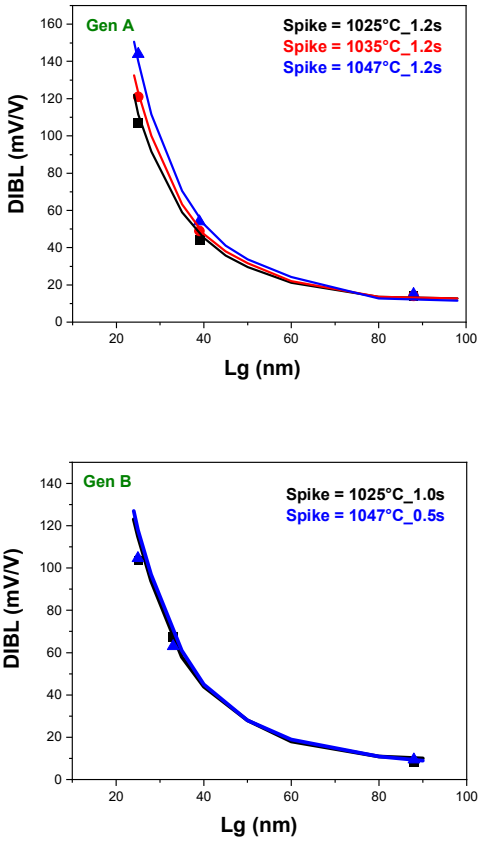

Fig. 4: DIBL vs Lg: measured (dots) and simulated (solid line) for different spike temperature (1025, 1035 and 1047 °C) and 2 S/D epitaxy generation Gen A and Gen B.

Besides, increasing T_{Spike} from 1025°C to 1047°C had a pronounced effect, exacerbating DIBL by roughly 18%. This increase highlights the significant influence of temperature on dopant activation and diffusion, while also negatively affecting short-channel behavior.

III. Projection into Advanced FDSOI Nodes with a Future Perspective

Using the calibrated deck, an in-depth investigation was carried out to study the impact of various scaling parameters on the electrical behavior of the device (Table 1). Specifically, we carefully investigate the effects of reducing channel (T_{Si}), BOX (T_{BOX}), and EOT thicknesses on DIBL, subthreshold swing (SS_{sat}) and threshold voltage (V_{th}). These simulations are crucial for anticipating the challenges and potential adjustments needed in process fabrication as dimensions shrink.

The analysis depicted in the graphs of Fig. 5, revealed that a T_{Si} reduction from 7.5 nm to 5.5 nm with optimizing T_{BOX} to 20 nm and decreasing EOT to 0.78 nm significantly enhanced electrostatic control across the channel, as evidenced by a 50% reduction in DIBL. This tighter control enables a more

effective gate modulation of the channel's potential barrier, which require higher gate voltage to invert the channel, leading to an increase in V_{th}.

Additionally, to explore the scaling effects on device performance, we conduct an in-depth investigation into the challenges associated with (S/D) epitaxy development. Specifically, we investigate the effects of increasing S/D phosphorus concentration and spike annealing temperature on DIBL and ON-state resistance (R_{ON}). Moreover, we investigate the effect of channel recessing prior to epitaxial layer deposition to reduce access resistance (R_{access}).

In this work, we employ TCAD simulation to extract R_{ON} and its various components, including resistance in the epitaxy layer (R_{epi}), under spacer regions (R_{spa}), and channel resistance ($R_{channel}$), as presented in Fig 6.

The extraction method is detailed in reference [6]. We simulate the I_d-V_g curves in the linear regime. For a specified gate voltage (V_g), we extract the electronic quasi-Fermi potential along the conduction path. Subsequently, we calculate the resistances between two symmetrical positions by applying:

$$R_{access} = \frac{eQ_F(x_2,V_g) - eQ_F(x_1,V_g)}{I_{dlin}} \quad (3)$$

As shown in Fig. 7, increasing P concentration from 1.6×10^{20} cm^{-3} (Gen A) to 2×10^{20} cm^{-3} (Gen B) led to enhanced dopant diffusion, effectively reducing L_{el} and then increasing the DIBL by approximately 4 mV/V, indicating a compromise in gate control over the channel. Furthermore, Gen B achieved 7 % of R_{ON} reduction.

This is due to the decreased S/D epitaxy resistance giving an improvement in device conductivity. These trends are observed for different epitaxy recesses depth. Additionally, we observe that increasing T_{Spike} from 1025°C to 1047°C had a pronounced effect, exacerbating DIBL by roughly 15 %. While it decreases R_{ON} by reducing channel resistance. This advantage is counteracted by an increase in resistance under spacers resulting from enhanced dopant diffusion.

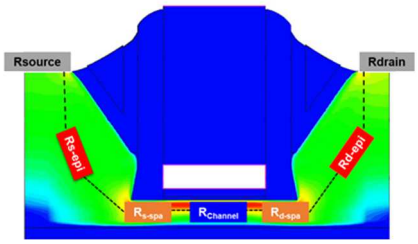

Fig. 6: Schematic of different resistance contribution with Ron resistance.

Furthermore, channel recessing revealed that a recess depth of 1 nanometer resulted in a roughly 5 % increase in DIBL. This occurs because recessing the silicon before S/D epitaxy allows dopants diffusing more extensively into the channel region, reducing the effectiveness of the gate in controlling the channel potential, hence increasing DIBL. Additionally, it results in a 4% reduction in R_{ON}. This is because the controlled diffusion of dopants into the channel creates a gradual doping profile, reducing abrupt changes in resistance and ensuring smoother carrier flow from the S/D to the channel. Moreover, the recess before epitaxy enhances dopant activation in the S/D regions.

These results highlights the remarkable compromise between DIBL and R_{ON} by increasing S/D epitaxy doping and recess depth.

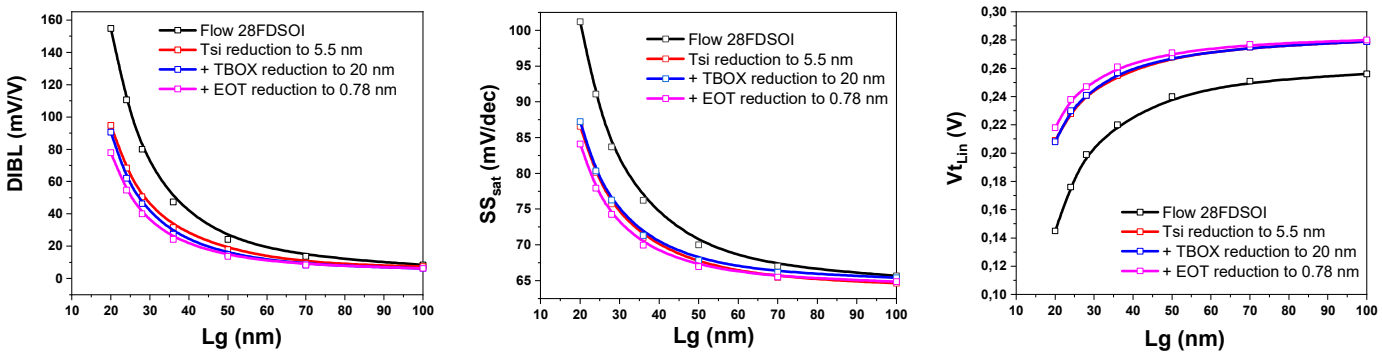

Fig. 5: DIBL, SS_{sat} and Vt_{lin} vs L_g for present 28FDSOI NMOS with respectively T_{si} reduction, T_{BOX} reduction and EOT reduction.

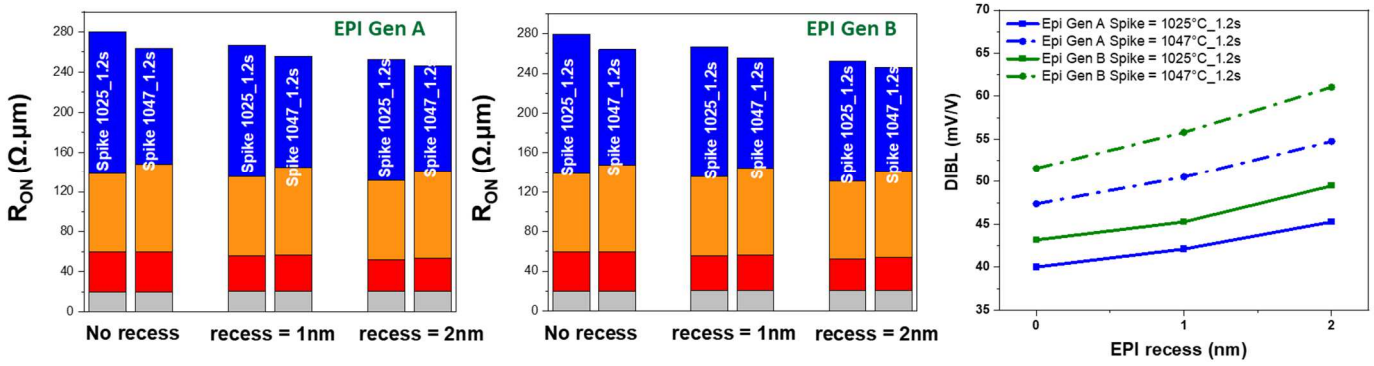

Fig. 7: R_{ON} and DIBL vs EPI recess for 2 different spike (1025 °C and 1047 °C for 1.2s) and 2 epitaxy Gen A and Gen B.

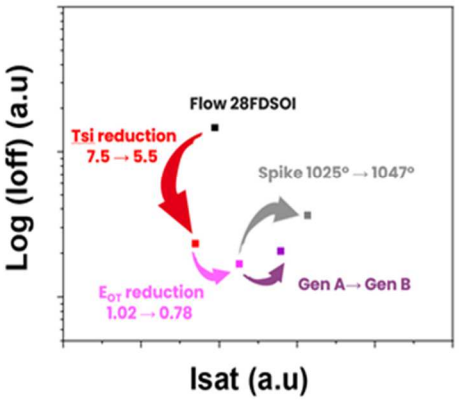

Fig. 8: I_{off} vs I_{sat} for different senario from intial 28FDSOI: impact of T_{si}, EOT, doping in epitaxy and spike.

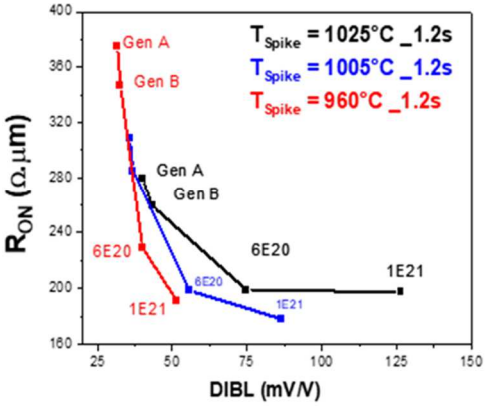

Fig. 9: Effect of reducing spike temperature on R_{ON} vs DIBL for different epitaxy doping concentration

Ultimately, Fig. 8 demonstrates the advantageous impact of scaling and optimizing the epitaxial layer on the I_{sat}/I_{off} ratio. This is achieved through a marked reduction in I_{off} and an improvement in I_{sat}, emphasizing the substantial influence of increasing S/D concentration and high spike temperature. However, increasing phosphorus concentration in the epitaxial layer, which is necessary to attain an acceptable R_{ON} value, requires careful monitoring of spike temperatures, as depicted in Fig. 9.

It is evident that with lower spike temperatures, R_{ON} varies significantly with the dopant concentration in the epitaxial S/D regions due to the limited dopant activation. This increased sensitivity to doping variations is less pronounced at higher T_{spike} temperature. At the same time, there is reduced sensitivity to DIBL due to the limited diffusion.

As an exploration for device optimization, we should investigate in a future work the use of combination of rapid thermal annealing with high temperature laser annealing. With this combination, thanks to a reduced diffusion and an enhanced dopant activation, we could achieve high doping concentrations in the S/D epitaxial layers up to 10^{21} cm^{-3} without exacerbating DIBL

IV. Conclusion

This study presents a comprehensive analysis of lateral dopant diffusion in S/D junction profiles for NMOS FDSOI devices. By calibrating phosphorus diffusion parameters against data measurement and refining global simulation methods, this work paves the way for scaling advanced FDSOI technology nodes and underscores the delicate balance required between enhancing device performance and mitigating short-channel effects.

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