Automated Algorithmic Parameter Extraction of TCAD-Based SPAD SPICE Models

Patryk Maciążek*†, Isobel Nicholson†, Jean-Robert Manouvrier‡, Denis Rideau‡, Filip Kaklin†, Elsa Lacombe‡, Mohammed Al-Rawhani†, Christel Buj‡, Sara Pellegrini†, Vihar Georgiev*.
*Deep Nano, JWSE University Of Glasgow, UK.
†STMicroelectronics Edinburgh, UK.
‡STMicroelectronics Crolles, France.

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***Abstract*—We present a methodology of automated parameter extraction for TCAD-based SPAD SPICE models using the Levenberg-Marquardt algorithm. The demonstrated solution has been validated on a large number of SPAD designs. These have been simulated using a well calibrated process and device simulator. Physics-based parameters which are difficult to measure experimentally were extracted from TCAD. We are able to accurately bench the designs against key figures of merit such as maximum count rate (MCR) through comparison with silicon characterisation. This method can be applied before silicon characterisation for predictive SPICE models.**

***Index Terms*—TCAD, SPAD, SPICE, Levenberg-Marquardt, predictive SPICE, Parameter Extraction**

I. Introduction

Single Photon Avalanche Diodes are *p-n* junctions capable of sensing individual photon absorption events, with many applications including automotive [1] and consumer electronics industries [2]. Improvements in speed and functionality of predictive tools such as TCAD and SPICE are needed to allow for rapid optimisation of SPAD models for circuit simulation. During early technology development phase, SPAD pixel optimisation is challenging in the absence of characterisation-derived SPICE models. There are also challenges in deploying a TCAD-based SPAD SPICE model effectively. Manual fitting of SPAD SPICE models to TCAD data is not suitable for large-scale evaluation, thus necessitating an automated algorithmic approach. Any implementation will rely on reproducing the capacitance characteristics of the design as well as those regarding breakdown. To be considered successful, any device model must compare well against key figures of merit from silicon characterisation such as maximum count rate (MCR), in addition to the characteristics that are used to fit the model.

II. Background Theory

SPADs rely on impact ionisation in the high field region from the photo-generated carrier causing an avalanche. The avalanche must be quenched and SPAD recharged to its original condition. Recent SPAD SPICE models [3] use characterised silicon data like the current-voltage (IV) and capacitance-voltage (CV) curves as target behaviour for the model. Inside, the SPICE SPAD models are driven by the standard definition of the charge in a p-n junction with an arbitrarily shaped doping profile as shown in Eq. 1 [4].

$$Q(V) = \frac{C_j(V_0) * \phi_i}{1-p} * \left[1 - \left[1 - \frac{V}{\phi_i}\right]^{1-p}\right] \tag{1}$$

The capacitance C_j at a given voltage is used to calculate the charge, and thus the electric field. The remaining parameters such as the grading of the junction p or the forward voltage ϕ_i are used for fitting purposes. The fitted charge is used to calculate electric field, and in turn is used in the Van Overstraten De Man impact ionisation model [5]. This model is used to calculate the multiplication coefficients G_e of charge carriers due to impact ionisation in the high field region.

$$G_e = \alpha_e \exp^{-\beta_e / E_{field}} \tag{2}$$

The field-dependent multiplication coefficients are combined with the number of charge carriers created per unit photo-generation I_{unit}^{ramo} based on the carrier charge q, carrier velocity v and electric field at unit cathode potential E_o taken from the Shockley-Ramo theorem [6].

$$I_{unit}^{ramo} = q * v * E_0 \tag{3}$$

$$M_e = G_e/\tau_e * I_e/I_{unit}^{ramo} \tag{4}$$

These are combined with values for the carrier lifetime τ_e and used in the McIntyre model (5) [7] to calculate the device current. Equivalent equations for holes apply. The calculated currents are summed to give the avalanche current.

$$dI_e/dt = [M_e * I_e + M_h * I_h - I_e]/\tau_e \tag{5}$$

III. Extraction Methodology

Before commencing the fitting process, it is required to extract values for τ_e, τ_h and I_{unit}^{ramo} from TCAD. This necessitates the extraction of carrier velocities and electric field at unit cathode potential. This is done because a change in architecture [8] or manufacturing process [9] can impact these values. It is challenging to deduce these values from CV or IV curves and therefore simulation methods must be used to estimate their value. Using TCAD, carrier lifetimes and velocities can be extracted. These are then both used in calculation of model parameters. Shown in Figure 1, the electron velocity is seen to be constant in the region of interest. As can be seen in Figure 2, there is some small variation of

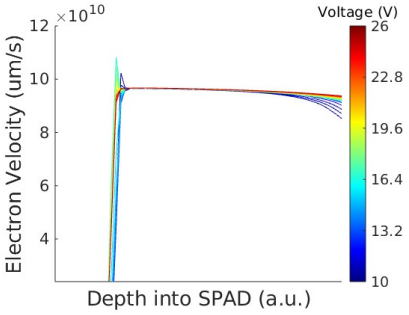

Fig. 1. Graph depicting the electron velocity as a function of vertical depth inside the SPAD.

these parameters with respect to voltage. For simplicity we have taken the first order approximation of constant values. The effects of variation of both lifetime and Ramo parameters on pulse shape which in turn controls the circuit test responses is shown in Figure 3.

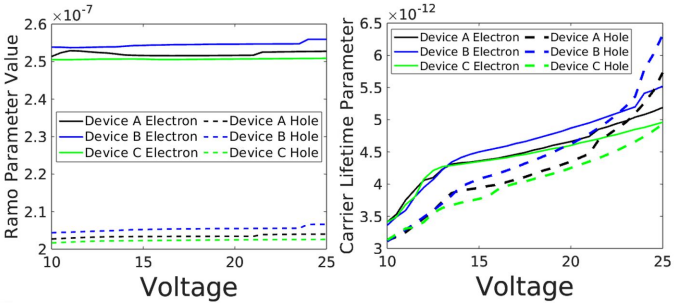

Fig. 2. Graphs depicting the Ramo model parameter, I_{unit}^{ramo}, and carrier lifetime τ as a function of applied voltage as extracted from TCAD data.

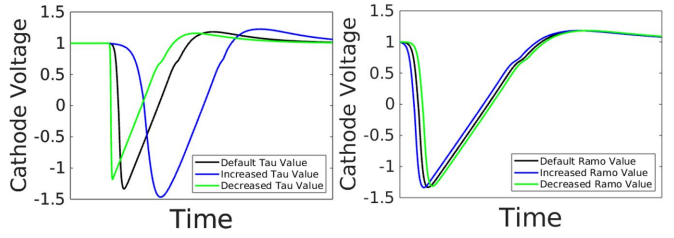

Fig. 3. Graph depicting the effects of varying τ (carrier lifetime) and I_{unit}^{ramo} parameters on the shape of the pulse on the cathode of the trial diode. The values of both parameters were varied by a scale factor of 5 in both graphs.

The next step of the extraction uses the Levenberg-Marquardt algorithm [10] to align the SPICE model to CV & IV data from TCAD (or characterisation) through adjusting known model parameters as in equation 1. The algorithm (Figure 4) requires a reasonable parameter estimate for initialisation and recursively calculates gradients and uses them when calculating the next guess aiming to minimize the error function. The error function is defined as the sum of the relative errors of all fitting points. Weighting factors are used to emphasise the quality of fit for certain points such as the breakdown voltage or device capacitance at zero bias. The gradients are calculated with the finite difference method, using numerical variation of each parameter by 1%. The resultant changes in error are used to assemble the Jacobian matrix (step 8 in Figure 4). The updated parameter set is calculated with the Moore-Penrose inverse, using the Jacobian, a diagonal matrix D taken from $J_k^T J_k$ and a variable λ which depends on previous error (step 9). λ is evaluated at each guess, it increases when a guess does not reduce the error function, and conversely reduces when a lower error value is achieved.

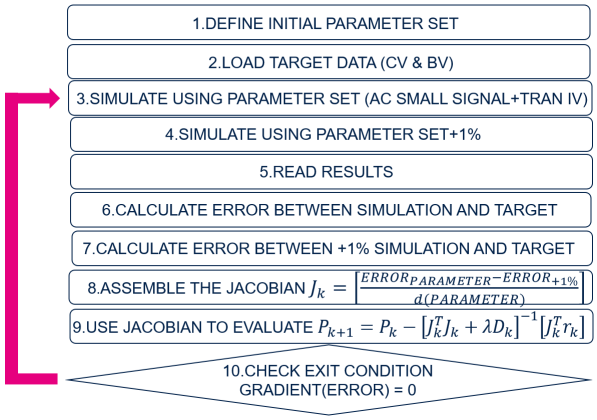

Fig. 4. Diagram illustrating the flow of the parameter extraction algorithm.

The algorithm integrates directly with a chosen variant of SPICE (Siemens Eldo) for IV and CV analysis to maintain model consistency and avoid compatibility issues with different SPICE solvers. To account for the possibility of a local minima being found rather than a global one when minimising the error function, the fitting algorithm is ran multiple times using a different starting points for the initial guess. Random start initial guesses use a normal distribution for the parameters where the original values are the mean with a defined standard deviation to ensure that despite being varied, the values are ones that are physically possible.

Ten SPADs with varying electric field profiles were modeled in TCAD (devices A through J) and implemented on silicon. These trials were engineered to shape and vary the internal electric field. Their BV and CV characteristics were extracted from mixed-mode simulations, and used as inputs to the fitting algorithm.The results of are illustrated in Figure 5. The convergence of the algorithm was quick, only requiring 50.8 iterations to converge on average, and resulting in a fit that had a mean error of 1.85% per fitting point, with around 2300 points being used to fit any given SPAD. Highest quality of fit can be seen on device A, which achieved a mean error per fitting point of less than 1.4% with device B being the fastest to converge at 35 iterations.

The quality of the recreation of target characteristics is

demonstrated in Figure 6 where the CV and IV characteristics of device A are shown to match the TCAD based on the parameters extracted using the demonstrated algorithm. On the whole, there are no major outliers in terms of quality of fit of desired characteristics to the underlying model as all ten trials came within 0.5% of each other, with a little more variation seen in the number of iterations required for convergence.

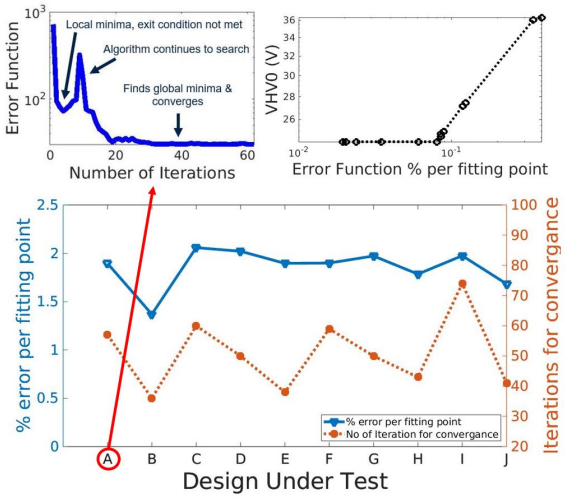

Fig. 5. Final fitting error and number of iterations to reach convergence for each device under test. Top Left: value of the error function vs number of iterations for device A. Top Right: VHV_0 figure of merit converging as the average error % per fitting point reduces (see Testing and Results)

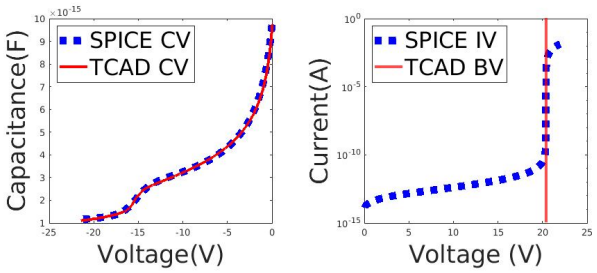

Fig. 6. Graphs depicting the simulation result using the final values from parameter extraction for device B and comparing with the target data.

IV. Testing and Results

SPAD model behaviour with an integrated quench circuit similar to the Figure 7 was evaluated in SPICE. The lowest bias VHV_0 to produce a pulse was extracted [11]. The value of VHV_0 is given by sum of the BV and the voltage swing required to cross a triggering threshold. This is evaluated using a transient voltage ramp, where the applied bias is being ramped up whilst the SPAD is provided with incident photons at regular intervals. The test bench looks for the lowest biasing values to achieve an output pulse from the end-stage inverter. To demonstrate this, two quench circuits with differing triggering thresholds as described in Figure 7 were examined. The first quench circuit (quench circuit 1) had a lower capacitance ratio of C_{IN} to C_S. The increased VHV_0 of quench circuit 2 reflects its higher triggering threshold.

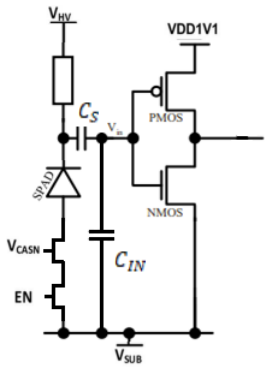

Fig. 7. Diagram of SPAD under test in an example quench circuit [12]. The ratio of C_{IN} to C_S in the capacitance voltage divider prior to the inverter can be varied to change the triggering threshold of the circuit. This causes variation in VHV_0 between circuits as can be seen in Figure 8.

Figure 8 demonstrates the extracted values of VHV_0 taken from the combinations of the two quenching circuits used with the diodes under test. Comparing the three traces in the graph, crucially we see that the extracted VHV_0 values are all above the TCAD breakdown voltage, with a constant voltage difference between TCAD BV and circuit 1 and circuit 2. This suggests that the difference in voltage is down to the difference in triggering threshold which is a property of the quench circuit rather than the individual diode. Comparing the diode trials to each other, we see that the diode trials clearly reflect the differences in their architecture. Given the same trial-to-trial behaviour seen in each of the three traces, we can assume that the this behaviour is down to the diode trials, rather than being a property of the quench circuit.

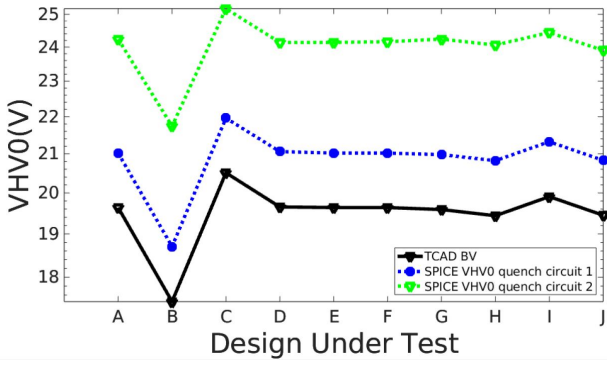

Fig. 8. Graph showing the result of using the fitted parameter sets inside the VHV_0 circuit benchmark. The graph highlights the device level characteristics being reflected in the circuit level simulations in both circuit despite the different triggering voltages associated with circuit configuration

Secondly, the same set of extracted parameter sets were inside the integrated circuit were evaluated for the maximum count rate (MCR) possible given the combination. The is an important characteristic of the SPAD and circuit combination

[13], as they both contribute to the overall result. The test bench evaluates the response of the circuit when it is biased at its VHV_0 point as it is stimulated with photons from a poissonian source with a defined inter-pulse time. A sweep of inter-pulse times is carried out, as the circuit can enter a state of paralysis where it does not return to its original condition (thus not functioning properly), and shortening of the inter pulse time does not correlate with a higher MCR. An example illustration of this behaviour can be seen in Figure (9)

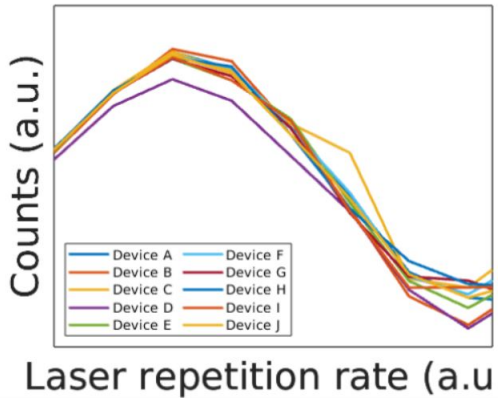

Fig. 9. Graph depicting the example behaviour inside a simulation MCR test bench, highlighting the behaviour of performance roll-off where the output count rate no longer tracks the photon input rate following paralysis.

Figure 10 depicts the result of the second benchmark test which looks at the max count rate of the diode trials inside the quench circuitry. The diode trials in the SPICE test bench conveyed the key behaviour trends seen in silicon characterisation when comparing trial to trial. The range of MCRs seen in the SPICE test bench for devices C and D was lower than that seen in characterisation of the silicon for devices, however the average difference between the SPICE bench and the characterisation was seen to be around 5%.

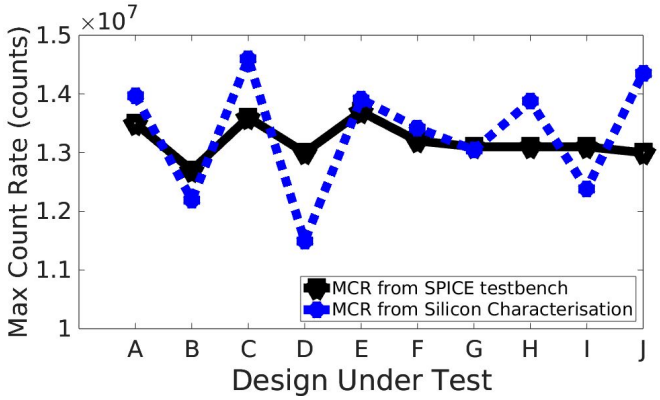

Fig. 10. Graph depicting the result of the max count rate SPICE benchmark, with a comparison of same diode and circuit seen in silicon characterisation.

V. Conclusion

In conclusion, this work presents a methodology for automating SPAD SPICE model extraction from TCAD outputs. Based on this methodology, we were able to extract model parameters for ten diodes and use them in circuit simulation, testing for the lowest bias point to all successful triggering (VHV_0) as well as maximum count rate (MCR) of the SPAD and circuit used. The VHV_0 test demonstrates the expected results where the circuit has a higher triggering point than the breakdown voltage of the diode due to the threshold of the surrounding circuitry. Going from trial diode to diode, the test bench conveys the trends in behaviour resulting from changes in design. The MCR test bench also compares favourably when compared to characterisation data, by effectively conveying the trends in MCR variation due to the differences in architecture. This successful methodology can lead to improved design processes by offering a means of faster evaluation of large volume of trial candidates, with a variety of circuits. This will allow for a more efficient design process thus resulting in shorter cycle times and shorter time to market.

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