Atomistic Multiscale Simulation-Based Extraction of Design Margins in Advanced Transistor Architectures

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***Abstract*—Employing Kinetic Monte Carlo (KMC) method for epitaxy simulation reinforced with Molecular Dynamics for KMC model parameter extraction, this study establishes an approach for determining design margins in transistor architectures characterized by high aspect ratio cavities. This integrated atomistic and multiscale simulation framework allows prediction of the epitaxy quality and potential defects as well as the optimization of key design parameters.**

Keywords— Multiscale Simulation, KMC, MD, Epitaxy, DRAM

I. Introduction

Source-drain (SD) epitaxy became a key semiconductor process a few decades ago when it first allowed the creation of SiGe stressors for boosting the mobility of PMOS devices. Later, the same idea was applied for NMOS devices to create extremely steep and well-controlled lateral junction profile.

Recent movement towards three-dimensional devices was only possible because of epitaxial growth of sacrificial layers [1]. By depositing and etching these layers, complex three-dimensional structures can be made with great controllability [2]. Success in the epitaxy process and optimization relies heavily on the controlling the faceting found during the growth of Si/SiGe system [3]. To accurately predict and fully capitalize this behavior, atomic scale simulation is preferable. The Kinetic Monte Carlo (KMC) method that predicts the evolution of atomic processes (diffusion, adsorption, etc) by stochastically selecting events based on their probabilities, is one of the most efficient approaches. This method efficiently simulates film growth and surface evolution over long timescales, providing valuable insights into how growth parameters affect material properties. Its ability to capture the kinetics of epitaxial layer formation makes KMC an essential tool for optimizing deposition processes.

II. Multiscale Atomistic Epitaxy Simulation Methodology

While accurate atomic-scale epitaxy simulation models are widely used in semiconductor technology for predictive analysis of epitaxy rate, shape, and crystal lattice effects (e.g. [4,5]), most cannot explicitly account for local structure topology, which significantly impacts epitaxy characteristics. Given the nanoscale size of typical device features, common computational fluid dynamics approaches are inadequate due to

a large Knudsen number (Kn), necessitating molecular flow simulations to accurately predict the distribution of precursors on the material's surface. To address this, an efficient particle tracing methodology was developed and integrated with KMC simulations to consider the effect of local inhomogeneous distribution of incoming precursors (Fig. 1).

Since KMC is inherently an empirical method, it requires calibration of input parameters – such as binding energies for nearest and next-nearest neighboring atoms, adsorption, desorption, and diffusion rates – to deliver quantitatively robust results [4]. Calibration is challenging due to the simultaneous occurrence of many processes, making it nearly impossible to isolate them. Consequently, the same set of final structure parameters can be fitted by completely different sets of KMC model parameters, leading to significant calibration ambiguity and a high risk of increased simulation error with even slight changes in epitaxy conditions.

We have applied Molecular Dynamics (MD) simulation to extract key reactant species diffusion rates and simplify calibration process. We are using Reax Force Field approach [8] and an in-house potential parametrization extracted from the extensive set of DFT simulations. In simulation a single silicon adatom was placed on Si (110), (111), and (100) Silicon surfaces (example is shown in Fig 2a and Fig. 2b).

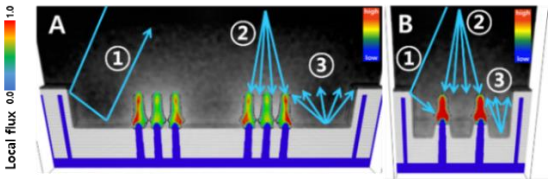

Fig. 1. Results of particle tracing simulation of precursors density distribution showing the effect of local structure on the epitaxy: depending on the geometry of the exposed silicon, the rate of precursor molecules scattering from surrounding structures (1), the average precursor density per exposed seed (2) and the rate of deflection from the non-Silicon surfaces (3) are different, leading to significant difference in the effective SD growth rate, depending on the local pattern and exposed Si structure.

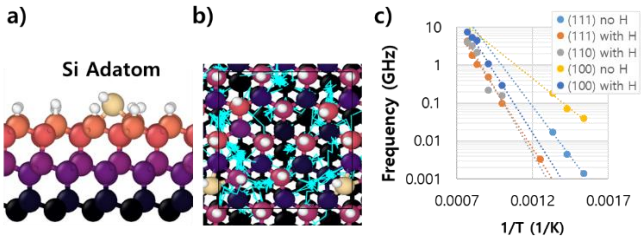

Fig. 2. Example of an atomic structure side view (a) and a full trajectory of MD simulation (b). Trajectories are shown with cyan color, multiple vibrations around local equilibria and occasional hoppings are observed. Extracted diffusion hops frequencies for different Si orientations and presence/absense of H passivation are also shown (c).

TABLE I. ACTIVATION ENERGY (E_A) AND PREFACTOR (f_0) OF ADATOM DIFFUSION ON UNPASSIVATED SI SURFACES.

Facet	**(111)**		**(100)**	
Method	**MD**	**H/W [9]**	**MD**	**H/W [10,11]**
E_A (eV)	1.06	1.07	0.63	0.66
f_0 (THz)	200	191	3.07	2.74

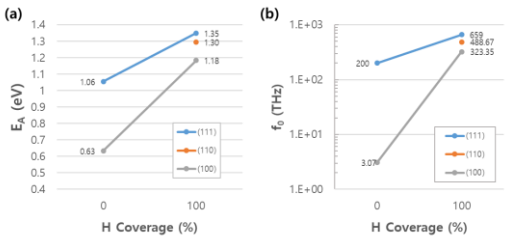

Fig. 3. Hydrogen passivation effect on diffusion statistics. (a) activation energy (E_A) and (b) prefactor (f_0) with respect to H coverage. Increment of activation energy by H passivation lowers total diffusivity on the surface.

Extracted diffusion rates (Fig.2c) clearly follow Arrhenius law and for the validation of the results we have compared activation energies and prefactors from our simulations with the reported experimental data for UHV silicon surface diffusion [9-11] (Table 1). The activation energy (E_A) extracted from MD agrees 99% with the H/W value while the exponential prefactor agrees 90% with the reported H/W data, which validates our methodology. The diffusion activation energy (E_A) on the (111) surface is 1.06 eV, higher than the 0.63 eV observed on the (100) surface, indicating slower diffusion on the (111) surface. This orientation dependence of activation energy may result from the number of dangling bonds per atom (only one on the (111) surface versus two on the (100) surface) making the (111) surface energetically more stable.

Since typical epitaxy and reflow process conditions are resulting in Hydrogen-passivated surfaces, MD simulations were extended to the case of high process temperatures (1000-1300 K) and considered full saturation of all Si dangling bonds with H atoms. Extracted adatom diffusion activation energies (E_A) are shown in Fig. 3a, and the prefactors are shown in Fig. 3b. Hydrogen passivation leads to lower diffusion rates for all surface orientations (Fig 2c), and as the decrease of the diffusion rate is not due to fewer potential diffusion sites since dangling bonds are H-passivated, but due to a change in the diffusion mechanism itself.

We have gathered diffusion statistics for more complex surface structures, including those with basic orientations steps in high symmetry directions shown in Fig 4.

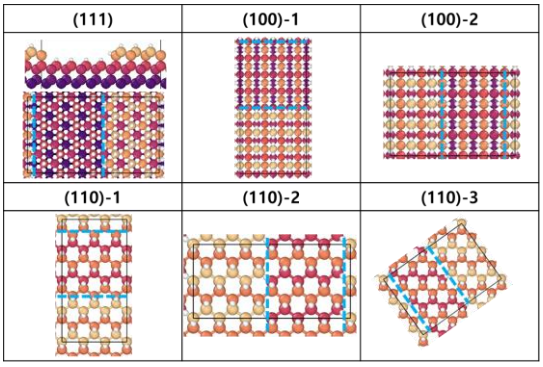

Fig. 4. Stepped surface structures on each facet. Atom color indicates the height of the atoms. On (111) facet, both top view and the side view of the structure is shown. The step has one atomic layer height.

Each computational cell contains twice as many atoms as those used for flat surface MD simulations. Each step has the

height of a single repeating unit of atomic structures, corresponding to the facet orientation. All dangling bonds are passivated by hydrogen atoms to ensure stability during MD simulations. A single Si adatom is placed randomly, so the diffusion statistics include both flat surface and step structure diffusion.

In Fig. 5, schematic diagrams of the step orientations (a, c, d) and full diffusion statistics with respect to temperature (b, d, f) are presented.

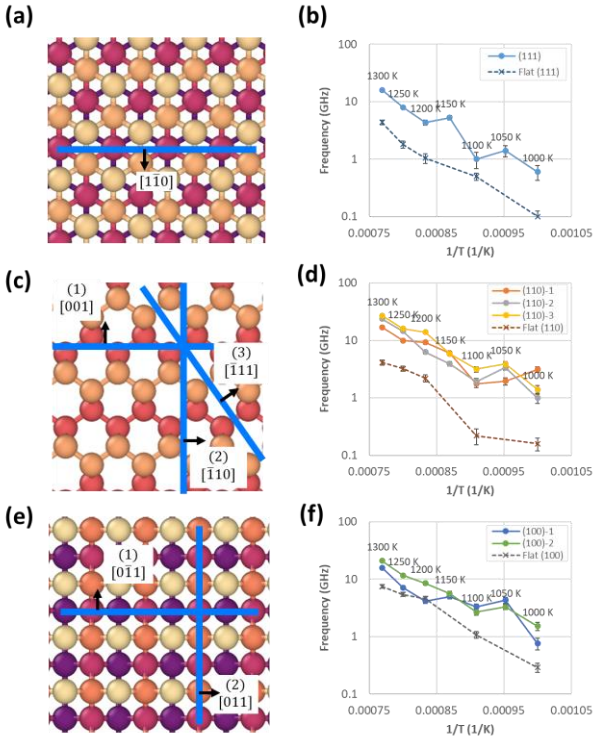

Fig. 5. Schematic of step orientation and diffusion statistics. Panels (a) and (b) depict the step structure and extracted diffusion frequency for the (111) facet, while panels (c) and (d) present the corresponding data for the (110) facet, and panels (e) and (f) for the (100) facet. Across all facets, the diffusion rate on stepped surfaces is higher compared to flat surfaces.

A wide temperature range from 1000 K to 1300 K is simulated. At each temperature and on each step, a single Si atom is placed in five different random locations across the surface. Since the cell includes both flat regions and steps, the diffusion statistics include both flat surface diffusion and step edge diffusion. In Fig. 5 (b, d, f), the diffusion rate at step edges is about an order of magnitude higher than on flat surfaces. The Arrhenius relation is less distinct for stepped surfaces compared to flat surfaces due to multiple diffusion mechanisms and the mix of flat surface and step-edge diffusion events. Temperature-dependent diffusion statistics, analyzed using the Arrhenius relation, show activation energy decrease due to presence of the steps for up to 0.5 eV on (110) surfaces. In Fig. 5 (d) differences between various step orientations are not clearly visible. However, significant deviations in activation energies, up to 0.4 eV, are observed for each step orientation according to the Arrhenius relation. For the hydrogen effect on diffusion at flat silicon surfaces, E_A and f_0 exhibit opposite trends compared to the step effect. The diffusion frequency prefactor slightly decreases for stepped surfaces, while total diffusivity increases significantly. This suggests that the activation energy is the dominant parameter for diffusion rate, unless there is a substantial deviation in the prefactors.

A diffusion database for non-periodic island structures, featuring symmetric edges as listed in Fig. 5 was constructed. Fig. 6 shows structure evolution during heat treatment. While all the structures are stable for up to 1300K, island structures begin to deform at about 1000 K. At lower temperatures, corner regions deform first as they are the most unstable.

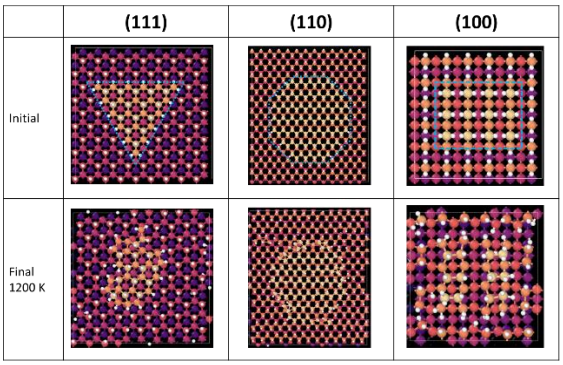

Fig. 6. En example of initial and final atomic configurations of Silicon surfaces with island structures. The island edges reflect highly symmetric directions relative to the facet orientation. The islands deform at relatively lower temperatures compared to flat and stepped surfaces.

III. Applications of the Methodology

The integration of empirical adsorption parameters, precursor ray-tracing, and MD-derived diffusion parameters is utilized across various applications in Logic and Memory technology. This approach is essential for estimating epitaxy-related design rules early in the process development stage.

One of the major challenges in developing novel devices process technology is the epitaxial growth in high depth-to-width aspect ratio structures. In these cases, the epitaxy process can generate numerous defects since the growth occurs not only from the bottom of the exposed Silicon seed but also from the sidewalls. This can potentially result in the formation of voids and grain boundaries.

Fig. 7 shows an example of epitaxy in a narrow structure which leads to the formation of extremely thin and deep trench in the middle of the growing surface. KMC parameters for simulation of epitaxy for five different recipes (v1.0, v2.0, v3.0, v3.1, and v4.0) have been calibrated based on experimental data and using the multiscale parameter extraction methodology explained in Section II.

The growth rate at the center of the epitaxial structure was compared. Since typical lattice KMC simulations cannot explicitly predict lattice defects, a criterion based on growth rate is applied: if vertical growth rate at the central point of the structure cavity exceeds that of a blanket (100) wafer, it suggests that the sidewalls have collapsed, likely forming a stacking fault or void. Earlier versions of epitaxy recipes have shown a spiking growth rate at the center. It means that the structure is growing not because of the attachment of the atoms to the bottom, but due to the merging of side-wall growth fronts. After process

optimization (v3.1 and v4.0) the side-wall growth rate was reduced and the structure showed much slower growth rate at the center, indicating a void-free structure. Using our multi-scale KMC simulation, prediction of void formation from different recipes depending on the initial module target specifications (MTS) of structure is now possible.

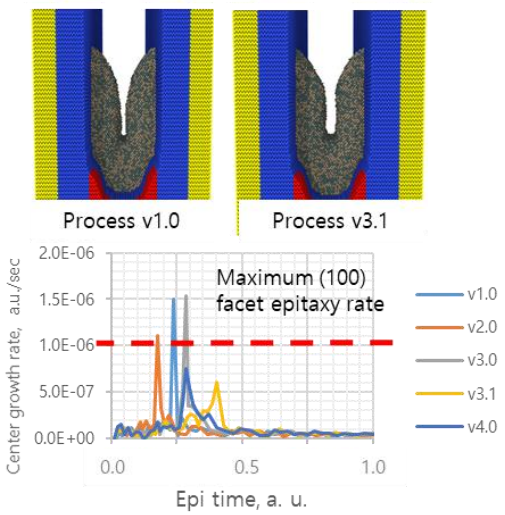

Fig. 7. Comparison between different epitaxy process versions in Logic device for the same volume of grown material. Process V3.1 shows much slower growth rate at the center (below growth rate at flat (100) surface). Therefore, formation of the defect is less likely.

To further demonstrate our simulation capability, we have simulated epitaxy growth on a multiple Si seed to examine their merge dynamics as well as void formation in between different epitaxially grown silicon (Fig. 8).

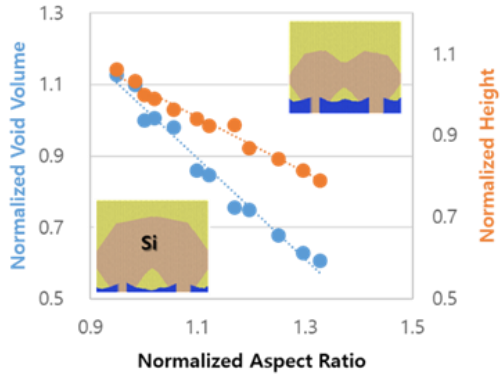

Fig. 8. An example of epitaxy growth and merge dynamics from multiple seeds. Depending on the topography and the process conditions, the growth pattern changes leading to different defects, such as void formation.

For each incoming structure and specified recipe, the rate at which the epitaxial precursor reaches the silicon seed was modeled using KMCRay. The reaction rates for different facets were calibrated based on both MD simulations and experimental results. Consequently, the growth rate of a specific facet is influenced by the structure and the epitaxy recipe used. We found that as the aspect ratio of incoming structure increases, the merge point of two epitaxy decreases. This results in the smaller final void between two epitaxy. Additionally, because the merge point was lowered, the final height of epitaxially grown Si is also lower. KMC/KMCRay methodology, augmented by MD-extracted diffusion parameters is able to predict key process parameters effect on the void volume, therefore optimizing the epitaxy conditions depending the product MTS. At the same time, at early stages of technology development it is possible to determine process margins and the tolerance for process variation and therefore reduce technology process parameter optimization space, reducing number of wafers that have to be spent for pathfinding lots.

IV. Conclusions

In this work, we have developed a multiscale atomistic simulation methodology that combines KMC epitaxy simulation, KMCRay precursor molecules tracing algorithm, and MD simulations for extraction of key model parameters. Our new epitaxy simulation framework enables accurate evaluation of novel advanced semiconductor device structures for potential epitaxy process issues and defects and provides efficient means for design margin extraction at early stages of technology development.

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