Atomistic analysis on random telegraph noise of SF transistors in sub-micrometer CIS pixels

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***Abstract*— This study presents a comprehensive model of random telegraph noise (RTN) in L-shaped source follower (SF) transistors within 0.5µm CMOS image sensor (CIS) pixels, using density functional theory (DFT) to analyze discrete traps at the Si/SiO_2 interface. Detailed measurements of the image signal spectrum influenced by RTN enhance our understanding of its characteristics and the atomistic origins and effectiveness of fluorine ion implantation (F-IIP) passivation for noise reduction are also explored. Monte Carlo simulations model the stochastic behavior of electrons, revealing significant RTN variations primarily due to interface traps. Passivation technology, including F-IIP and hydrogen passivation, are shown to mitigate these effects. The strong correlation between simulation and measurement results underscores the importance of understanding the atomistic configuration of defects at Si/SiO_2 and the shallow trench isolation (STI) interfaces for improving image quality in scaled-down sensors.**

Keywords*— *RTN, Pixel, CIS, Fluorine Passivation, DFT, SF, Atomistic Analysis

I. Introduction

RTN becomes a significant concern when scaling down sub-micrometer dynamic random access memories (DRAM), flash memories, and logic devices. In image sensors, RTN manifests as undesirable blinking spots in images, caused by electrons traveling through the transistor channel being captured and emitted by traps located at the Si/SiO_2 interface. This issue exacerbates as the pixel pitch is further reduced to enhance image resolution. Therefore, reducing RTN is a critical technology for scaling down pixels in CIS and enhancing image quality. While previous research focused on the physical modeling of RTN characteristics of individual transistors [1], this study extends to investigate interface traps that directly influence RTN through ab-initio calculations and measurements. Exploring the noise characteristics of image sensors with high-density features has enhanced our understanding of the impact of interface traps on RTN.

II. RTN Model of Image Sensor

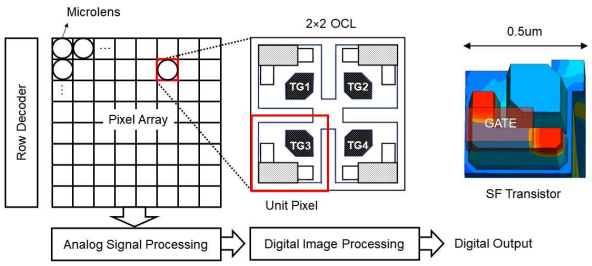
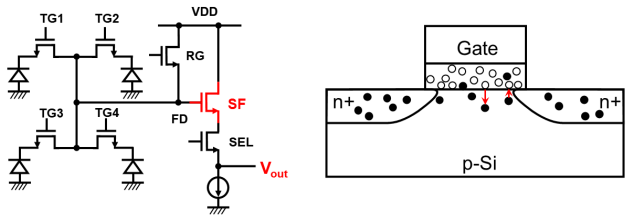


Fig. 1. Pixel array schematic in CIS, a unit pixel layout with 2×2 OCL, and SF transistor

Figure 1 depicts the layout of a unit pixel and the SF transistor structure within a pixel array featuring a 2×2 on-chip lens (OCL). The SF transistor has an L-shaped channel structure designed to maximize the gate area within the unit pixel structure. The active channel width is 80 nm, and the channel structure overlapping the gate extends up to 200 nm horizontally and 120 nm vertically.

Figure 2(a) shows the circuitry of an active pixel sensor, which includes seven transistors: four transfer gates (TGs), a reset gate (RG), a selector (SEL), and a SF transistor. The SF transistor transfers the gate signal from the floating diffusion (FD) to V_{out}, functioning in conjunction with a current source.

As shown in Fig. 2(b), electrons are captured by the empty trap sites or emitted from the occupied traps at the Si/SiO_2 interface or within the SiO_2 and the charge at the traps of the SF transistor affects the V_{out} signals.



(a) (b)

Fig. 2. (a) Circuit of seven nMOS transistors (TGs, SF, RG, SEL) in 2×2 OCL. The electrons created by photodiode modulates the gate bias of SF transistor and it changes the output signal (V_{out}). (b) The trapping and de-trapping process of electrons across the gate oxide interface in the SF transistor

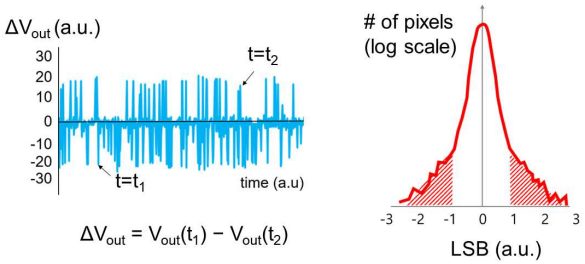


Fig. 3. The left graph shows time-varying noise signal and schematics of the correlated double sampling. The right figure shows a histogram of RTN at dark condition and the decaying tail means the stochastic nature of RTN.

The V_{out} signals are converted to image through the correlated double sampling (CDS) to cancel out offset noise. However, this process does not eliminate low-frequency flickering noise originating from the differential analog circuit and SF transistor. We define the RTN measurement metric as the probability of a given pixel generating ΔV_{out} above a certain threshold, as shown in Fig. 3.

$$P_{c,e} = \frac{1}{\tau_{c,e}} \exp\left(\frac{-t}{\tau_{c/e}}\right) \quad (1)$$

$$f_t = \left[1 + \exp\left(\frac{E_t - E_f}{kT}\right)\right]^{-1} \quad (2)$$

$$\tau_c^{-1} = c_n n_s P_t f_t \quad (3)$$

$$\tau_e^{-1} = c_n n_s P_t (1 - f_t) \quad (4)$$

$$\frac{\tau_c}{\tau_e} = \mathrm{g} \exp\left(\frac{E_t - E_f}{kT}\right) \quad (5)$$

$$P_T = \exp\left[-\frac{4\sqrt{2\,m^*}}{3\,\hbar\,qE_o}\left(\varphi_t^{\,3/2} - \varphi_c^{\,3/2}\right)\right] \quad (6)$$

Stochastic behavior of electrons at the Si/SiO_2 interface of SF transistors is simulated with a Monte Carlo technique, where the capture time τ_c and the emission time τ_e of each trap are calculated by the mean of SRH statistics as shown in (1)-(5) [2]. Equation (1) describes the capture and emission probability. f_t is the Fermi-Dirac distribution function, E_t is the trap energy, and E_f is the quasi-Fermi energy. In (4), n_s is the surface carrier density, and c_n is the capture coefficient. Equation (6) describes the tunneling probability from WKB theory. E_O is the oxide electric field, $\hbar$ is the Planck's constant, q is the electron charge, and m^* is the effective mass of an electron. φ_c represents the band offset between the conduction band edge and the potential barrier of the SiO_2 insulator, while φ_t denotes the energy difference between the trap energy and the bent conduction band edge energy. E_c and E_v are the conduction and valence band edges, as shown in Fig. 4.

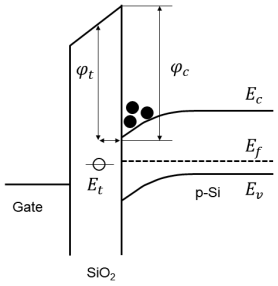


Fig. 4. Band diagram of Poly-Si Gate/SiO_2/Si structure for nMOS transistor

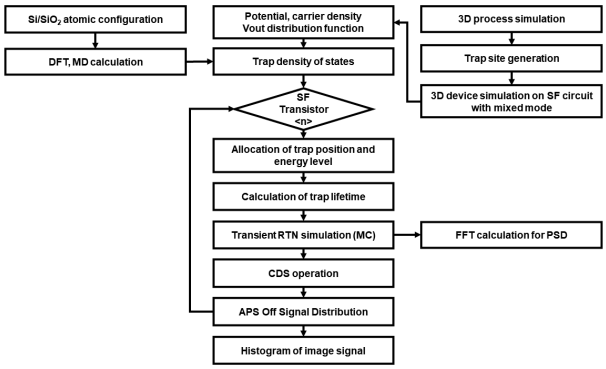


Fig. 5. Schematic diagram of transient RTN simulator for CIS.

Figure 5 presents a schematic diagram of the transient RTN simulation for a pixel array. The block labeled "APS Off Signal Distribution" in the diagram illustrates the signal distribution resulting from the differential analog circuits and digital blocks. This distribution is derived from measurements where noise signals from the SF transistors have been completely removed. The measured distribution is implemented in the simulation flow using the Monte Carlo method.

Figure 6 shows both the measurement results with the SF transistor noise removed (solid line, APS off) and the typical RTN measurement results that include noise from the SF transistors (dashed line).

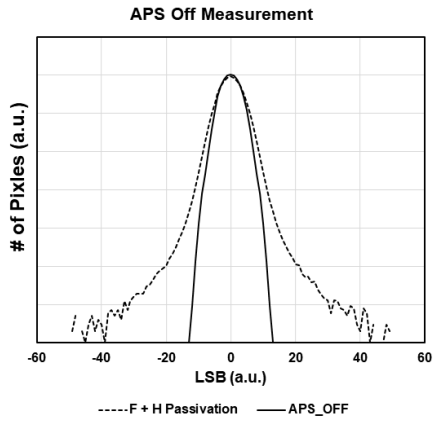


Fig. 6. The solid line represents the signal measurement after removing the flickering noise from the SF transistors (APS off). The dashed line depicts a typical RTN measurement that includes noise from the SF transistors.

The position and energy distribution of traps at the Si/SiO_2 interface under the Poly-Si gate are defined using random variables. The distribution of the density of interface traps (D_{it}) and the trap distribution are convolved to account for the D_{it} dispersion characteristics of each trap. Since the silicon channel edge region is expected to have a high defect level due to damage from the STI etch process, the edge and the central regions are separately defined for calibration. This is illustrated schematically in Fig. 7.

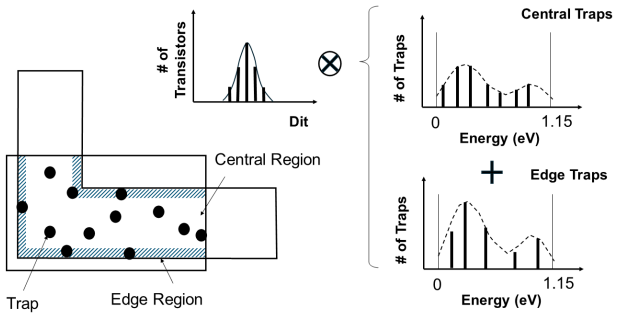


Fig. 7. The schematic on the left illustrates the definition of edge and central regions to address the increase in traps due to etch damage in the silicon channel. The diagrams on the right show the method for defining traps in terms of energy distribution and spatial location, using convolution to account for the D_{it} distribution characteristics.

III. F-IIP Passivation Effect

The F-IIP passivation is a crucial process for reducing flickering noise along with hydrogen passivation. Fluorine is implanted into the Poly-Si layer after the gate formation process. The segregated F atoms immunize defect sites at the gate oxide interface during thermal processes, as shown in Fig. 8.

DFT calculations show that F atoms reconstruct defect structures at the Si/SiO_2 interface as shown in Fig. 9(a). The structure is one of over 30 Si and amorphous SiO_2 interface structures and is a representative example, demonstrating a reduction of the originally existing three defects at the Si/SiO_2 interface to a single defect.

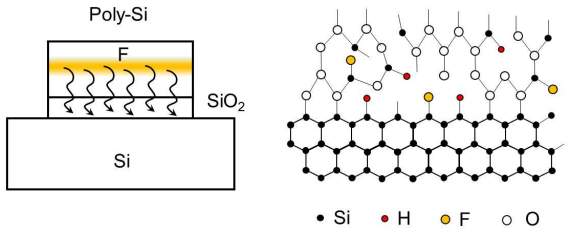


Fig. 8. The left image illustrates the process of fluorine, introduced by implantation into the Poly-Si layer, diffusing down to the SiO_2 and Si interface and passivating defect sites through heat treatment. The right image shows a schematic of the Si and SiO_2 interface atomic structure with dangling bonds passivated by hydrogen and fluorine.

Before passivation, trap densities are higher near the conduction band than the valence band, consistent with the observed double-peak shape near the Si band edges [5]. After passivation with F-IIP, D_{it} significantly decreases, as illustrated in Fig. 9(b). A similar reduction trend is also observed when simultaneous passivation with fluorine and hydrogen is performed. Furthermore, the RTN characteristics are slightly improved when fluorine and hydrogen are used together for passivation compared to when each is used alone.

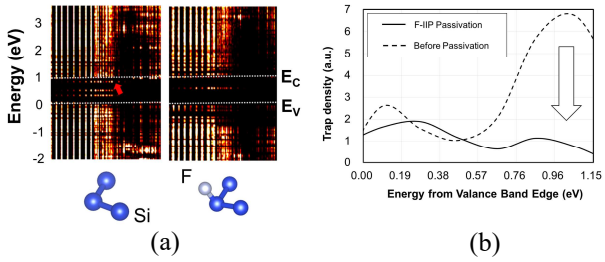


Fig. 9. (a) The figures demonstrate the outcomes of the electron system before F-IIP passivation (left) and after F-IIP passivation, resulting in the disappearance of traps (right). (b) The graph shows the trap density of 30 systems with a dirty Si/SiO_2 interface (dashed line) and the density of states (DOS) of the electron structure after passivation with F-IIP (solid line). The dashed line represents the trap DOS in unpassivated systems, while the solid line indicates the improved DOS following passivation.

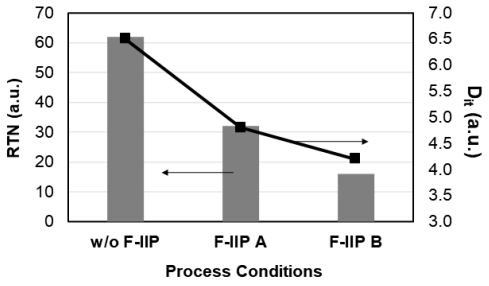


Fig. 10. The graph presents RTN and D_{it} measurement results dependent on various F-IIP passivation conditions.

Figure 10 shows D_{it} and RTN measurement results after F-IIP passivation. These results indicate that RTN values change under various F-IIP conditions, and the improvement in RTN with the reduction of D_{it} suggests that the decrease in defects is crucial for enhancing RTN characteristics.

IV. RTN Simulation Results

Depicted in Fig. 11, V_{out} variation is obtained from a 3D process and device TCAD simulation. The distribution function dependent on the location of a single electron defect inside the oxide is used in our simulation.

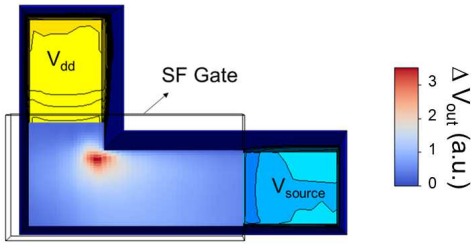


Fig. 11. ΔV_{out} distribution plot by the location of a single electron occupied at Si/SiO_2 interface.

As shown in Fig. 12, for example, ΔV_{out} reaches a higher value when five electron traps are located at a STI corner, compared to randomly assigned five electrons at the Si/SiO_2 interface in the channel area. This result suggests that the presence of statistically captured electrons in certain trap sites, positioned along the main current path, leads to significant voltage variations, serving as the primary cause of deteriorating RTN.

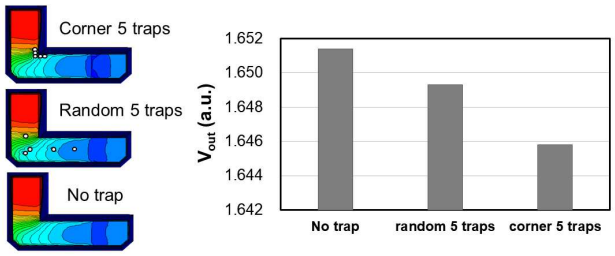
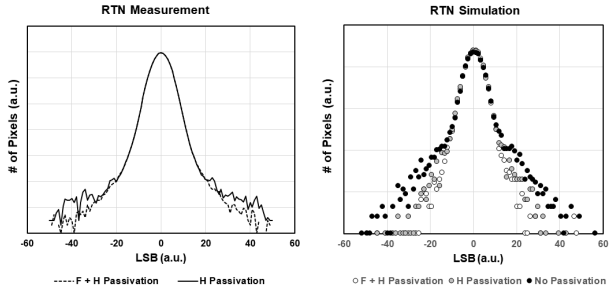


Fig. 12. Simulation results of V_{out} values and potential profiles are provided for three scenarios: when no electrons are trapped, when five electrons are randomly distributed in the Si/SiO_2 channel, and when five electrons are gathered in the corner region.

Figure 13(a) shows the measurement results, representing the difference between using F-IIP passivation with hydrogen passivation versus only hydrogen passivation. Figure 13(b) illustrates the simulation results comparing the F-IIP passivation model following hydrogen passivation with the hydrogen passivation model alone. The comparison of RTN measurements and simulation results reveals a close match in histogram shape. Further analysis indicates that the RTN tail shape is primarily influenced by trap energy levels, trap density, and the morphology of specific areas, such as the edges of STI.



(a) (b)

Fig. 13. (a) RTN signal measurements comparing F-IIP passivation with hydrogen passivation versus hydrogen passivation alone. (b) RTN histogram from simulations showing the comparison between the F-IIP and hydrogen passivation models.

V. Conclusion

A novel simulation methodology for RTN in image sensors is presented. The model demonstrates a strong correlation with RTN measurements on L-shaped SF transistors in 0.5µm unit pixels of CIS. We show that the significant variation in RTN is primarily induced by edge interface traps, and the microscopic origins of passivation are also investigated. These results indicate that the RTN behavior of a pixel array in CIS accurately reflects the atomistic configuration of defects at Si/SiO_2 and STI interfaces.

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