A TCAD to SPICE Simulation Framework for Analysis of Device to Circuit BTI and HCD Aging

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Invited Paper

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***Abstract*— Time kinetics of FET aging due to BTI and HCD are simulated by identical physical models in standalone and TCAD frameworks, and calibrated using experimental data from GAA SNS p- and n- FETs. The calibrated standalone physical models are used in a circuit aging simulator, making it compatible with cycle-by-cycle input excitations. The circuit simulator is used to estimate aging under DVFS and random input activity. Results are compared against conventional circuit aging simulation, and the significance of cycle-by-cycle simulation is highlighted.**

***Index Terms*— GAA SNS FET, BTI, HCD, TCAD, SPICE**

I. Introduction

Parametric shift due to Bias Temperature Instability (BTI) and Hot Carrier Degradation (HCD) is an important reliability concern in Gate All Around Stacked Nano Sheet (GAA-SNS) p- and n- channel FETs [1]-[4]. The Self-Heating (SH) effect-related temperature (T) rise is a concern due to high thermal resistance of these confined channel devices [5], [6], which in turn exacerbates the BTI and HCD impact due to their positive T activation [1]-[4]. In a digital logic circuit under operation (AC), BTI impacts the on/off phases while HCD impacts the transitions between on and off phases [7], [8]. In device level (DC), BTI is tested at non-zero gate (V_G) and zero drain (V_D) bias, but HCD at various V_G/V_D combinations, where BTI and HCD get coupled, and SH-related T-rise has a stronger impact [1], [2]. The BTI and intrinsic HCD (from the isolation of BTI and HCD) time kinetics at various V_G, V_D, and T are modeled at device level respectively by BTI Analysis Tool (BAT) and Hot Carrier Analysis Tool (HCAT), in standalone and TCAD implementations [1]-[4], [9], [10]. The standalone BAT and HCAT are utilized in Circuit Aging Reliability Analysis Tool (CARAT), a cycle-by-cycle circuit aging simulation platform, and used to study the impact of Dynamic Voltage Frequency Scaling (DVFS) and random input activity in various digital circuits [9]-[12]. In this paper, additional results are shown to establish the necessity of the proposed device-to-circuit flow.

II. Device Modeling Frameworks

The BAT framework, implemented as standalone version and in Sentaurus Device [13], is shown in Fig.1. It uses the Reaction-Diffusion (RD) model for interface trap generation, and the Transient Trap Occupancy Model (TTOM) for their charged state or occupancy and contribution (ΔV_{IT}). TTOM is calculated by the Activated Barrier Double Well Thermionic (ABDWT) model, the latter is also used for charge trapping in pre-existing defects, either holes (ΔV_{HT}) for Negative BTI (NBTI) or electrons (ΔV_{ET}) for Positive BTI (PBTI) in p- and n- FETs respectively. The Reaction-Diffusion-Drift (RDD) model is used for bulk trap generation (ΔV_{OT}). The threshold voltage shift (ΔV_T) is a sum of uncorrelated contribution from ΔV_{IT}, ΔV_{OT} and ΔV_{HT} or ΔV_{ET}. The RD and RDD models are implemented by the Capture-Emission De-passivation (CED) and Multi-State Configuration (MSC) modules in TCAD.

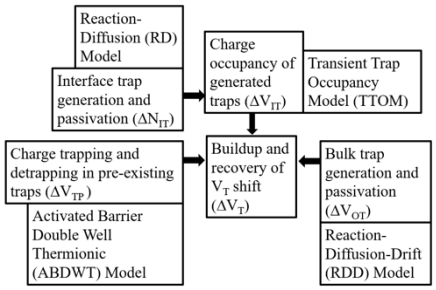


Fig.1. Schematic of BAT framework (ΔV_{TP} is ΔV_{HT} for NBTI and ΔV_{ET} for PBTI), implemented in both standalone and TCAD versions [3].

In RDD model, Fig.2, Hydrogen (H) passivated bonds (X-H) are dissociated during stress, the released H atoms diffuse and initiate reactions to break additional bonds (Y-H, Z-H/O) in the gate insulator of a FET. The resulting H_2 molecule and ionic (H_2^+, OH^-) species diffuse/drift in the gate and backend. The RD model is a subset of RDD model (no ion generation). Charges in broken bonds (X-, Y-, Z-) cause device parametric shift. Reverse processes are triggered after removal of stress.

In ABDWT model, two stable energy states, E_1 (reservoir) and E_2 (trap), are separated by a barrier (E_B) that is normally distributed in energy, having Arrhenius T-activated mean and spread, Fig.2. Due to barrier lowering during stress, charge transfer from E_1 to E_2 is initiated, increasing the occupancy of E_2; reverse process happens after removal of stress.

Modeling of HCD time kinetics involves calculating the following in TCAD: (a) carrier and lattice heating, (b) trap generation, and (c) impact of charges in the generated traps on parametric shift. The simulated carrier and lattice heating in 2-D equivalent cross-sectional p-FET and n-FET structures is shown, Fig.3, coupled Spherical Harmonics Expansion and Thermodynamic modules of Sentaurus Device are used. Trap

generation is calculated using the RDD model implemented by the CED-MSC framework. A combined energy-thermionic model is used for CED [4].

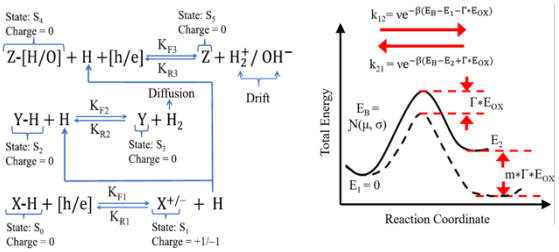


Fig.2. Schematic of (a) RDD and (b) ABDWT models, used respectively for time kinetics of trap generation and trapping, implemented in both standalone and TCAD versions [3].

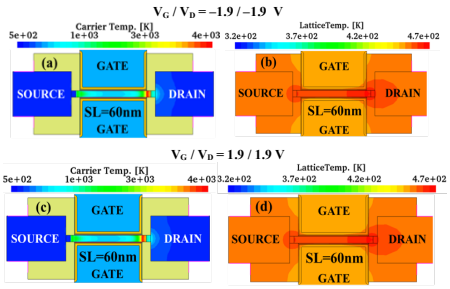


Fig.3. TCAD simulated (a, c) carrier and (b, d) lattice temperature profiles in 2D cross section of GAA SNS (a, b) p-FET and (c, d) n-FET.

III. Device Modeling Results

Fig.4 plots the measured and TCAD modeled ΔV_T during and after NBTI and PBTI stress (V_D=0), with subcomponents. ΔV_{HT} and ΔV_{ET} are small in production-quality devices, they saturate fast during stress and recover fast after stress. ΔV_{IT} and ΔV_{OT} evolve gradually and show power-law at long time during stress, respectively with long-time slope (n) of ~1/6 and ~1/4. ΔV_{IT} recovery is over an extended timescale, due to faster occupancy change and slower trap passivation, and the recovery of ΔV_{OT} is negligible. TCAD-implemented BAT is used for modeling NBTI and PBTI stress and post-stress ΔV_T time kinetics data measured at V_G x T stress conditions; a few cases are shown in Fig.5 (more examples in [9]). Standalone BAT has identical results as TCAD, not explicitly shown.

BTI and HCD modules are simultaneously used to model the measured ΔV_T during and after HCD stress (non-zero V_D). The setup is validated at multiple V_G and V_D stress conditions (V_G <, = and > V_D), as shown in Fig.6 and Fig.7 for p- and n-FET respectively. BTI contribution to overall ΔV_T under HCD stress is larger in p-FET than n-FET, as NBTI is higher than PBTI. However, the intrinsic HCD contribution to overall ΔV_T under HCD stress is higher in n-FET than p-FET. The post-stress recovery is due to that of BTI only, while intrinsic HCD does not recover. TCAD implemented BAT and HCAT are used to model HCD stress and post-stress ΔV_T time kinetics in p- and n- FETs at V_G x V_D stress conditions; a few cases are shown in Fig.8 (more examples in [9]). Standalone HCAT has identical results as TCAD, not explicitly shown.

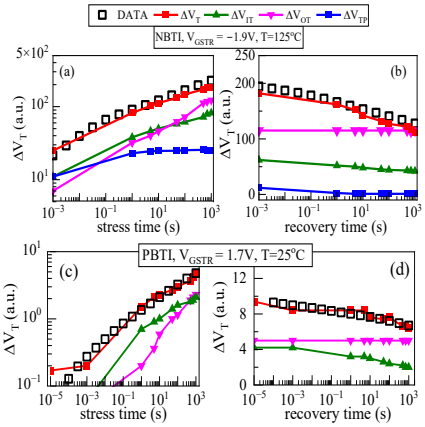


Fig. 4. Measured (symbols) and TCAD modeled (line + symbols) ΔV_T time kinetics in (a, b) p-FET and (c, d) n-FET for BTI (a, c) during and (b, d) after stress, the BAT subcomponents are also shown.

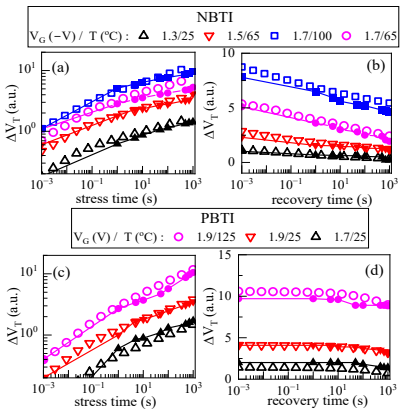


Fig.5. Measured (symbols) and TCAD modeled (line + symbols) ΔV_T time kinetics in (a, b) p-FET and (c, d) n-FET, (a, c) during and (b, d) after stress, for BTI under multiple V_G / T conditions.

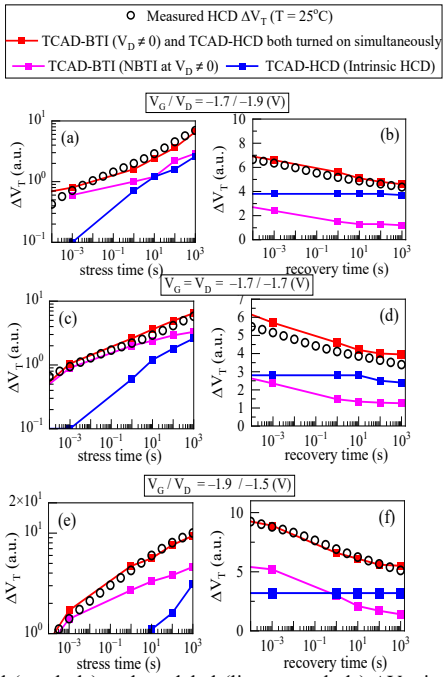


Fig.6. Measured (symbols) and modeled (line + symbols) ΔV_T time kinetics (a, c, e) during and (b, d, f) after HCD stress in p-FET; the TCAD-BAT and TCAD-HCD modules are individually and also simultaneously turned on.

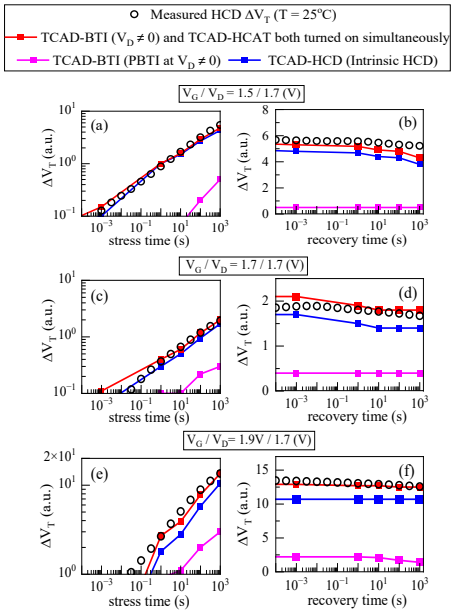


Fig.7. Measured (symbols) and modeled (line + symbols) ΔV_T time kinetics (a, c, e) during and (b, d, f) after HCD stress in n-FET; the TCAD-BAT and TCAD-HCD modules are individually and also simultaneously turned on.

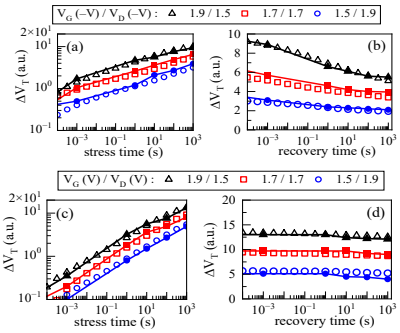


Fig.8. Measured (symbols) and modeled (line + symbols) ΔV_T time kinetics for (a, b) p-FET and (c, d) n-FET under multiple V_G/V_D (V_G >, =, < V_D) conditions (a, c) during and (b, d) after HCD stress. TCAD-BAT and TCAD-HCD modules simultaneously turned on.

Table-I lists projected ΔV_T at various V_G/V_D conditions at End-Of-Life (EOL) of 10 years, calculated by the calibrated BTI and HCD models.

IV. Circuit Modeling Framework

Fig.9 shows the CARAT framework, where the entire flow is automated and executed by the Control Framework (CF). First, HSPICE [14] is run with user defined Netlist and fresh p- and n- FET Model Cards (MC). The terminal biases of each FET of a circuit are grabbed by the Waveform Grabber (WG), and are shaped for BTI (trapezoidal to rectangular) and HCD (on to off transitions to staircase) analysis by the Pulse Shaper (PS). BAT and HCAT (having similar time kinetics as TCAD) modules calculate ΔV_T for BTI and HCD respectively, and the Degradation Extrapolator (DE) is used to project the cycle-by-cycle simulation results under AC pulse to EOL by a suitable DC reference (note, HSPICE AC simulation is run up to 100ns or 1µs). The Model Card Modifier (MM) modifies MC of all FETs with EOL ΔV_T, and a HSPICE simulation is run with updated MC. The fresh and aged simulations are compared for timing degradation.

V_G (V)	ΔV_T (in a.u.) for PMOS / NMOS for V_D=			
	0V	0.8V	1.05V	1.4V
0.8	19 / 1	23 / 22	30 / 46	49 / 97
1.05	47 / 5	60 / 56	81 / 110	138 / 227
1.4	148 / 42	203 / 193	288 / 349	506 / 651

Table-I: Extrapolated ΔV_T at EOL for various V_G / V_D (V_G >, =, < V_D) conditions at fixed T = 65° C for p-FET / n-FET.

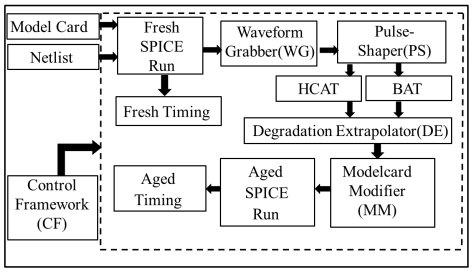


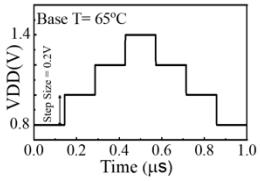
Fig.9. CARAT Framework using standalone BAT and HCAT models that are calibrated with TCAD [3].

V. Circuit Modeling Results

Inverter, NAND, and NOR-based 21-stage Ring Oscillator (RO) circuits are simulated with CARAT at various fixed V_{DD}, and under DVFS conditions where V_{DD} increases and reduces in steps between a minimum and maximum range; resulting frequency degradation (Δf) are listed respectively in Tables II and III. Simulations are done with only NBTI, both NBTI and PBTI (BTI), BTI plus only n-HCD, and all (BTI plus n- and p-HCD). NBTI in p-FET and HCD in n-FET dominate device DC stress in Table-I, while RO results are dominated by NBTI when all the mechanisms are turned on, Tables II and III. The HCD impact becomes more relevant at higher V_{DD} conditions. Moreover, none of the fixed V_{DD} cases can reproduce DVFS results, showing the significance of cycle-by-cycle simulation.

Cases ⇩ / VDD (V) ⇨	% Δf for 21 stage RO using								
	Inverter			NAND			NOR		
	0.8	1.05	1.4	0.8	1.05	1.4	0.8	1.05	1.4
NBTI	1.6	4.1	14	1.6	4.3	14.2	1.6	4.6	15.8
BTI	1.7	4.2	17.4	1.8	4.7	17.4	1.8	4.9	18.7
BTI+nHCD	1.9	5.4	20.4	1.97	5.2	20.8	2.05	5.5	22.7
All	2	5.7	22.4	2.02	5.4	23.1	2.07	5.7	25

Table-II: Δf (%) for Inverter, NAND, and NOR-based RO with the application of fixed V_{DD} at T=65°C for NBTI, BTI, BTI + n-HCD, and BTI + HCD (All).



DVFS Conditions	% Δf for 21-stage Ring Oscillator using		
	Inverter	NAND	NOR
NBTI	8.8	9	9.7
BTI	10.9	11	11.5
BTI+nHCD	12.6	12.6	13.6
BTI+HCD	13.7	13.6	14.7

Table-III: Δf (%) for Inverter, NAND, and NOR-based RO with application of DVFS waveform on left for NBTI, BTI, BTI + n-HCD, and BTI + HCD (All).

Fig.10 shows XOR gates realized by various combinations of NAND and NOR gates, and random waveform patterns that are used as input excitations. Results are listed in Table-IV, for only BTI and BTI plus HCD conditions for both p- and n-FETs, and for symmetric (*e.g.*, AA) and asymmetric (*e.g.*, AB) input pulses. All waveforms have an effective duty of 50%, and therefore, the random activity results are compared to RO-like pulses. The symmetric cases show similar results as RO-like pulses, while all asymmetric cases show higher rise delay degradation ($\Delta\tau_{RISE}$) but lower fall delay degradation ($\Delta\tau_{FALL}$) compared to RO-like pulses. BTI dominates over HCD for all cases (implementation and pulse type), but the relative impact of HCD is higher for NOR2 based implementation.

Higher $\Delta\tau_{RISE}$ than $\Delta\tau_{FALL}$ is observed for symmetric cases and RO-like pulse for only NAND based implementation, and for asymmetric cases for all the three NAND and NOR based implementations. However, higher $\Delta\tau_{FALL}$ than $\Delta\tau_{RISE}$ is seen for symmetric cases and RO-like pulse for both NOR based implementations. The results show limitation of effective duty approach under random input activity, once again justifying the need for cycle-by-cycle analysis.

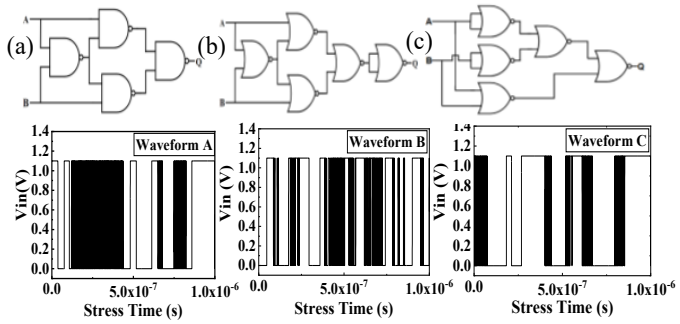


Fig.10 (top). Circuit Diagram for XOR with (a) NAND, (b) NOR1 and (c) NOR2, (bottom) activity waveforms applied to the above circuits.

Cases	Propagation Delay degradation, $\Delta\tau/\tau$ (in a.u.) for XOR with NAND / NOR1 / NOR2 for the following cases			
	$\Delta\tau_{RISE-BTI}$	$\Delta\tau_{FALL-BTI}$	$\Delta\tau_{RISE-BTI+HCD}$	$\Delta\tau_{FALL-BTI+HCD}$
AA	21 / 19 / 20.3	15 / 27 / 24	23 / 19.2 / 21.4	16 / 29.5 / 30.4
AB	28 / 28.7 / 25.4	10.6 / 18.2 / 17	28.3 / 30.5 / 26.4	14.3 / 22 / 24.4
AC	26.6 / 27.8 / 25	11.7 / 19.4 / 18	29 / 29.8 / 26	14 / 23 / 25.6
BA	27.3 / 28.5 / 25.5	10.8 / 18 / 17.5	29.2 / 30.6 / 26.5	14 / 22 / 24.8
BB	21.7 / 17.5 / 20.2	14.8 / 28.5 / 24.3	23 / 19.7 / 21	15.6 / 28.6 / 32
BC	28.4 / 28.5 / 25.5	10.7 / 18 / 17.5	29 / 31.7 / 26.5	14.7 / 22 / 24
CA	26.6 / 28.6 / 25.2	11.5 / 20.2 / 18.2	28 / 29.7 / 26	15 / 24 / 25
CB	28 / 28.6 / 25.5	11 / 18.3 / 16.5	28.2 / 30.5 / 26.7	14.6 / 22 / 24.4
CC	20.6 / 19 / 20.3	15.8 / 28.4 / 24	22.2 / 19.2 / 21	16.7 / 29 / 31.4
RO-like	20.6 / 16.3 / 21.2	15.6 / 28 / 25.2	22.6 / 17.8 / 21.8	16.4 / 28.8 / 34.4

Table-IV: Propagation delay degradation % of XOR from Fig.10 (top) for BTI and BTI+HCD with the application of waveforms from Fig.10 (bottom).

VI. Conclusions

The use of identical physical models, standalone BAT and HCAT, for the time kinetics of BTI and HCD in device and circuit simulation removes the need of aging compact models, which is a known challenge especially for BTI recovery. Due to identical physics governing standalone and TCAD versions, isolation of intrinsic HCD from measured HCD data, where BTI also contributes, can be straightforwardly used into circuit simulation. The cycle-by-cycle capability of CARAT provides a more realistic assessment of delay degradations as compared to simple methods like fixed V_{DD} and effective duty approach, respectively for DVFS and random input activities.

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