A self-consistent tiling method for chip-scale stress simulation

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***Abstract*—We present a self-consistent boundary treatment method to account for the long-range stress effects in chip-scale stress simulations. The long range effects are superposed onto the stress solution of the individual tiles as the boundary displacements in a self-consistent manner. The model concept is rigorously tested and applied to a realistic example to demonstrate large-scale simulation capability. Chip-scale and even wafer-scale simulations can be achieved by the nested application of the proposed method. An important potential application would be mask design improvement to avoid stress-related device failure.**

***Index Terms*—stress, FEM, self-consistent tiling**

I. Introduction

As two-dimensional device scaling approaches to the physical limit, three-dimensional (3D) stacking [1]–[5] has been persued to continue increasing the device density and performance of a chip. In 3D devices, one of the major failure source is the mechanical stress, such as fin leaning during fin isolation process in logic devices [6], delamination of stacked multi-layer [7], and crack formation in back-end-of-line (BEOL) stacks [8].

To avoid such failures, the layout design needs to be improved based on the results of an accurate mechanical stress simulation. However, the current stress simulation method based on the conventional finite element method (FEM) is limited by the mesh size [9], in which the small feature size ($\sim$10 nm) cannot be resolved in a chip-scale ($\sim$cm) simulation [10], [11]. Therefore, it requires a scale-bridging method to connect the two scales using some type of homogenization of material and mesh coarsening. The representative volume element (RVE) method and its variations are well known methodologies [12], [13] and recently a tiling method successfully predicted BEOL crack probability using mesh coarsening and domain decomposition [10], [11]. In the tiling method ([10], [11]), the decomposed tiles have an overlapping region shared with the neigbhor tiles to reduce the boundary effects introduced with domain decomposition. In this work, we present a self-consistent tiling method without the overlapping region to remove the artifically introduced boundary effects.

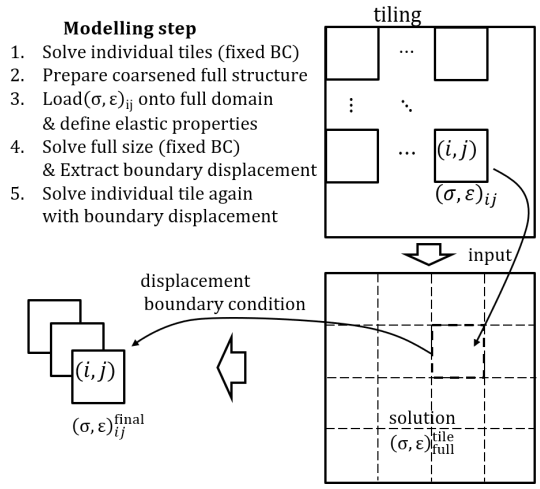

Fig. 1. Simulation steps. In this work, full size one-shot simulation is performed before step-1 to prepare the exact solutions for model evaluation.

II. Methods

Fig. 1 illustrates the modeling steps. In the beginning, a large chip-scale structure is divided into many small tiles which are simulated individually with a fine mesh and the fixed boundary conditions (step-1). With the fixed boundary condition, the normal component of the displacement is set to zero. The next step is preparing the mesh coarsened full structure (step-2). Then the individual tile solutions $(\sigma, \varepsilon)_{ij}$, the results of step-1, are loaded onto the mesh coarsened full structure as an input value (step-3). Elastic properties of coarsended mesh needs to be redefined to represent the average modulus correctly. The full structure is solved with the tiled individual solutions as the input, and the displacement along the each tile boundaries is extracted (step-4). Finally, the individual tile is solved one more time with a different boundary condition from the step-1. At step-5, each tile boundary node has the fixed displacement value acquired from the step-4.

In this work, we used the conventional finite element methods implemented with the weak form of the force equilibration equation [14] in our in-house stress simulator. The boundary condition at step-1 is not important because its contribution to the solution pair $(\sigma, \varepsilon)_{ij}$ is automatically removed with the new boundary conditions at step-4, which was demonstrated in [15].

Before applying the model to a real application, we performed a validation simulation to test if the tiled results are the exactly same as the full simulation results when coarsening is skipped. The model validation steps are descibed in Fig. 2. Validation simulation was performed using a simple structure composed of 3×3 tiles having a rectangular internal structure. Random intrinsic stress was assigned to the host material of each tile as shown in Fig. 3a). Fig. 3 shows that the self-consistent tiling method produces identical results to the full simulation results. Although the step-4 results are not shown here, it is also same as the full simulation results (step-1), which justifies using single tile solution pair,$(\sigma, \varepsilon)_{ij}$, as the input of the step-4 instead of the original initial intrinsic stress even with the changed boundary conditions at the tile boundaries. For full size simulations (step-1 and step-4), we also tested the free-standing boundary condition to simulate the free chip boundary after dicing wafer, in which only minimal number of degrees of freedom is removed to prevent translation and rotation of the solution. The results of step-1, step-4, and step-5 are still identical. Fig 3 g) and h) shows the stress and displacement distribution with chip deformation with the free-standing boundary condition.

III. Applications and Discussions

We applied the self-consistent tiling method to a layout whose schematic is shown in Fig. 4. It consists of two materials: metal and oxide. Full structural details cannot be resolved in this scale and thus only schematic is provided. Initial intrinsic stress is assigned as the source of the stress to represent the thermal mismatch stress which is progressively

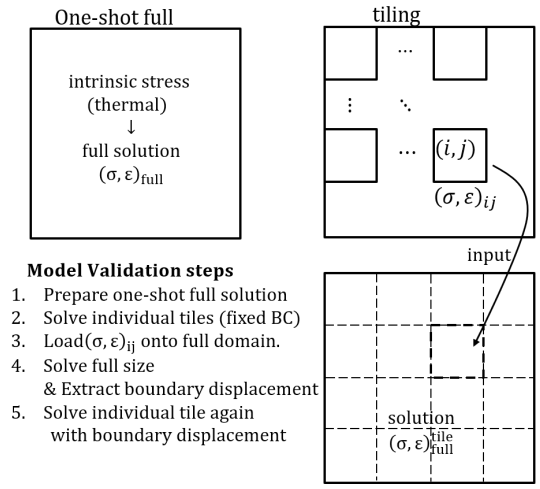

Fig. 2. Model validation steps for self-consistent tiling method.

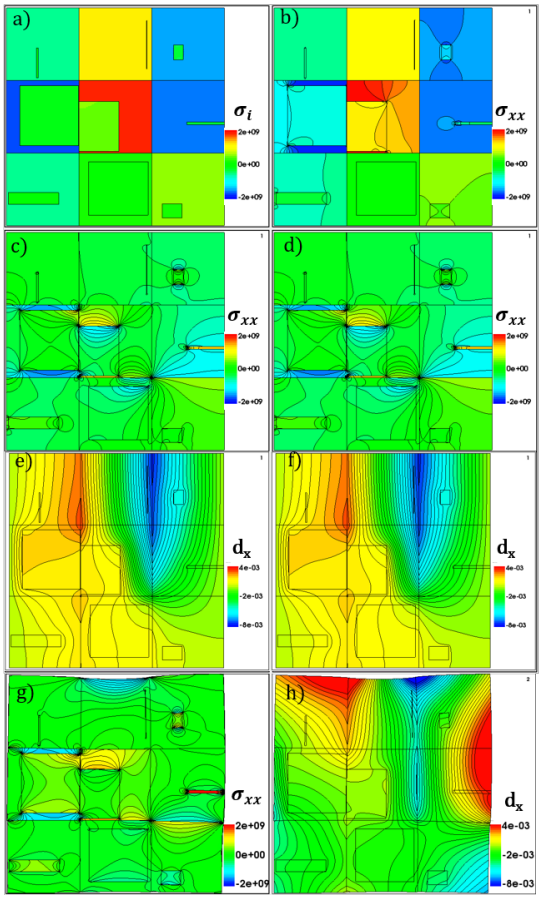

Fig. 3. Self-consistency test results. a) Initial intrinsic stress (σ_i) distribution. b) Stress-xx (σ_{xx}) distribution of individual tile with the fixed boundary condition (step-2 in Fig.2). c) Stress-xx (σ_{xx}) distribution in full simulation (step-1 in Fig.2). d) Stress-xx (σ_{xx}) distribution with tiling method (step-5 in Fig.2). e) Displacement-x (d_x) in full simulation (step-1). The unit is μm. f) Displacement-x with the self-consistent tiling method (step-5). g) Stress-xx (σ_{xx}) with free-standing boundary condition. h) Displacement-x with the free-standing boundary condition. The results confirm that step-1, step-4, and step-5 all produce the same results without mesh-coarsening. The boundary deformation is exaggerated by a factor 2 for better visualization in g) and h).

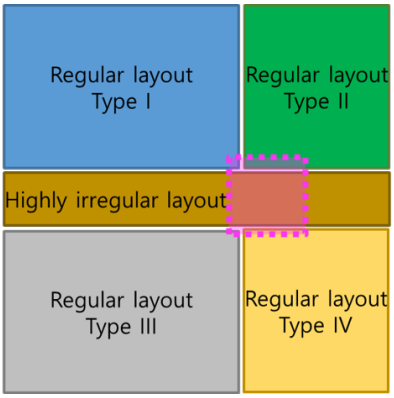

Fig. 4. Schematic of the test structure. The pink dotted box is the selected tile to present details of results in Fig 8.

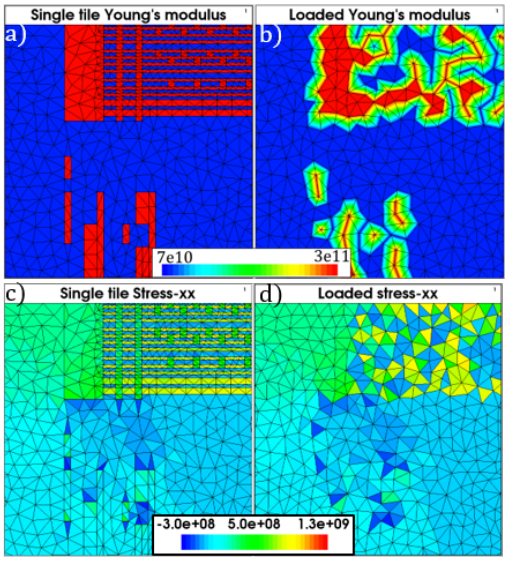

Fig. 5. Loading single tile results onto coarsened mesh. a) Young's modulus in the single tile. b) Interpolated Young's modulus in the coarsend structure. c) Stress-xx in the single tile result. d) Loaded stress-xx onto the mesh-coarsened structure.

built up during deposition, etch, and chemical-mechanical-planarization (CMP) cycles in real process [11]. Table I lists the parameter values used for the simulation. The parameter values were selected for demonstration purposes and not directly related to specific materials or processes.

TABLE I
MODEL PARAMETERS.

parameter	metal	oxide
intrinsic stress	1.6 GPas	-50 MPas
Young's modulus	300 GPas	70 GPas
Poisson ratio	0.2	0.17

The original mesh structure having 1.2 million nodes was decomposed into 5×5 tiles. Before solving individual tiles, full one-shot simulation was performed to prepare reference data for model evaluation. The original fine structure was coarsened to have $\sim$0.2 million nodes, and the elastic properties (Young's

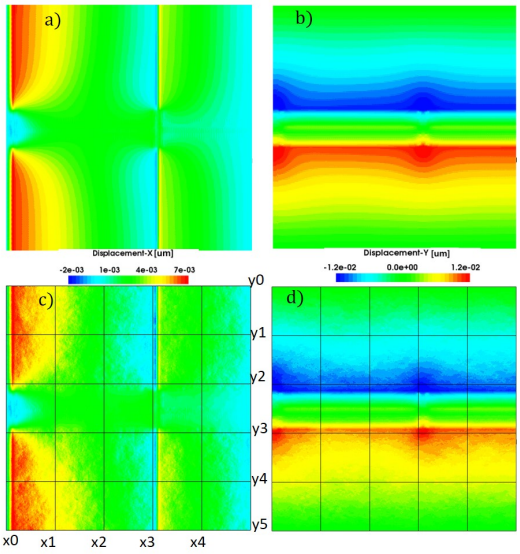

Fig. 6. Comparison of displacement components. Full simulation results (a and b) are compared with the results of tiling methods at step 4 (c and d).

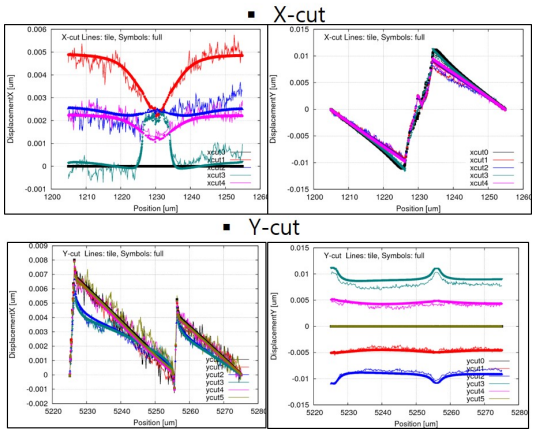

Fig. 7. Comparison of displacement at tile boundaries: x-cut positions and y-cut positions are shown in Fig. 6 c.

modulus and Poission ratio) were defined at each mesh node by interpolating the original value from the full mesh. The Young's modulus sampling example is shown in Fig. 5 a) and b). The Poisson ratio was sampled in the same way. In Fig. 6, the one-shot full simulation results are compared with the tiling results after step-4. Overall the displacement vector is well reproduced by the self-consistent tiling method. For quantitative comparison, each component of the displacement vector is compared along each tile boundary in the x-cut and y-cut plots (Fig. 7). Although the main purpose of the coarse mesh simulation (step-4) is to extract the displacement at the tile boundary, it gives a good agreement inside the tile as well at this level of coarsening. Finally, the final results at step-5 were compared with the exact solutions of the one-shot simulation (Fig. 8).

There are two error sources. The first one is mesh change occuring at tile decomposition. Unless the tile boundaries are

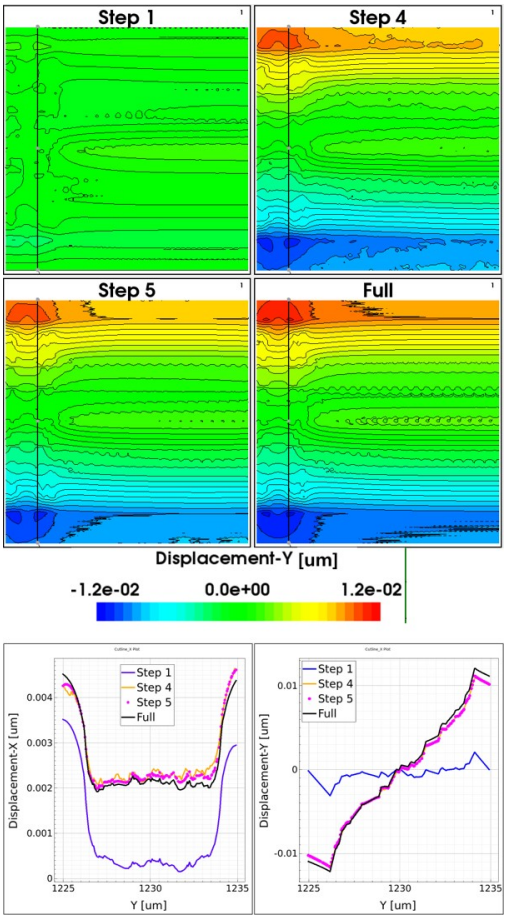

Fig. 8. Comparison of displacement components inside tile. The black solid line in the two dimensional contour plots represents the cut line along which the one-dimensional displacement is plotted.

exactly aligned with the mesh lines in the original layout, tile decomposition will modify the mesh near the tile boundary. If the original mesh is prepared carefully, this error can be removed as shown in our validation example. The second is the mesh coarsening which requires elastic property averaging and interpolation of loaded tile solutions. We tested two methods for the elastic property averaging. In one case, we assigned the volume-weighted average value to an entire tile. In the other case, the value at coarsened mesh node was interpolated from the original mesh 5b). The latter gives a better results for the coarsening level used in this work. This part can be further improved using more sophisticated RVE ([12]) or the stochastic volume element (SVE) model ([13]).

The bounary condition of the full size simulation (step-4) can be chosen depending on the desired manufacturing step to be simulated. Before dicing the wafer, the fixed boundary condition may be the appropriate choice. If wafer-scale displacement data is available at some selected locations on the wafer, applying a displacement boundary condition similar to step-5 is better. After the dicing process, the free-standing boundary condition would be the proper choice.

The self-consistent tiling method involves superposing long-range effects onto the single tile results in a self-consistent way, ensuring coherence and integrity of the solution in the overall tiling arrangement. When coarsening is applied multiple times in a nested loop, the simulation area increases by the power law to the number of applied coarsenings.

IV. Conclusion

We developed a scale-bridging stress simulation method to take the long-range stress effects into account by applying the displacement boundary condition in a self-consistent way. The model enables chip-scale or even wafer-scale stress simulations. An important application of the method can be predicting the stress hot spots for a given layout design, which can lead to optimization of the layout design before the fabrication process.

References

[1] R. Micheloni, S. Aritome, and L. Crippa, “Array architectures for 3-D NAND flash memories,” in Proceedings of the IEEE, vol.105, issue 9, September 2017.

[2] J. Ryckaert *et al.*, “The Complementary FET (CFET) for CMOS scaling beyond N3, in 2018 IEEE Symposium on VLSI Technology, pp.141-142, June 2018.

[3] A. Belmonte *et al.*, “Capacitor-less, long-retention (>400s) DRAM cell paving the way towards low-power and high-density monolithic 3D DRAM,” in 2020 IEEE International Electron Devices Meeting (IEDM), pp.609-612, December 2020.

[4] F. Hsu *et al.*, “3D X-DRAM: A novel 3D NAND-like DRAM cell and TCAD simulations,” in 16th IEEE International Memory Workshop (IMW), May 2024.

[5] H. Jun *et al.*, “HBM (High bandwidth memory) DRAM technology and architecture,” in 2017 IEEE International Memory Workshop (IMW), May 2017.

[6] P. Gencer, D. Tsamados, and V. Moros, “Fin bending due to stress and its simulation,” in 2013 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), September 2013.

[7] J. Kim, H. Kil, S. Lee, J. Park, and J. Park, “Interfacial delamination at multilayer thin films semiconductor devices,” ACS Omega 2022, 7, pp.25219-255228.

[8] S. Wang, L. Xue, H. Wang, R. Li, C. Sheng, Y. Sun, and S. Liu, “Research on BEOL failures of the chip-package interaction by shear tests of the bumps,” 22nd International Conference on Electronic Packaging Thechnology, 2021.

[9] K. Fischer, A. Pearce, X. Garcia-Teijeiro, A. Mallinson, I. Lloyd, S. Anderson, F. Gomez, S. Kisra, and A. Rodriguez-Herrera, “Seismic-scale finite element stress model of the surface. Geomechanics for energy and the environement,” vol.28, 100245, 2021.

[10] K. Yeom *et al.*, “Full chip stress model for flash BEOL crack failure risk analysis,” in 2023 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), September 2023.

[11] K. Yeom *et al.*, “Full chip stress model for defect formation risk analysis in multilayer structures,” in 2024 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), in press.

[12] T. Kanit, S. Forest, I. Galliet, V. Mounoury, and D. Jeulin, “Determination of the size of the representative volume element for random composites: statistical and numerical approach,” International Journal of Solids and Structures, vol.40, pp.3647-3679, 2003.

[13] J. Zhang, K. Liu, C. Luo, and A. Chattopadhyay, “Crack initiation and fatigue life prediction on aluminum lug joints using statistical volume elementbased multiscale modeling,” Journal of Intelligent Material Systems and Structure, vol. 24, issue 17, pp 2097-2109, 2012.

[14] A. J. Deeks and J. P. Wolf, “A virtual work derivation of the scaled boundary finite-element method for elastostatics,” Comput. Mech. 28, pp.489-504, 2002.

[15] C. Ahn, Y. Nishizawa, and W. Choi, “A finite element method to simulate dislocation stress: A general numerical solution for inclusion problems,” AIP Advances, vol.10, issue 1, 015111, 2019.