2024 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD) | 979-8-3315-1635-2/24/$31.00 ©2024 IEEE | DOI: 10.1109/SISPAD62626.2024.10732953

An Improved Overlap Capacitance Model for LDMOS Transistors based on the BSIM-BULK Framework

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***Abstract*—The gate-drain capacitance (C_{GD}) affects the input and output impedance of transistors, necessitating designers to consider it for proper matching and interfacing with other circuit elements. For Laterally Diffused Metal-Oxide-Semiconductor (LDMOS) transistors, the drift region overlap capacitance is a key contributor to C_{GD}. C_{GD} gradually decreases with drain voltage (V_D) and eventually saturates. However, before saturating, we observe a stepped decline in C_{GD} at higher V_D. This article provides physical insights into this step reduction of capacitance using Technology Computer-Aided Design (TCAD) simulations. Using the industry-standard BSIM-BULK model as a framework, we present an improved overlap capacitance model and validate it against measured LDMOS characteristics.**

***Index Terms*—BSIM-BULK, overlap, C_{GD}, and LDMOS.**

I. Introduction

LDMOS transistors are fundamental to circuits such as power amplifiers, switch-mode power supplies, and other electronic applications [1]–[4]. Fig. 1 (a) shows a simple schematic of an n-LDMOS transistor where a lightly doped n-drift region is connected between the gate edge and the drain terminal to sustain a high drain voltage (V_D). In BSIM-BULK, the drift region is modeled as a bias-dependent drift resistance (R_{drift}) connected between nodes D_i and D_{i1} as shown in the equivalent circuit diagram Fig. 1 (b) [5]. R_d and R_s are the drain and source contact resistances respectively. The drift region has two distinct regions: one under the thin gate oxide (L_{ov}) and the other under a thick oxide. The BSIM-BULK model, based on a physical charge-based core, calculates the capacitance of the intrinsic MOSFET and gate overlap drift region separately [6]. The capacitance equivalent of the LDMOS transistor is shown in Fig. 1 (c). In the absence of an inversion layer in the OFF state, the contribution of the intrinsic capacitance becomes negligible, and the overlap capacitance dominates. CGSO and CGDO denote the overlap capacitance contribution of the Lightly Doped Source/Drain (LDD) region, while CGDOV is the overlap capacitance contribution from the gate overlap on the drift region under the thin gate oxide. The gate-to-drain overlap capacitance in LDMOS transistors impacts the high-frequency response, the linearity of the power amplifiers, and the switching speed of the device. Therefore, accurate modeling of the overlap capacitance is essential for state-of-the-art technology [7], [8]. The existing BSIM-BULK model accurately captures the overlap capacitance due to the LDD region in low voltage MOSFETs [9]. Still, the existing overlap capacitance model of the drift region in BSIM-BULK does not capture the measured characteristics. With the application of V_D, C_{GD} gradually decreases and eventually saturates in the case of an LDD MOSFET. In our previous work [10], we provided a physical explanation and presented a compact model that accurately captures the capacitance under different bias conditions. However, in the case of an LDMOS transistor, the applied V_D is high, and we observe a step-like behavior in C_{GD} before it gets saturated. Numerous studies have focused on the capacitance behavior of the LDMOS transistor without

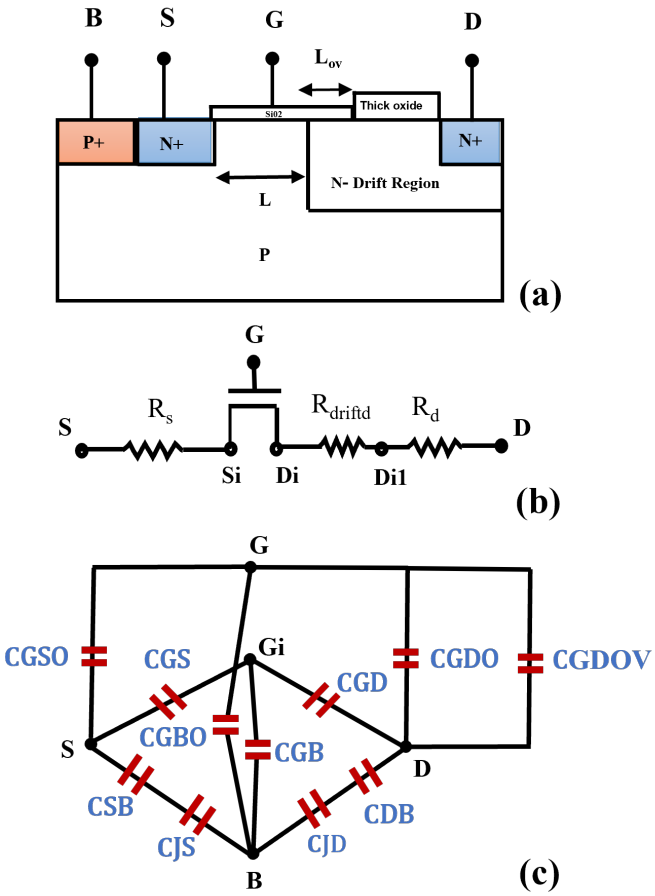

Fig. 1. (a) Simple schematic of an n-LDMOS transistor, (b) Its equivalent circuit. (c) Capacitance equivalent of an LDMOS transistor for both intrinsic and extrinsic MOSFET.

discussing the step behavior in C_{GD} or the underlying physics that explains the phenomenon [11]–[13]. In [14], the step behavior is modeled by limiting the applied V_{DG}. An overlap capacitance model is presented in [15], but the step behavior in C_{GD} is not discussed. To bridge this gap, we present an improved gate overlap drift region capacitance model that accurately captures the capacitance behavior at high voltages under the BSIM-BULK framework.

II. Analysis of the Existing Model

The gate-drain capacitance contribution due to the drift region is determined by the gate overlap drift length (L_{ov}), which undergoes accumulation, depletion, or inversion depending on the applied gate and drain voltage. The overlap charge due to drift region is given by (1) [6], [9]. In BSIM-BULK, L_{ov} is defined as a model parameter $LOVER$, C_{ox} is the oxide capacitance, and V_t is the thermal voltage. q_{drift} is the inversion and accumulation charge below the gate overlap of the drift region that is determined, as in the core BSIM-BULK model, by analytically solving $\Psi_{p,drift}$ from (2). $\Psi_{p,drift}$ is the normalized pinch off potential. $V_{fb,drift}$ is the flatband voltage of the drift region, and VFBOV is a model parameter to tune $V_{fb,drift}$.

$$Q_{GDOV} = W \cdot LOVER \cdot C_{ox} \cdot V_t \cdot q_{drift} \tag{1}$$

$$V_{fb,\,drift} = \Psi_{p,drift} - \gamma \cdot \sqrt{e^{-\Psi_{p,drift}} - 1 + \Psi_{p,drift}} \tag{2}$$

$$V_{fb,\,drift} = \frac{V_{G,\,D} - VFBOV}{V_t} \tag{3}$$

$$\gamma = \frac{2 \cdot q \cdot \epsilon \cdot NDR}{C_{ox} \cdot \sqrt{V_t}} \tag{4}$$

$$q_{drift,\,inv} = 2 \cdot n_q \cdot q_{inversion} \tag{5}$$

$$q_{drift,\,acc} = V_{fb,\,drift} - \Psi_{p,drift} - 2 \cdot n_q \cdot q_{inversion} \tag{6}$$

The inversion, depletion and accumulation charge is then given by (5) and (6). From the above equations, we conclude that the depletion charge in the drift region increases with V_D, the rate of change of Q_{GDOV} slows down, and C_{GD} gradually decreases with V_D. But, the existing model does not have the step decline in C_{GD} with V_D as observed in the measured data. We performed 2-D numerical device simulations using TCAD on the LDMOS FET structure, as shown in Fig. 2 (a), to understand the physics behind the abrupt change in C_{GD}. In Fig. 2 (b), a depletion region forms below the gate at the N-drift and P-substrate junction at moderate V_D. If the applied V_D is further increased, the drift region is depleted and extends beyond the gate overlap length, as shown in Fig. 2 (c). From TCAD analysis, we infer that the depletion charge moves beyond the gate overlap as V_D increases. This reduces the contribution of the accumulation region (under the overlap gate length ($LOVER$)) to the gate-drain capacitance. As a result, we see a sudden drop in C_{GD} with a steep slope as shown in Fig. 3.

III. Modeling of Step Capacitance Behavior

Fig. 4 schematically highlights the depletion region under the gate overlap length. When a moderate V_D is applied, the depletion region D_1 below the gate overlap extends up to X_{n1}. Further increase in V_D extends the depletion region D_2 beyond gate overlap length upto X_{n2}. The depletion width $W_{dep,dr}$ can be expressed as (7), where N_{Dr}, N_{sub} are the drift and substrate region doping concentration, respectively. $V_{bi,dr}$ is the built-in voltage for the drift and substrate junction, ϵ_s is the silicon permittivity, and q is the electronic charge. With the doping concentration in the drift region being less than the substrate, the depletion width primarily extends in the drift region and moves beyond the gate overlap length ($LOVER$) with increasing V_D.

$$W_{dep,dr} = \sqrt{\frac{2 \cdot \varepsilon_s \cdot (V_D + V_{bi,dr})}{q} \cdot \left(\frac{1}{N_{Dr}} + \frac{1}{N_{sub}}\right)} \tag{7}$$

This reduces the effective contribution of the accumulation region ($LOVER$) to the gate-drain capacitance. We then model the modified overlap gate length as (8), correctly

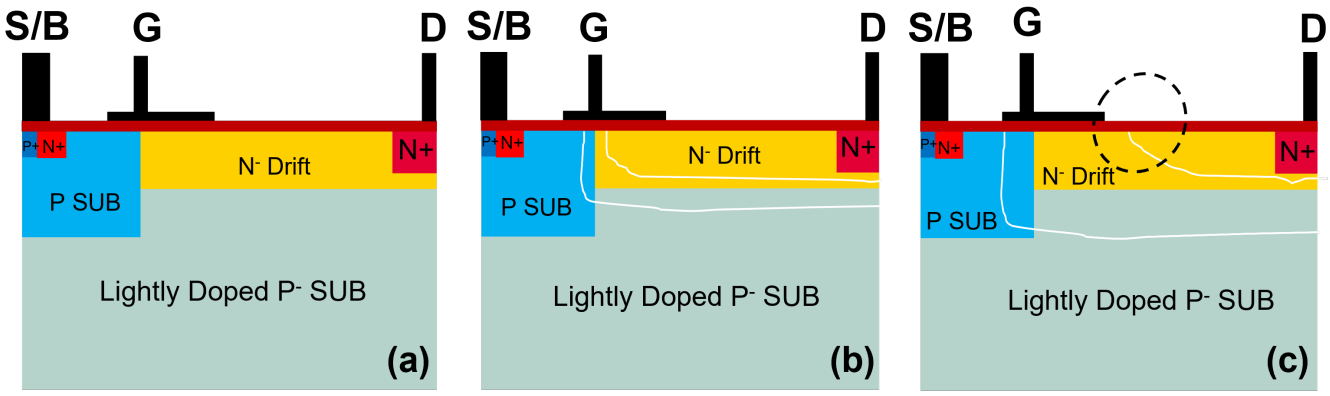

Fig. 2. Shows 2-D Numerical device simulation contour plots (a) LDMOS FET structure on which TCAD simulations are performed, (b) Moderate V_D is applied in OFF state, due to which depletion region is generated at the P substrate and N drift junction, (c) as higher V_D is applied, further depletion occurs in the lightly doped N drift region which goes beyond gate overlap length on the drift side.

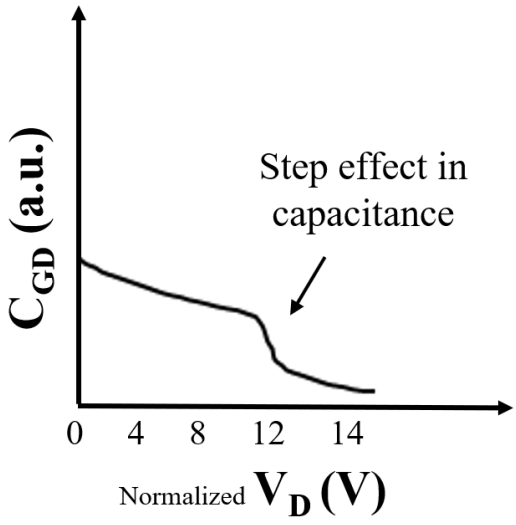

Fig. 3. Shows the step behavior observed during TCAD analysis in the C_{GD} vs. V_D at high V_D as soon as the depletion region goes beyond the gate overlap length.

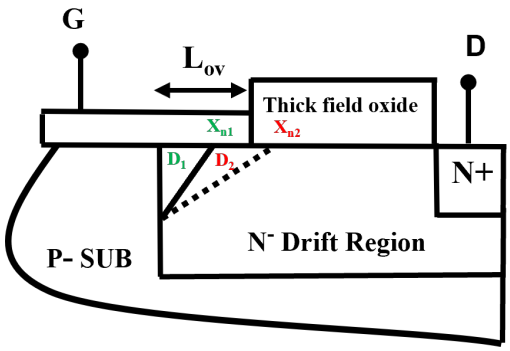

Fig. 4. Shows the schematic of depletion region extension in the drift region as the applied drain bias is increased.

explaining the charge contribution under the gate overlap length.

$$L_{\text{ov,new}} = LOVER - W_{\text{dep,dr}} \tag{8}$$

$$L_{\text{ov,new}} = LOVER \cdot (1 - LOVER1 \cdot \sqrt{V_{\text{D}} + V_{\text{bi,dr}}}) \tag{9}$$

The coefficient of the depletion width extension is defined by the model parameter $LOVER1$. After rearranging (8) and (9), the new gate overlap length, which is restricted to be a positive value, is given by (10). Parameter $LOVER2$ is introduced to make the model flexible enough to capture C_{GD} across varying LDMOS structures.

$$L_{\text{ov,new}} = LOVER \cdot (1 - (LOVER1 \cdot \sqrt{V_{\text{D}} + V_{\text{bi,dr}}} - LOVER2)) \tag{10}$$

The modified gate-to-drain overlap charge that accurately captures the capacitance is given as:

$$Q_{\text{GDOVnew}} = W \cdot L_{\text{ov,new}} \cdot C_{\text{ox}} \cdot V_{\text{t}} \cdot q_{\text{drift}} \tag{11}$$

The developed model accurately captures the measurement characteristics of two different width devices as shown in Fig. 5 and Fig. 6

Conclusions

We observed the step behavior in the capacitance of LDMOS transistors when operated at very high drain voltages. TCAD analysis is performed to study the underlying physics. We then presented a physics-based compact model under the BSIM-BULK framework, accurately capturing the measurement results.

Acknowledgment

We thank Infineon Technologies for providing us with the measured data. We also thank Science and Engineering Research Board (SERB), Department of Electrical Engineering and the Dean of Academic Affairs for supporting our work.

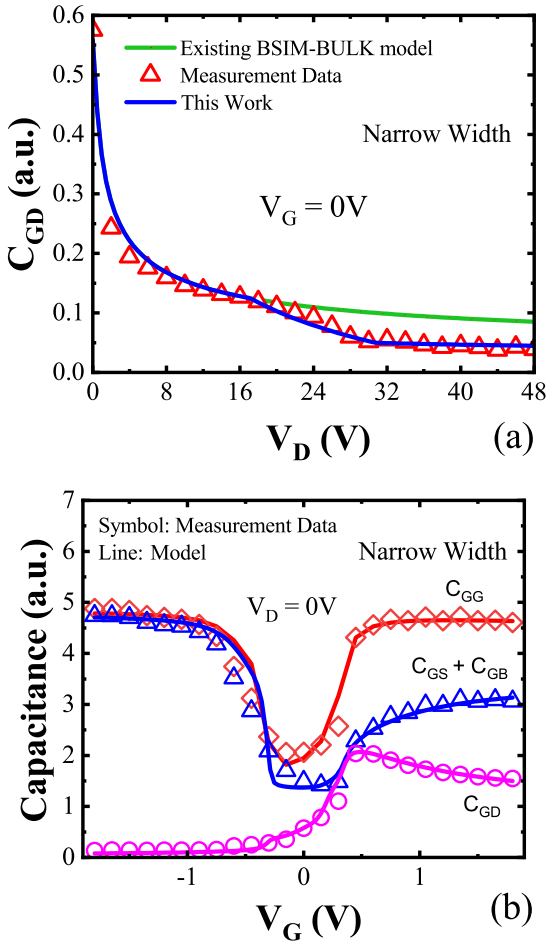

Fig. 5. Model validation with the measured data for narrow width device (a) shows C_{GD} vs normalized V_D in OFF state for both existing (green) and proposed model (blue) and, (b) shows all Capacitance vs V_G at V_D = 0V.

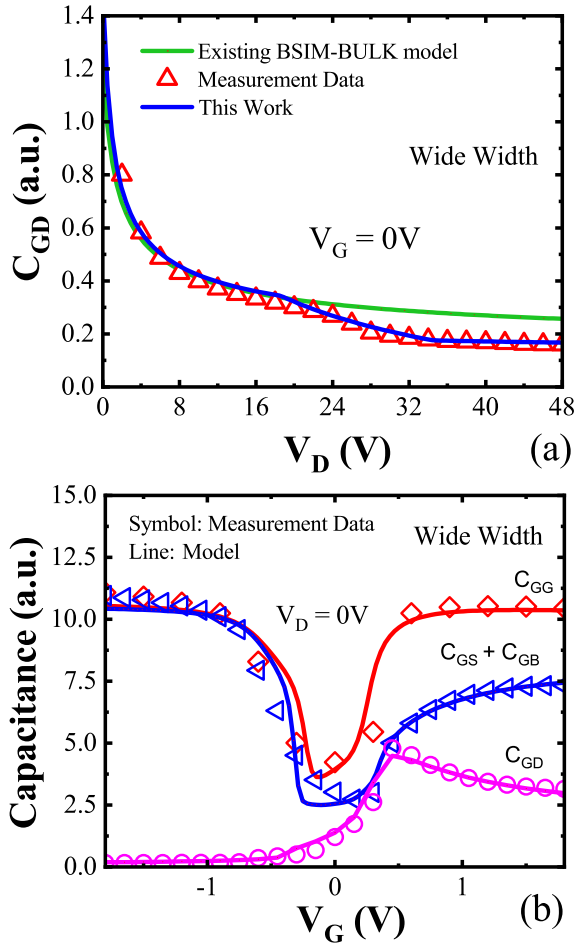

Fig. 6. Model validation with the measured data for wide width device (a) shows C_{GD} vs normalized V_D in OFF state for both existing (green) and proposed model (blue) and, (b) shows all Capacitance vs V_G at V_D = 0V.

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