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3D Electromagnetic simulation and modeling for DTCO of decoupling high-density capacitor in silicon interposer for HPC applications

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***Abstract*—In this paper, we present a Design-Technology Co-Optimization (DTCO) methodology of a heterogeneous 2.5D system that aims at integrating a passive interposer with HPC chiplets. The interposer comprises 3D high-density decoupling capacitors with the power delivery network (PDN) of the HPC chiplets. The proposed methodology is based on the discretization of the interposer into unit-cells and uses spatially distributed SPICE modeling to achieve voltage drop optimization, thus improving the performance of the chiplets at system level, in iterative loop processes. Using Electromagnetic (EM) simulation for unit-cells, incorporating boundary conditions that can be customized, we found out that neighboring cells play a significant role in the voltage drop seen inside the unit-cell as a result of resistive and inductive distributed parasitic interconnects. Consequently, these adjacent cells were incorporated into the EM simulation set-up for accurate power integrity analysis at system level.**

***Index Terms*—Power Delivery Network (PDN), Electromagnetic (EM) simulations, BEOL (Back-end-of-Line), Parasitic interconnects, High-density integrated capacitor, Chiplet, Design-Technology Co-Optimization (DTCO)**

I. Introduction

Using decoupling capacitors in a close proximity of chiplets system to reduce dynamic voltage drop and hence improve system performance is well known [1], [2]. However, addressing simultaneously integration of 3D heterogeneous systems with 3D high-density capacitor and interconnects is challenging and requires dedicated co-simulation methodologies between interposer and chiplets. These co-optimization techniques aim to provide accurate results within a shorter timeframe during the early stages of the device design and assembly choices.

Usually, PDN routing is simulated using a fixed full 3D electromagnetic (EM) description [3], [4], a classical lumped modeling [5] or even a complex distributed SPICE modeling [6]. Here, the methodology framework aims at providing relevant trade-off between complexity and accuracy, thanks to appropriate combination of simulation tools and to the development of generic spatially distributed unit-cells that are modeled using SPICE. Each unit-cell comprises realistic interposer BEOL (Back-end-of-Line) and 3D capacitor.

In the first part, the DTCO simulation and modeling framework of the 'heterogeneous 3D capacitance, PDN and chiplets system' is described. The second part focuses on the simulation results, from both the 3D electromagnetic interconnects simulation platform[1], ending up with a "low order spatially distributed SPICE modeling", and the system-level simulation platform.

II. DTCO simulation methodology

In this work, we propose a DTCO co-simulation methodology consisting in three phases (Fig. 1), considering unit-cells

[1]For confidentiality reasons, 3D EM simulation results data are presented with arbitrary units (a.u.)

EM simulation to set up the interposer SPICE netlist including parasitic. For 3D EM simulation, we use ANSYS Q3D, which

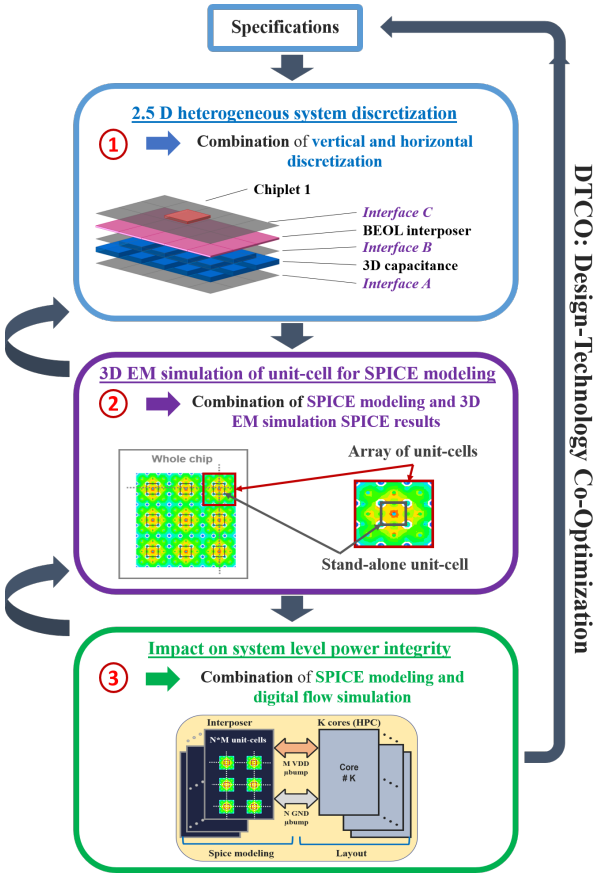

Fig. 1. DTCO simulation and modeling framework for a pre-study of a 3D passive silicon interposer embedded decoupling 3D high-density integrated capacitor; 1: From DTCO specifications to 2.5D system discretization, 2: 3D EM simulation and SPICE modeling, 3: 3D high-density capacitor and 3D parasitic impact on system performances

is a 3D EM solver for parasitic extraction and to perform voltage drop analysis, we use ANSYS Redhawk linking the distributed SPICE model to the digital flow [7].

A. Phase 1: 2.5 D heterogeneous system discretization

The first phase refers to the 2.5 D heterogeneous system discretization, illustrated in Fig. 2 and Fig. 3, which is performed on the layout and stack data of the silicon interposer with the embedded 3D capacitor, the PDN 3D routing and the 3D interconnects. Vertical and horizontal discretization consist respectively in selecting the main interfaces of the heterogeneous stacked system (interfaces 'A' and 'B' corresponding to top and bottom capacitance electrodes and interface 'C' located between the BEOL interposer and the chiplets) and in dividing the whole area in repeatable 'unit-cell', as illustrated in Fig. 3.

B. Phase 2: EM simulation of unit-cells for SPICE modeling

The goal of this phase is to perform accurate 3D EM simulation of the unit-cell PDN interposer routing with realistic

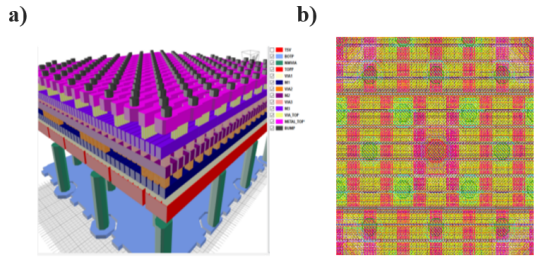

Fig. 2. Q3D simulation framework of a 3D high-density decoupling capacitor to chip interconnect network unit-cell: 3D view (a), 2D layout view (b), proposed horizontal and vertical discretization consisting of a stack of 3D entities and 2D interfaces divided into arrays of unit-cells

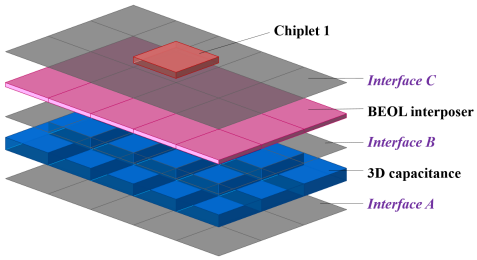

Fig. 3. Proposed horizontal and vertical discretization consisting of a stack of 3D entities and 2D interfaces divided into arrays of unit-cells

stack and layout data described in Fig. 2.a,b. The choice of Q3D ANSYS tool for 3D EM simulation (which is a "quasi-static" solver [5]–[7]) is driven by some simplifications:

1) Simulation of individual "unit-cells" (discretization described in phase 1)
2) Reduction of frequency bandwidth ([10 MHz-1 GHz])
3) Customization of boundary conditions
4) Quasi-equipotential excitations assumption

Quasi-equipotential excitation assumption is related to both limited sizing (boundary conditions) and low-frequency bandwidth [8]. ANSYS Q3D simulation set-ups are shown in Fig. 4, indicating the unit-cell with its interposer interconnect networks in-between interfaces 'A', 'B' and 'C' defined in Fig. 3, as well as the boundary conditions represented by the adjacent unit-cells. As shown in Fig. 4, by using for the ANSYS Q3D fields excitations set-up either 'CB' or 'CBA', we can discriminate spatially the various routing interconnect parasitics, ending up with the SPICE modeling described in Fig. 4. For example, to get the SPICE modeling of the 3D interconnects linking the top to the bottom capacitance electrodes (between 'A' and 'B' interfaces) in its 3D EM environment, we can do a subtraction of the simulation results using the two set-ups. For the 3D high density capacitor, we consider its equivalent SPICE modeling usually obtained using RF characterization [9].

C. Phase 3: Impact on system-level power integrity

The key figure-of-merit addressed in this phase is the dynamic voltage drop. We simulate at the chiplets level to

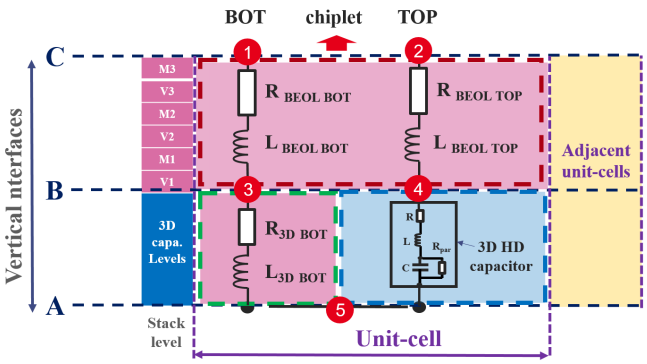

Fig. 4. Q3D simulation framework of a 3D high-density decoupling capacitor to chip interconnect network unit-cell based on proposed horizontal and vertical discretization in Fig 3: Simulation set-ups 'CB' (1, 2, 3, 4 connection) and 'CBA' (1, 2, 4, 5 connection)

quantify the balance between the positive impact of adding in the passive interposer 3D high-density integrated decoupling capacitor and the negative impact of adding the capacitor related parasitics on voltage drop. The PDN is simulated with ANSYS Redhawk as depicted in Fig. 5, where the N by M capacitor unit-cells are connected to the chiplet micro-bumps through BEOL routing by name mapping.

D. Toward an iterative process flow optimization

The methodology proposed is based on 3D EM simulation results using a transversal optimization approach, from the process to the system. As illustrated in Fig. 1, the framework is an iterative process to adapt in parallel accuracy and complexity trade-off of the simulations, as well as design, process, stack and material choices based on modeling and simulation results. The idea is to keep interconnect parasitic parameters available all along the system analysis in order to find obvious ways to optimize the dynamic voltage drop.

III. Co-simulation results

We apply here our DTCO simulation and modeling framework and discuss the significant results related to phase 2 and 3.

A. 3D EM simulation results

Q3D simulation results of the two routing network paths 'CB' and 'CBA' indicated in Fig. 4 are shown in Fig. 6, where resistance and inductance parasitics are extracted for a unit-cell with and without its adjacent cells. Results in Fig. 6 highlight the significant reduction of parasitics when considering the adjacent unit-cells (unit-cell embedded in a N by N unit-cells array). Another relevant result is the identification of the main parasitic contribution in Fig. 4, which is the 3D interconnect itself, in serie with the BEOL connected to the bottom electrode, and located between interfaces A and B. Moreover, we can observe in Fig. 6 that the R, L parameters are quasi-constant in the frequency range of interest. So no low frequency effects neither high frequency effects are impacting significantly our devices. Current repartition shown in Fig. 7 confirms the propagation outside the unit-cell and is used to validate customized boundary conditions.

B. System level simulation results

Table I summarizes three scenarios of interposer taking into account the whole PDN from VRM up to the chiplets (Fig. 5) in order to assess quantitatively the interconnect parasitics impact. For the interposer part, we consider the SPICE netlist including parasitics, as shown in Fig.4, with various boundary conditions and non-frequency dependent passive elements. Comparing the simulation results of scenarios 1 and 2, we can

TABLE I
Simulation results of PDN power integrity using various scenarios

Scenarios[a] using 3D high-density decoupling capacitor modeling including interconnect networks	**Area percentage of chiplet with more than $50\,mV$ voltage drop (%)**
1/ Stand-alone unit-cell	60.8
2/ Unit-cell in a 3*3 array (REF. case)	30.2
3/ REF. case when halving interco. parasitics	24.8

[a]**Scenarios 1 and 2 indicated in Fig. 6.**

see that adjacent cells reduce significantly the dynamic voltage drop. This is in accordance with the 3D EM results presented in Fig. 6. Therefore, adjacent cells must be taken into account because they have a major positive impact on PDN power integrity results: a factor of two for the key figure-of-merit presented in table I. In order to investigate optimization of interconnects, scenario 3 uses a 'virtual' test case based on a unit-cell in a 3 by 3 array, where the interconnect parasitics[2] would be halved. This last scenario allows a decrease of the key figure-of-merit of 5.4% (table I), highlighting that interposer routing could be optimized.

IV. Conclusion

Power integrity analysis of a PDN for chiplets including 3D high-density integrated decoupling capacitor in a passive silicon interposer solution is performed using a dedicated DTCO simulation methodology. As depicted in Tab. I, we face different solutions to optimize the performance at system-level assessing the impact of localized interconnect parasitics. Thus, the present methodology proposes an intermediate solution for the interposer modeling, between a full 3D electromagnetic description [3], [4] and a classical lumped modeling [5], relying on simplified assumptions. Indeed, it considers unit-cells EM simulation modeling taking into account customized boundary conditions in accordance to system accuracy analyses and requirements.

The main outputs of this paper are:

1) Methodology to address complex 3D heterogeneous system, going from the device up to the system, based on customized 3D EM simulation boundary conditions

[2]indicated in Fig. 4 between interfaces 'A' and 'C'

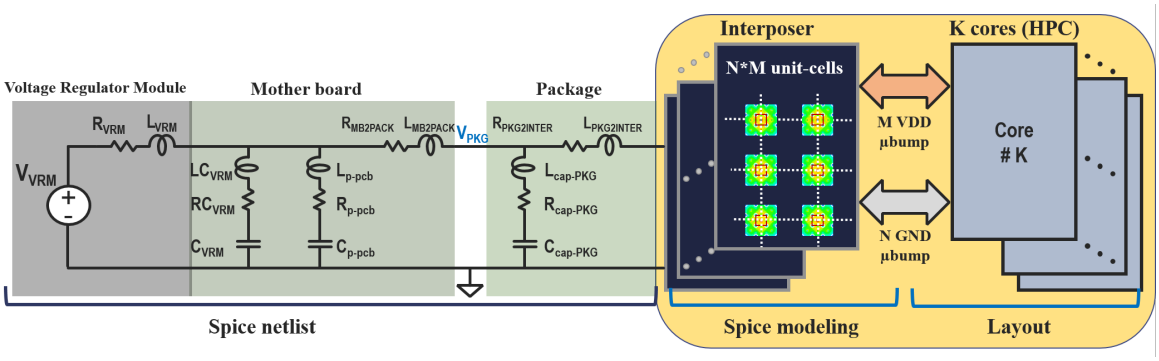

Fig. 5. System level Power Delivery Network

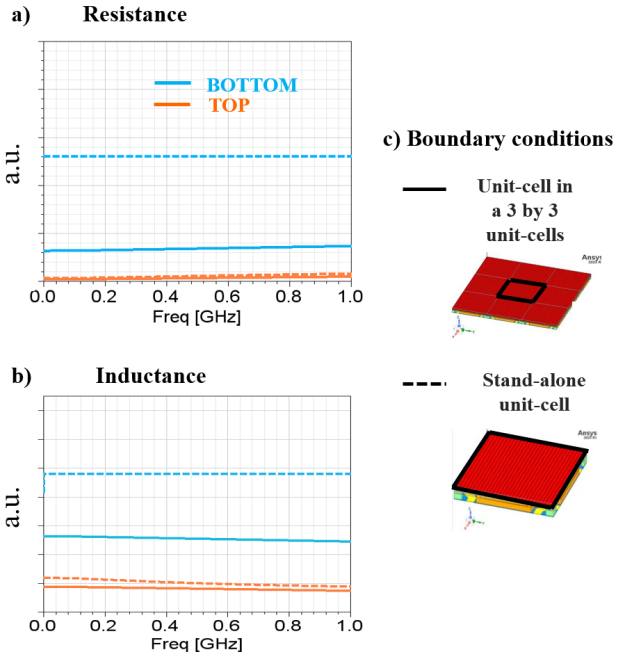

Fig. 6. Q3D parasitic extractions of 3D high-density integrated capacitor to chip interconnect network for a stand-alone capacitor unit-cell and for a unit-cell in a 3 by 3 unit-cells array in the [100 MHz-1 GHz] frequency bandwidth with specific unit-cell Boundary Conditions: Resistance (a), Inductance (b)

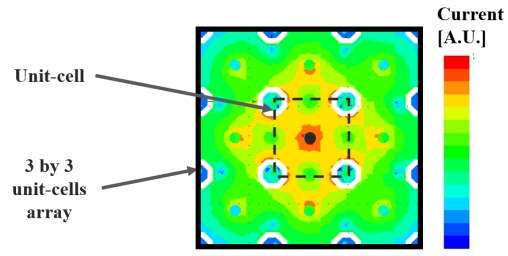

Fig. 7. Current distribution from Q3D simulation results of 3D high-density integrated capacitor to chip interconnect network for a stand-alone capacitor unit-cell and for a unit-cell in a 3 by 3 unit-cells array (Fig. 5) at frequency of 10 MHz

2) An iterative methodology suitable for the early stages of the design process, based on choices and trade-off between complexity and accuracy
3) Various 3D EM simulation platform set-ups to extract spatially distributed parasitics
4) An overall DTCO approach that can be used for design, process and material optimization

Based on the simulation results, in order to optimize the PDN power integrity, we can either reduce 3D interconnect itself, which can be done for example by increasing its area or reduce the inter-cell network parasitics. The last strategy allows providing a better current flow on a larger area as it increases parallelization and can be addressed by modifications in the process, stack and/or design choices.

REFERENCES

[1] M. M. Jatlaoui et al., "Multi-terminal Ultra-thin 3D Nanoporous Silicon Capacitor Technology for High-Speed Circuits Decoupling," in 2022 IEEE 72nd Electronic Components and Technology Conference (ECTC), May 2022, pp. 908–913.

[2] J. Kim et al., "Chiplet/Interposer Co-Design for Power Delivery Network Optimization in Heterogeneous 2.5-D ICs," IEEE Transactions on Components, Packaging and Manufacturing Technology, vol. 11, no. 12, pp. 2148–2157, Dec. 2021.

[3] S. Hou et al., "Integrated Deep Trench Capacitor in Si Interposer for CoWoS Heterogeneous Integration," in 2019 IEEE International Electron Devices Meeting (IEDM), Dec. 2019, pp. 19.5.1–19.5.4.

[4] L. Smith, R. Anderson, D. Forehand, T. Pelc, and T. Roy, "Power distribution system design methodology and capacitor selection for modern CMOS technology," IEEE Transactions on Advanced Packaging, vol. 22, no. 3, pp. 284–291, Aug. 1999.

[5] Z. Xu et al., "Modeling of power delivery into 3D chips on silicon interposer," in 2012 IEEE 62nd Electronic Components and Technology Conference, May 2012, pp. 683–689.

[6] Z. Xu, J.-Q. Lu, B. C. Webb, and J. U. Knickerbocker, "Electromagnetic-SPICE modeling and analysis of 3D power network," in 2011 IEEE 61st Electronic Components and Technology Conference (ECTC), May 2011, pp. 2171–2178.

[7] ANSYS Q3D extractor, 2023 R1, ANSYS REDHAWK, 2023.

[8] K. Dieng et al., "Electrical Model of Different Architectures of through Silicon Capacitors for High Frequency Power Distribution Network (PDN) Decoupling Operations," in 2016 IEEE 66th Electronic Components and Technology Conference (ECTC). Las Vegas, NV, USA: IEEE, May 2016, pp. 74–81.

[9] H. Jacquinot and D. Denis, "Characterization, modeling and optimization of 3D embedded trench decoupling capacitors in Si-RF interposer," in 2013 IEEE 63rd Electronic Components and Technology Conference, May 2013, pp. 1372–1378.