Simulation Challenges of SiC MOSFET Switching Performance and Reliability

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***Abstract*—This paper describes a holistic SiC MOSFET simulation flow with a focus on switching and reliability performance in the form of Short-Circuit validation. Several key physical aspects native to SiC MOSFETs are elucidated in TCAD simulations. A novel link between TCAD and SPICE is demonstrated. This link leads into a full SPICE model calibration simultaneously to typical power converter operating regions and Short-Circuit reliability.**

***Keywords*—Silicon-Carbide (SiC), power MOSFET, TCAD, SPICE, Short-Circuit**

I. INTRODUCTION

Silicon-Carbide (SiC) is now a prevalent technology in the power electronic space. The fast growing demand for electric vehicles (EV) is driving the market for high efficiency semiconductor power solutions. The electricity requirements of these EVs are also driving the demand for solar inverters and wind farms to generate electricity from renewable sources. The higher power density and faster switching native to these applications presents new design challenges for designers of SiC MOSFET power modules. Without complete simulation flows, costly fabrication and test-based design cycles are often needed.

There are many distinct challenges to simulating SiC MOSFETs from TCAD during technology development to SPICE in application simulation. The paper looks at several aspects native to SiC MOSFET modeling and simulation with a focus on the Short-Circuit test (SC). This test is a critical success criterion in 3-phase inverters for EV motor control to protect the battery and the components of the vehicle in case of loss of control of the converter. SC type I is common SC test simplification where the Device Under Test (DUT) is gated on into a faulty event with shorted load.

Methodologies are described that link device modeling and simulation between TCAD and SPICE in a cohesive flow. Section II details challenges in SiC MOSFET TCAD simulation. Sections III describes a technique to link TCAD to SPICE in a physical and automated manner. Section IV provides experimental results and validation of the SPICE models. Finally, section V states the conclusions and future work.

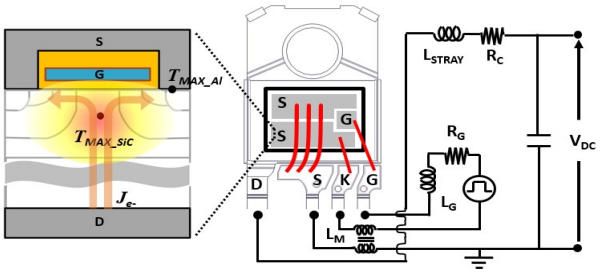


Fig. 1. Schematic description of the mixed-mode simulation for SC test in SiC MOSFETs. Schematic cross section indicates current flow and maximum temperature locations in SiC and Al regions (T_{MAX_SiC} ,T_{MAX_Al})

II. NEW ELECTRO-THERMAL SIC MOSFET TCAD PHYSICS MODELS

For those TCAD users transitioning from Silicon to SiC power MOSFETs, most of the novelty encountered in physics models is directly or indirectly related to the one of the following aspects:

- traps and trapped charges at or near the SiC/Oxide interface
- non-ionized impurities and crystal defects acting as traps and recombination centers in the bulk
- anisotropy for electrical and thermal characteristics

Besides these three phenomena, all the rest of parameters in the electrical and thermal physical models are normally adapted from Silicon to 4H-SiC, which is a wide-bandgap material featuring high critical electric field, saturation velocity, and thermal conductivity.

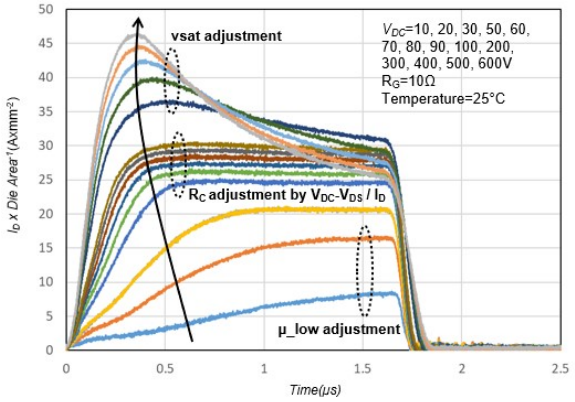


Fig. 2. Set of measured I_D-V_{DS} waveforms from SC test in a wide range of V_{DC}. Different V_{DC} levels allow different adjustments in TCAD models and circuit parasitics

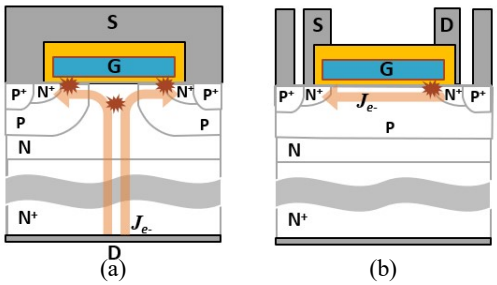


Fig. 3. Schematic description of cross section in (a) vertical SiC MOSFET and (b) lateral SiC MOSFET test structure indicating current flow and current saturation locations

Regarding the channel mobility at low electric field (μ_low), some contributions like the Coulomb scattering, are related to the existence of charge at the SiC/Oxide interface [1]. To properly calibrate the density of traps at SiC/Oxide interface, DC transfer characteristics are used. Differently, the trap parameters related to capture/emission require the support from dynamic testing. An accurate dynamic model for traps is fundamental to capture effects like BTI and Vth hysteresis [2].

As per the non-ionized impurities, the incomplete ionization model for dopants is of utmost importance to capture switching losses in TCAD simulations [3]. Also related to implanted dopants, the implanted regions may imply a certain level of damage in the crystal, thus generating recombination centers for free carriers. This requires an additional complexity in defining carrier lifetime models in different regions of the SiC bulk [4]. In combination of the mobility models, an accurate lifetime prediction is crucial to replicate the third quadrant conduction and reverse recovery.

Finally, the orientation effect for the hexagonal crystal structure of 4H-SiC should be accounted for in the TCAD simulations. In this sense, the anisotropic carrier heating and drift velocity lead to the anisotropy of impact ionization and breakdown voltage. Similarly, the anisotropy in phonon thermal transport, thermal resistivity, and specific heat needs special attention in scenarios with self-heating [4].

As a matter of example, the Short-Circuit test (SC) is one of the most challenging switching events to be simulated [5]. It entangles practically all the previous physical models and additional ones related to non-permanent high gate current [6]. In fact, the extreme local temperatures (T_J=T_{MAX_SiC}>1300K) enhance the thermionic effect in such a way that tunneling models, recommended for very thin oxides (<3nm), are suitable to predict gate current in SiC MOSFETs with thick oxide (>40nm). Moreover, SC simulation also needs the use of the so called mixed-mode combining TCAD and SPICE elements. The latter accounts for the external circuit that provides electrical excitation as well as for all the parasitic elements from device package, PCB boards and passive components [5].

A schematic description of our mixed-mode simulations is represented in Fig. 1 without explicitly displaying the package parasitics. The parasitic elements in the gate and power loops can be extracted from other finite-element simulations or by simple analysis of measured waveforms. In the second option, a set of V_{DS} and I_D waveforms from onsemi's advanced EliteSiC MOSFET technology for a wide V_{DC} range is convenient as seen in Fig. 2. For V_{DC}<30V, curves assist in the calibration of μ_low related models, being more efficient in reducing self-heating effect than curve tracer pulses (>100μs). For 40V< V_{DC}< 100V, curves are ideal to calculate the power loop series resistance R_C. For V_{DC}>100V, the self-heating effect and current saturation are dominant effects. At any V_{DC} range, the power loop stray inductance (L_{STRAY}) can be easily extracted by $\Delta V_{DS} = L_{STRAY} \bullet dI_D/dt$.

As a part of the calibration methodology, dedicated test structures are also desired. Hence, lateral SiC MOSFETs depicted in Fig. 3 help to disentangle the role of the channel and JFET regions in the current saturation with separated calibration of the carrier velocity saturation models. By using the Canali model for current saturation with high field mobility [7], the velocity saturation can be adjusted to match I_D peak in SC as shown in Fig. 4.

III. TCAD TO SPICE LINK

It is well known that TCAD, especially mixed-mode, has long simulations time that can be prohibitive for large scale application circuits with power modules. On the other hand, SPICE provides much faster simulation time however at the expense of physical accuracy. Recently, advance physically based models for SiC MOSFETs have been developed that retain reasonable physics of the technology including process parameters [8], [9]. Such models provide a link back to the full physical accuracy of TCAD through a custom developed flow in Sentaurus Work Bench presented here called SPICE Assist as shown in Fig. 5 [10].

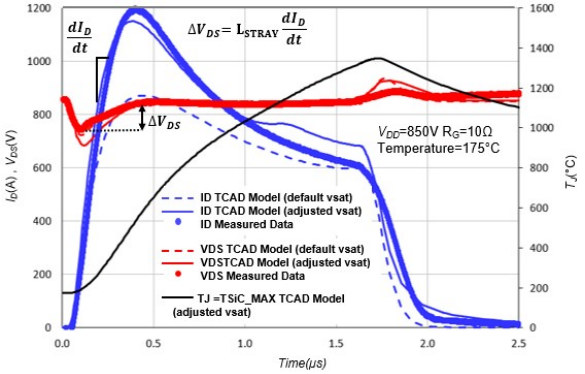


Fig. 4. Measured vs. TCAD I_D-V_{DS} waveforms from SC test at the more stringent conditions

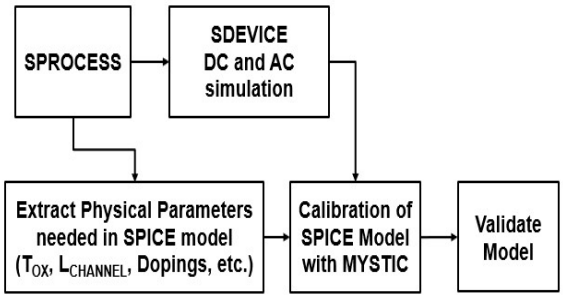


Fig. 5. SPICE Assist flow within Sentaurus workbench

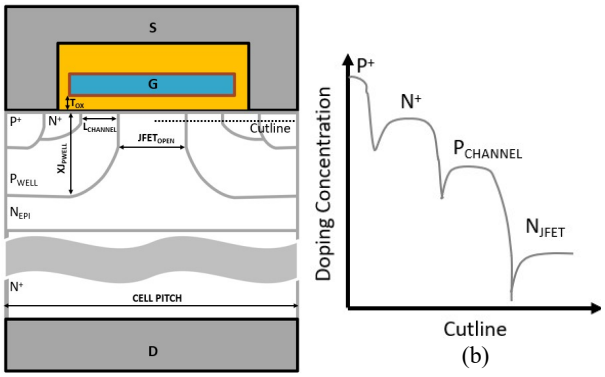
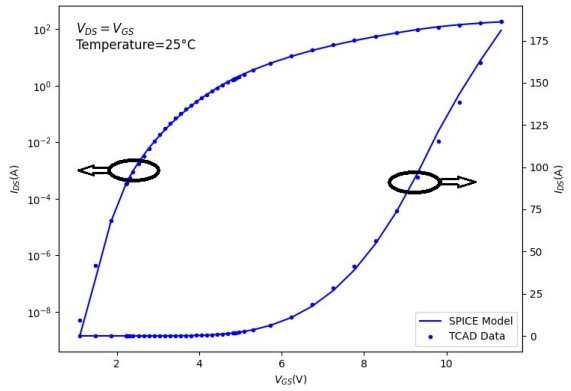


Fig. 6. SiC MOSFET process parameters used in SPICE Assist flow shown in (a) cross section and (b) doping profile

Following the SPROCESS step, the essential process parameters from the device structure are automatically extracted via a TCL script within the SPROCESS command file. The script facilitates the extraction of all necessary process parameters, such as T_{OX}, $L_{CHANNEL}$, $P_{CHANNEL}$, N_{JFET}, and others as shown in the cross section and doping profile in Fig. 6. These extracted process parameters are fed into an automated MYSTIC calibration step. The MYSTIC step calibrates the model to the data generated by SDEVCE. SVISUAL then provides model validation plots as shown in Fig. 7. SPICE Assist can be used to generate models practically instantaneously that track changes in the technology through SPROCESS. This is particular useful for application engineers to feed back application performance to technology developers early in the technology development phase.



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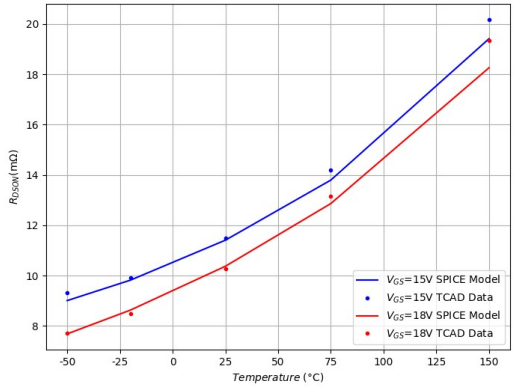

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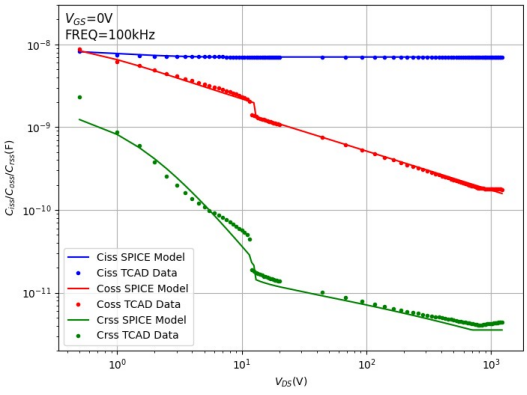
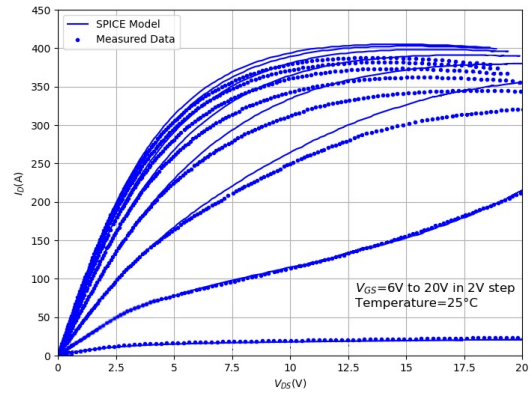


(c)

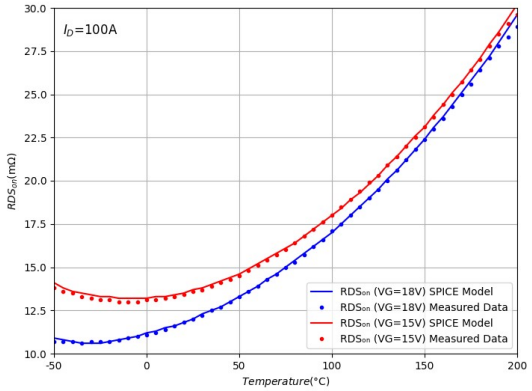
Fig. 7. SPICE Assist validation for (a) I_D-V_{GS}, (b) RDS_{on}, and (c) Capacitance-V_{DS}

IV. SPICE MEASUREMENT VALIDATION

The final step in the overall simulation flow is to build and validate SPICE models to measurements on the same EliteSiC MOSFET from section II. Starting with the SPICE Assist models, a full calibration to measured data including the Short-Circuit test described in section II is performed. Fig. 8 displays the typical model matching for I_D-V_{DS}, RDS_{on}, and capacitance. where the I_D-V_{DS} range is considered low power. Conventional power MOSFET model extraction focuses solely on this low power region since curve tracers are not able to measures I-V in high power regions typical of device operation in Short-Circuit. Model parameters including self-heating for the channel, JFET, and drift resistance are extracted to match the low power data. The problem



(a)



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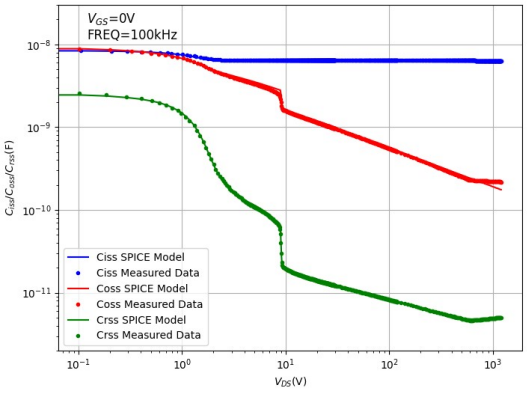

(c)

Fig. 8. Measurement validation of SPICE model for (a) I_D-V_{DS}, (b) RDS_{on}, and (c) Capacitance-V_{DS}

with this approach is, the modeling engineer has no information about the very high drain current due to the simultaneously high gate and drain voltages in SC. The low power model is used somewhat blindly to simulate SC performance. If there is a imbalance between self-heating parameters, channel velocity saturation and its temperature coefficient, and temperature coefficients of the JFET, the SC drain current will not match its measurement. With the inclusion of SC data from the start of the model extraction, the right balance for the interdependence of the model parameters on low and high power regions can be found. Fig. 9 displays the SPICE model match to the SC data before using SC data and after. It should be noted accurate capacitance modeling as shown in Fig. 8(c) is also required to capture the SC switching waveforms. The peak of the

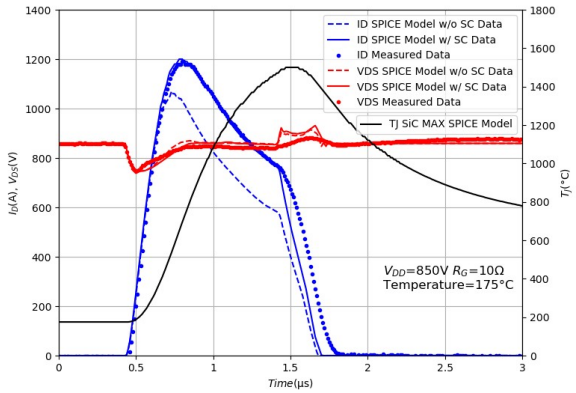

Fig. 9. Measured vs. SPICE I_D-V_{DS} waveforms from SC test

SC current is predominantly affected by the channel velocity saturation and self-heating parameters. Not surprisingly, this is similar to the TCAD findings in section II. The SPICE simulated T_J matches the TCAD results reasonably well. The accurate SPICE modeling of the SC I_D together with low power I_D including RDS_{on}, the capacitance, and the T_J enables accurate application and reliability simulation.

V. Conclusion

This paper presents a critical study of physical phenomena that affect the TCAD and SPICE simulation of onsemi's advanced SiC MOSFET technology with a focus on Short-Circuit reliability. The presented simulation flows demonstrate how TCAD, SPICE, and their linkage can be used to enable technology developers and application engineers to work together to produce advanced reliable state of the art SiC MOSFET technologies.

References

1. K. Lee et al., "Device simulation modeling of 1200 V SiC MOSFETs", Proceedings PCIM 2017, pp. 1-6, May 2017.
2. A. Sakai et al., "Impacts of the 4H-SiC/SiO2 interface states on the switching operation of power MOSFETs", Proceedings SISPAD 2015, pp. 64-67, September 2015
3. Z. Tong et al., "Origins of Soft-Switching Coss Losses in SiC Power MOSFETs and Diodes for Resonant Converter Applications", IEEE Journal of Emerging and Selected Topics in Power Electronics, 9, no. 4, pp. 4082-4095, April 2020
4. B. Kakarla, "Short Circuit Behavior of SiC MOSFETs," Ph.D dissertation, ETH Zurich, 2021
5. S. Kochoska et al., "Gate Current Peaks Due to Cgd Overcharge in SiC MOSFETs Under Short-Circuit Test", Proceedings of ISPSD 2023, pp. 246-249, May 2023
6. J. Roig et al., "On the TCAD Modeling of Non-Permanent Gate Current Increase During Short-Circuit Test in SiC MOSFETs", to be published in ICSCRM 2023
7. C. Canali et al., "Electron and Hole Drift Velocity Measurements in Silicon and Their Empirical Relation to Electric Field and Temperature", IEEE Transactions on Electron Devices, 22, no. 11, pp. 1045-1047, Nov 1975
8. C. He, et. al., "A Physically Based Scalable SPICE Model for Silicon Carbide Power MOSFETs", Proceedings of APEC 2017, pp. 2678-2684, March 2017
9. C. He, et. al, "SiC MOSFET Corner and Statistical SPICE Model Generation", Proceedings of ISPSD 2020, pp. 154-157, September 2020
10. Sentaurus TCAD Tools Suite. T-2022.03. Synopsys