Superconducting route to quantum computing

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***Abstract*—The basics of the hardware for superconducting quantum computing are described.**

***Index Terms*—quantum computing, superconducting qubit, circuit quantum electrodynamics, CMOS technology**

I. Introduction

Once thought nightmare [1], quantum computers are now being developed under various physical platforms of both natural (photons, ions, ultracold atoms, and Rydberg atoms) and artificial (semiconductor and superconducting devices) systems. Quantum bits (qubits) realized there by a variety of encoding schemes are not just 0 or 1 but can take a quantum mechanical superposition of 0 and 1 as well as an entangled state with multiple qubits. With each physical system having its pros and cons, we still do not know how quantum computers will look like twenty or thirty years later. But at this moment, one of the leading platforms is the system based on superconducting quantum circuits. The 53-qubit *Sycamore* processor from Google demonstrated quantum supremacy in the sampling of random quantum circuits, which the state-of-the-art classical counterpart would require 10,000 years to solve [2]. Even though the problem setting itself will not have practical applications and the claim is debatable [3], it has certainly intensified worldwide efforts to further unlock the potential of quantum computers, leading to more recent demonstrations using the large(er) number of superconducting qubits such as error suppression of a single logical qubit encoded using 49 physical qubits (including auxiliary qubits) [4], generation of a 51-qubit cluster state [5], and simulation of the magnetization of a spin system using 127 qubits and post-processing [6].

A salient feature of superconducting quantum circuits that has attracted quantum hardware developers is that one can engineer, or even create, the properties of qubits by a judicious design of the circuit parameters. Essentially, the individual hardware developers, whether in academic or in industry, have their own favorite superconducting qubits. It is not the intent of this talk to cover such a wide range of qubit architectures. Here, the author takes the system developed at RIKEN (national research institute in Japan) as a concrete example and describes how it works. It should be noted, however, that even in this example the qubit design, fabrication process, and control electronics have undergone continuous updates.

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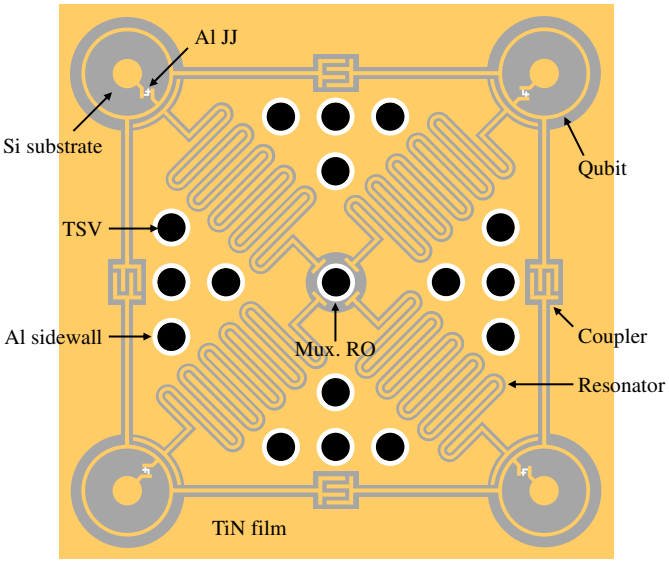

Fig. 1. Schematic layout of a quantum processor consisting of four qubits at the corners and a multiplexed readout (Mux. RO) structure at the center. JJ: Josephson junction. TSV: through-silicon via.

II. Hardware–chip, wiring, and electronics

Figure 1 shows a schematic layout of four superconducting qubits integrated with multiplexed readout. The circular-shaped qubits, or concentric transmons, are located at the four corners (a transmon is a type of superconducting qubit designed to be immune to the charge fluctuations). The neighboring qubits are coupled via the arms that run the side and meet at the middle to form an interdigit capacitor. The inner and outer circles of the qubit are shunted by the Josephson junction, two layers of superconductors interrupted by a thin insulating layer, which from the viewpoint of circuit design acts as a nonlinear and dissipationless inductor. The nonlinearity is an essential ingredient of a superconducting qubit. A linear LC circuit, when quantized, is a harmonic oscillator with the energy levels equally spaced by $\omega_{i,i+1} \equiv \omega_{i+1} - \omega_i = 1/\sqrt{\mathrm{LC}}$ (i = 0, 1, 2, ...). Such harmonic oscillator states are indeed formed in the readout resonators, the meander lines capacitively coupled to the qubits. The equally spaced levels mean that the drive frequency tuned to ω_{01} is likewise on resonance with other transitions $\omega_{i,i+1}$, precluding the distinction of the qubit subspace from higher levels. The cosine potential that the Josephson junction provides makes ω_{01} larger than the others, allowing us to define the ground

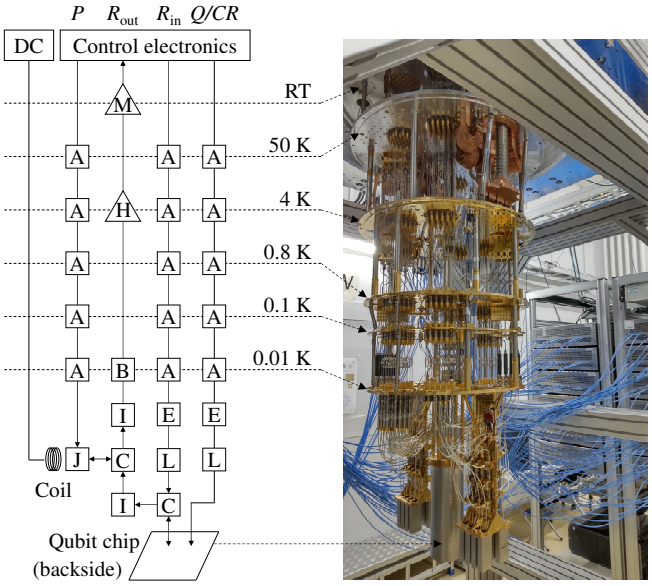

Fig. 2. (Left) Schematic of control and measurement chains from control electronics at room temperature (RT) to the qubit chip at 10 mK. *Q*: qubit control. *CR*: cross-resonance. $R_{\rm in}$: readout (input). $R_{\rm out}$: readout (output). *P*: pump for Josephson parametric amplifier (JPA, J). A: attenuator. E: eccosorb infrared filter. L: low-pass filter. C: circulator. I: isolator. B: band-pass filter. H: HEMT cryogenic amplifier. M: microwave amplifier. JPAs are flux-biased by passing currents to coils placed nearby. (Right) Photo of a dilution refrigerator and control electronics. A 64-qubit chip is installed inside of the magnetic shield (the silver cylinder at the bottom).

state as qubit $|0\rangle$ and the first excited state as qubit $|1\rangle$. The parameter α defined as $\omega_{12} - \omega_{01}$ characterizes the degree of nonlinearity of a qubit. In reality, the higher levels are still not negligible. The excitation to them, called leakage, is a significant source of quantum logic errors in superconducting quantum processors.

The abilities to perform single- and two-qubit gates and a readout of the qubit state are mandatory to any quantum processors. In the design of Fig. 1, all these are realized by applying microwave pulses. To this end, coaxial cables are in contact with the backside of the chip via pogo pins, aligned perpendicular to it; see the schematic of Fig. 2. Each qubit has its own control wiring right behind the inner circle, and the four readout resonators are joined together at the central port, to which the readout microwave pulses are applied. A single-qubit gate is a properly timed microwave pulse on resonance with the given qubit, driving the qubit onto anywhere in the Bloch sphere, or an arbitrary superposition of $|0\rangle$ and $|1\rangle$ including the relative phase.

The readout scheme is based on the concept of circuit quantum electrodynamics [7]. The readout resonator is detuned from the qubit and couples to it dispersively such that the resonance frequency is dependent on the qubit state. The signal reflected from the resonator then carries the information of the qubit state in its frequency and phase. This dispersive readout is one realization of quantum nondemolition measurements required for quantum error correction. But the Purcell effect can still induce the qubit dephasing, and on-chip filters (Purcell filters) are often used concomitantly [8].

There are various ways to perform two-qubit gates. The cross-resonance (CR) gate [9] adopted in the present design is advantageous in avoiding the introduction of additional RF or DC wiring to the chip. The same wiring that is used for the single-qubit gate can be used. When the neighboring two qubits, say Q1 and Q2, have different frequencies ω_{q1} and ω_{q2}, applying ω_{q2} on Q1 does nothing (ideally) to Q1. ω_{q2} can drive Q2 via the coupler, but the way it does is dependent on the state of Q1. One can thus realize a conditional gate between two nearest-neighbor qubits.

The qubit layout in Fig. 1 constitutes a unit cell extendible to a larger lattice of qubits by simply repeating it two-dimensionally. The side length of the unit cell is about a quarter of a centimeter and that the wiring comes out of plane. Therefore, there is enough room for introducing a coaxial cable even to a qubit in the middle of a large lattice. In-plane wiring if used would have to employ air-bridges overarching multiple microwave lines, possibly increasing the crosstalk among them.

The qubit chip consists of multiple layers of materials. The substrate is a high-resistivity silicon (Si) wafer with the thickness of 300 μm. Titanium nitride (TiN) films, which are superconductors resistant to oxidation and have large kinetic inductance [10], are deposited with the thickness of 100 nm on both sides of the wafer. Through-silicon vias (TSVs) are formed by the Bosch process and the sidewalls are covered with aluminum (Al). Al-covered TSVs electrically connect the front and back sides of the chip, effective in suppressing spurious electromagnetic modes such as the chip mode (the rectangular cavity mode arising from the size of the chip) and the slotline mode (the mode between unconnected ground planes) which otherwise can damage the qubit coherence. Josephson junctions made of Al and AlO_x have 200 nm $\times$ 200 nm in area. The RIKEN team now routinely fabricates chips containing 64 qubits of an 8 $\times$ 8 lattice.

The fabricated circuits do not have any functionalities to tune the qubit frequencies *in situ*, whereas to perform accurate (high-fidelity) CR gates the qubit frequencies must be properly assigned within the lattice (in an extreme case, if nearest-neighbor qubits share the same frequencies the CR pulse will drive the both qubits). However, the inevitable process inhomogeneity calls for methods to adjust the qubit frequencies after fabrication. One promising approach is laser annealing [11]–[13]. Illumination of laser focused onto a junction area increases its resistance, enabling independent trimming of the qubit frequencies.

The chip is mounted inside of a dilution refrigerator and is cooled down to 10 mK. While the superconducting transition temperature $T_{\rm c}$ of bulk Al is 1.14 K, the chip must be at temperatures well below $T_{\rm c}$. The qubit frequencies typically fall on the 2-to-10 GHz range, chosen largely in light of the availability of high-frequency electronics. For instance, in one of our designs, the qubit (resonator) frequencies are set between 7.7–8.9 (10.1–10.4) GHz, with α = $-$400 MHz (negative due to the softening potential). 10 GHz corresponds

to 0.48 K in temperature, and the thermal excitation to the higher levels must be suppressed. The suppression is not sufficient just by cooling the chip, because the signals come from room temperature (RT). The incoming signals are progressively attenuated and thermalized at multiple temperature stages (A in Fig. 2). For instance, a typical microwave power for readout is at the single photon level of -130 dBm. The noises outside of the operational frequency range are rejected by low-pass (L) and band-pass (B) filters. The eccosorb filters (E), which absorb photons in the infrared regime, are also employed. Such photons exist as stray light or black body radiation from the higher temperature stages and, with energies larger than $2\Delta \approx 2 \times 1.76 k_{\rm B} T_{\rm c}$, can break Cooper pairs. The broken Cooper pairs, or quasiparticles, wandering about inside a superconductor are harmful, as they exchange energies with qubits or cause parity switching by tunneling across the junction barrier [14].

The readout microwave pulse ($R_{\rm in}$) reflected at the chip is sent back to the electronics ($R_{\rm out}$) directed by circulators (C). Not to mention, the single-photon-level signal would die out without amplification. Quantum-limited amplifiers are desired as the first-stage amplification. Impedance-matched parametric amplifiers (IMPAs) [15], a type of Josephson parametric amplifiers (JPAs), are installed in the photo of Fig. 2 (inside of the rectangular, silver magnetic shields at the bottom). They are pumped parametrically at twice the readout frequencies (*P*). Other types of JPAs, such as Josephson traveling wave parametric amplifier (JTWPA), can also be used, and some are commercialized [16]. Additional amplifications are carried out at the 4-K stage by a high electron mobility transistor (HEMT, H) cryogenic amplifier followed by a low-noise microwave amplifier (M) at RT.

To estimate the number of coaxial cables needed to fully operate an N-qubit device, we count N for *Q/CR*, $N/4$ for $R_{\rm in}$, $R_{\rm out}$, and *P*, thus $1.75 \times N$ in total. For the 64-qubit setup in Fig. 2, this amounts to 112 coaxial cables, connected all the way from FPGA-based digital control electronics at RT to the 10-mK stage.

III. Remarks

Here, a few remarks that may be of interest to those in the semiconductor industry are made.

From manufacturing standard, the superconducting quantum circuits described above are fairly large. Why? One reason is that the $\lambda/2$ coplanar waveguide resonators have dimensions largely dictated by the wavelength and the materials dielectric constant. Furthermore, to design a transmon, a small charging energy, or equivalently a large total capacitance, is required. In Fig. 1, the outer diameter of the concentric transmon is about 600 μm. The use of an interdigit capacitor for instance should decrease the size of a transmon compared with a parallel planar capacitor. This is certainly true and in some part has been employed, but shrinking the size this way turns out to affect the coherence. This was not so obvious in early studies, but the community now understands that defects omnipresent at the metal–air and metal–substrate interfaces, or inside of the junction that is typically amorphous, can act as microscopic two-level systems and absorb single-photon microwaves. This leads to the energy (dielectric) loss in the circuit, i.e., the relaxation of a qubit (T_1). A miniaturized device concentrates the microwave intensity in a small region and is prone to the energy loss. Making a device larger dilutes the distribution of microwave across the device and extends T_1 [17]. For this reason, over the years, transmons have become bigger and bigger. This, however, is not the end of the story. Recent studies have uncovered that when the dimension of a transmon matches with the wavelength of above-100-GHz photons, the transmon itself acts as a dipole antenna to absorb the resonant photons [14], [18]. This is somewhat similar to the chip mode mentioned earlier, but this time the relevant photons have the energies larger than 2Δ and generate quasiparticles.

In the face of such a size effect, it is worthwhile to revert to shrinking the size of transmons again, while of course preserving the coherence. Not to mention, a smaller footprint is advantageous for further integration of qubits. In a merged-element transmon (MET), the Josephson junction is designed to serve as both a nonlinear inductor and a parallel shunt capacitor [19], [20]. This requires a micron-sized junction, but the overall footprint can be reduced. While the large junction indicates more defects in the amorphous barrier layer, but they can be traded by a reduced participation of the metal–air and metal–substrate interfaces. The coherence times comparable to standard transmons have been reported [20]. A FinMET is another emerging idea that combines the concepts of MET and FinFET, and complements the need of reducing defects in a large junction of MET [21]. An anisotropic etch of the Si substrate creates a thin wall of Si (fin). By depositing Al films on both sides, the Al/Si/Ai structure works as a tunnel barrier with reduced dielectric loss of crystalline Si. It is further hoped that this approach will be compatible with the industry-scale CMOS process.

In semiconductor qubits, it is a logical step toward large-scale quantum processors to leverage the state-of-the-art CMOS fabrication facilities, as the fabrication processes are quite similar [22]. However, the fabrication of transmons is not necessarily compatible with the CMOS process. For instance, the double-angle Al evaporation is a key process to produce high-quality junctions without breaking a vacuum in between the depositions of two Al layers. On the other hand, overlap junctions, which require separate lithography steps for the two layers, are compatible with the CMOS process, but tend to have lower-quality junctions. Importantly, a recent report has shown that the manufacturing process using overlap junctions can produce high-quality transmons [23].

Lastly, a straightforward application of CMOS technology will be the use of cryogenic CMOS for the control of superconducting qubits to minimize the heat load from RT [24]. Cryogenic multiplexer will further reduce the number of required wiring [25]. Alternative ideas are to use single-flux quantum (SFQ) circuits [26], [27] or photonic links [28]. Such continuous technology development will bring large-scale, fault-tolerant quantum computers closer to the reality.

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