3D Simulation Method to Predict Breakdown Voltage of Complex Large-Scale Ring Corner in SJ MOSFET

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***Abstract*—We present a fast and accurate 3D TCAD simulation method to predict breakdown voltage (BV) and charge imbalance process margin in the complicated large-scale ring corner region of a super junction (SJ) MOSFET by building an automatic structure editing algorithm and a proposed BV model. The algorithm automatically analyses 300 ×300 μm² GDS within minutes, subdividing it into more than 50 sections based on the pillar design, and creates a 3D structure using physics-based 2D process simulation for each section. The proposed empirical BV model is established by combining the maximum electric-field extracted from 3D TCAD simulation and experimental BV results obtained from different ring corner designs. We developed a 650V-class SJ MOSFET using the proposed method. To find better design solution, the proposed simulation method can be used to analyze the design weakness of the ring corner by evaluating the spatial distribution of the electric field. In addition, the measured BV value and thermal emission microscope images show that the proposed method is accurate in predicting BV levels and BV hot spots. Therefore, it can be seen that the proposed 3D analysis method is valuable for predicting BV in SJ ring corners and can be expanded to other large devices in a fast and accurate way using 3D TCAD.**

Keywords—3D TCAD Simulation, Super Junction MOSFET, Power Devices, Edge Termination, Ring Corner.

I. Introduction

The super junction (SJ) MOSFET has been widely used in power electronics industries, particularly in switching mode power supplies, due to its advantageous characteristics such as excellent trade-off behavior between breakdown voltage (BV) and on-state resistance (Rsp), shorter reverse recovery time, and high-speed switching capability [1-2]. For next-generation, the lateral pitch size should in principle be narrowed to maintain a high BV while increasing the pillar doping concentration to further reduce Rsp. However, this approach results in narrowing manufacturing process margins. In SJ MOSFETs, for given Rsp target, widening the process control margin for BV caused by charge imbalance is a key for achieving process controllability in mass production [3-8]. SJ MOSFET is a single device consisting of an active (cell) and ring regions, as shown in Fig. 1(a). Careful design of the charge imbalance margins in each region, including the active (cell), x-direction ring, y-direction ring, and ring corner, is required to maximize the overall process control margin determined by the minimum BV of the entire region, as described in Fig.1(b). Once the structure of the main pillar of the active area (cell) is determined, the design of the ring regions becomes critical in meeting the BV criteria, as BV in the ring region is typically lower than that in the active region. Pre-evaluating the BV of each region requires TCAD simulations for the subdivided ring area. However, the ring corner in SJ MOSFET generally has a complicated structure, and the simulation domain for the ring corner can be a few hundred micrometers, resulting in difficulties such as time-consuming and costly work compared to other regions. Therefore, in this study, we propose a fast and accurate 3D TCAD simulation method to estimate BV and charge imbalance process margin for large-scale ring corner in SJ MOSFET.

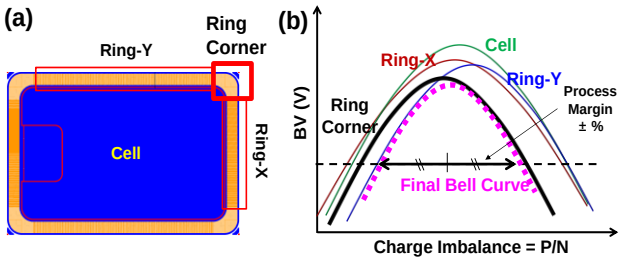

Fig. 1. (a) Top view of SJ MOSFET. (b) Concept of the total process control margin for BV

II. Simulation Method

The proposed method to predict the BV of the SJ ring corner is two-fold: (1) Automatic 3D structure editing algorithm and (2) Empirical BV model using the maximum electric-field (E-field) extracted from 3D simulations. Using the proposed algorithm (Fig. 2(a)), we can analyse the GDS to determine the composition of different pillar structures in the ring corner region and their location information, as shown in Fig. 2(b). Initially, the GDS is subdivided into pieces of equal size. The pitch size, mask size of the main pillar, and p-type mask size of the top surface were used as distinguishing indicators, and if any of them were different, it was judged as a different segment. With different mask information extracted from each segment, 2D process simulation of each area was performed to implement the structure and doping profile. Since the BV of SJ MOSFET is very sensitive to variations in doping concentration even as low as 1%, accurate doping profiles for n/p pillars are generated through fully physics-based 2D

process simulations. Subsequently, 3D ring corner is created by merging the boundary 3D structures with more than 50 different 2D doping profiles (Fig. 2(c) and (d)). All of these processes are performed automatically by the algorithm written in Python.

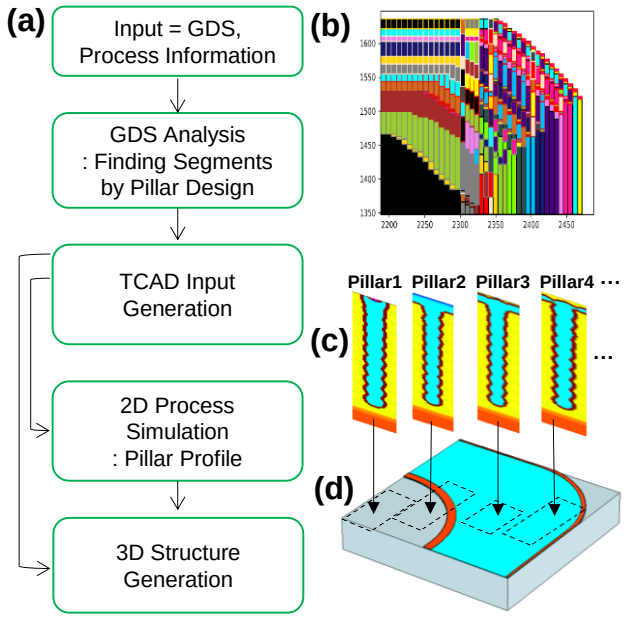

Fig. 2. (a) Procedure of the proposed Automatic 3D structure editing algorithm. (b) Results of identifying regions for each segment with different pillar designs using GDS analysis. Each pillar design structure and location information are extracted. (c) Physics-based 2D process simulations for pillar profiles of each segment. (d) Boundary structure with a backend structure for contacts. By merging (c) and (b), a complete 3D simulation structure for the ring corner can be effectively be created in a short amount of time.

Generally, to evaluate the BV of the device, the Poisson equation as well as the carrier continuity equation are solved using a standard procedure. However, in a large-scaled 3D structure like a ring corner of SJ, which consists of several millions of nodes, following the standard procedure is impractical due to the tremendous simulation time and unpredictable convergence problems [9]. Therefore, this work avoids such problems by proposing an empirical-based BV model to predict the BV. The device simulation includes only the Poisson equation without carrier continuity equations to obtain the maximum E-field, reducing simulation time and minimizing convergence issues during device simulation. For the application of the proposed method, the BV prediction model is generated as a function of the simulated maximum E-field, corresponding to experimentally measured BVs of different ring corner designs merged for BV modeling.

III. Results and Discussion

Fig. 3(a) shows the simulated 3D ring corner structure, which is 300×300 μm^2. The contour in Fig. 3(b) shows the areas where the E-field exceeds 2e5 V/cm. Using the proposed method, 3D simulations of SJ MOSFETs with eight different ring corner designs with having BV hot spot at the ring corner in actual measurements were performed, and the maximum E-field values have been extracted as the fixed drain bias condition. Fig. 3(c) shows the results of the proposed BV model, depicting the relationship between the maximum E-field extracted from 3D TCAD simulations and the measured BVs of the eight devices. The triangle symbols show that is it able to calculate the BV by the proposed model at different charge imbalance points, all using the same ring corner design.

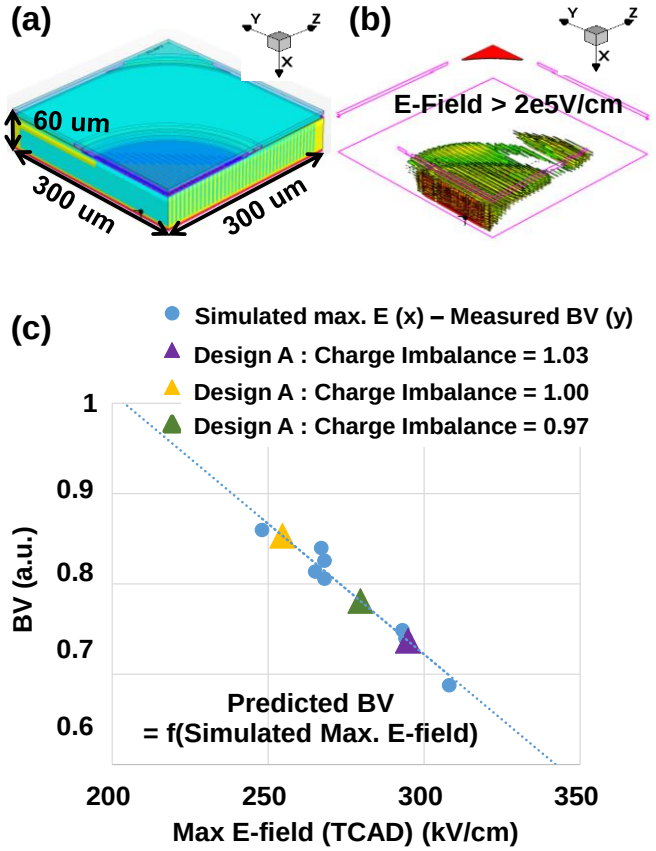

Fig. 3. (a) 3D TCAD-simulated structure and (b) E-field distribution of the SJ ring corner, respectively, using the proposed method. (c) Results of the proposed BV Model. Simulated Max. E-field vs. BV (dot: measured data to build the BV prediction model (dashed line)). The triangle symbols show the predicted BV of Design-A by the proposed BV model).

We first used the propose simulation method to study the design weakness of a ring corner by analyzing the spatial distribution of E-field. When the main pillar design is decided, the boron profile design in the top surface area in ring region has a significant effect on the BV. Fig. 4 shows the spatial distribution of E-field as a result from 3D device simulations for two different ring corner designs with changing the mask critical dimension for boron at the top surface. At the fixed drain bias, in Design-A (Fig.4 (c)), the magnitude of the electric field exceeds the level of 2.5e5 V/cm in a specific area in the lateral direction of the pillar. The solid lines shows the electrostatic potential contours in the fingers on the right in the Fig.4 (c) and (d). The arrow shows the edge of the electrostatic potential which is corresponding to the effective depletion width. To reduce the electric field for the Design-A, the electrostatic potential distribution must be expanded in both Y and Z directions. Therefore, Design-B was built to increase

the boron concentration at the surface by increasing the critical mask size for the designed area in Fig.4 (b). As a result, it can be seen that the electrostatic potential distribution in Design-B is widely expanded, and accordingly, the E-field is reduced to a superior level of 2.5e5 V/cm or less under the same drain bias condition. As the maxium E-field decreases, the predicted BV of Design-B increases by 14% compared to Design-A. It is noted that the proposed simulation method will be very useful to improve design solutions as it can be used to find design weaknesses of the ring corner by analyzing the spatial distribution of the electric field.

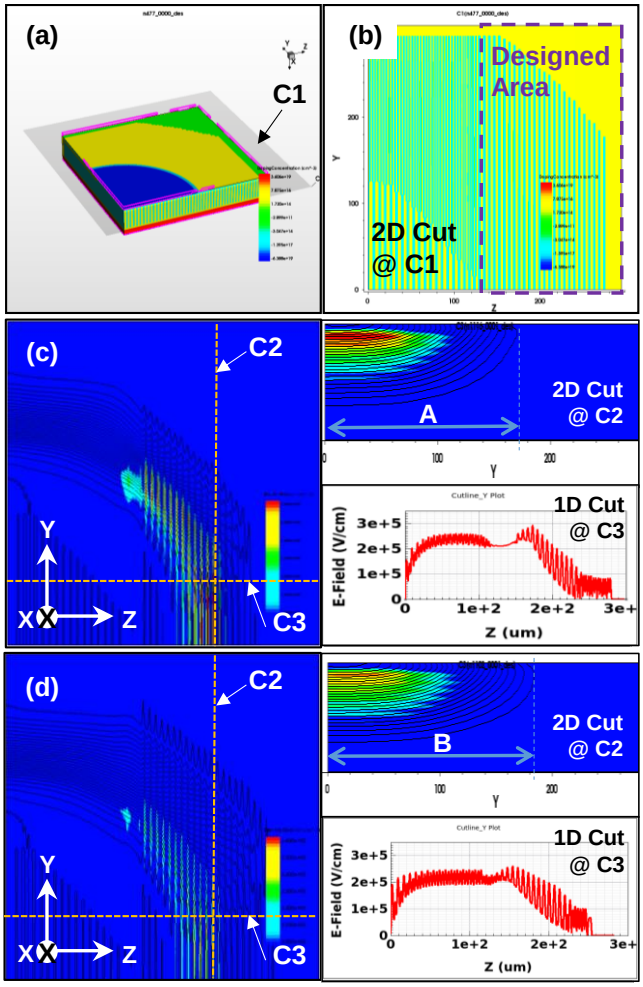

Fig. 4. (a) 3D TCAD-simulated structure. (b) Net doping concentration in the range of -1e19 (blue, boron) to 1e19 (red, phosphorus) on plane C1 in Fig. 4(a). In this case, the critical dimension of the mask for boron implantation is used as a design parameter in the dashed box. (c-d) Simulated E-field on 2D-cut C1, C2, and 1D-cut C3 of the Design-A and Design-B, respectively, in the range of 2.5e5 to 3.0e5 for 2D plane. The solid lines in 2D planes show the electrostatic potential contour. Design-B has wider critical dimension of the mask for boron than Design-A.

A complex large-scale ring corner design was developed on a 650V-class SJ MOSFET using the proposed simulation and design solution method. Fig. 5 shows the results of 3D device simulations for ring corner in 650V-class SJ MOSFET with different charge imbalances. The figures on the left side shows 2D slice-cut at the point of maximum E-field, which is where breakdown occurs for ring corner. Additionally, using the same simulation method, BV simulations were performed on Ring-X and Ring-Y as shown in the tables in the Fig. 5. As mentioned in Fig. 1, since the BV is detemined by the minimum BV of the entire region, the simulation results predicted that BV would occur in the ring corner when the C.I. is 0.97, and BV would occur in the Ring-X when the CI is 1.03, respectively. The simulated BV and breakdown point, according to charge imbalance, exhibit excellent agreement with the measured BV value and the hot spots identified by a thermal emission microscope (THEMOS) images. Notably, it is worth mentioning that the proposed 3D TCAD simulation method allows accurate prediction of the breakdown behavior of large-scale ring corners within 1-2 days.

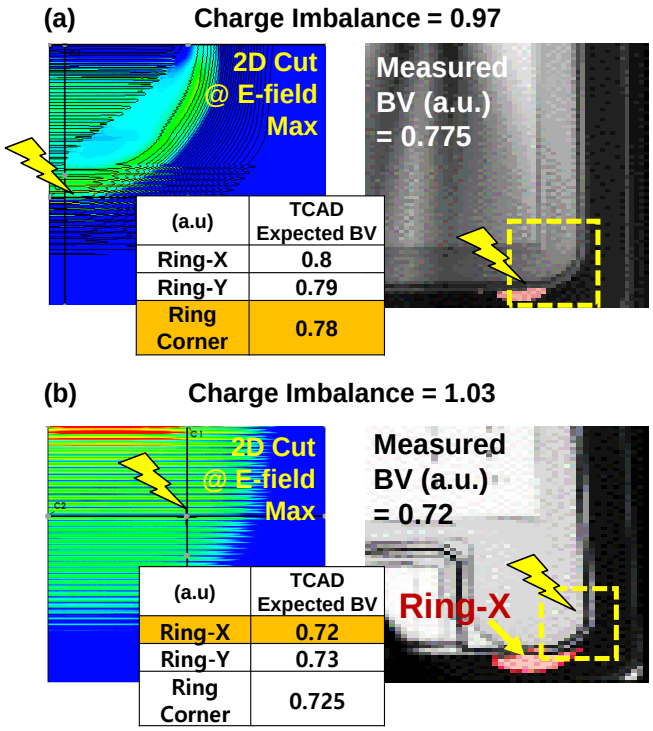

Fig. 5. TCAD vs. Measurement results of devices with different charge imbalances: (a) charge imbalance = 0.97 (N-rich) and (b) charge imbalance = 1.03 (P-rich). Left: 2D image extracted at the Max. E-field in the 3D ring corner simulation. Table shows the simulated BV in different ring regions on the same chip. The orange row section shows the TCAD expected BV value and hot spot. Right: THEMOS images at breakdown in the fabricated 650V-class SJ MOSFETs. The yellow dashed line and lightning image show the simulation domain and predicted BV hot spot by the 3D ring corner simulation.

IV. Conclusions

We proposed a 3D TCAD simulation method to evaluate the BV of the ring corner region in SJ MOSFET. The proposed simulation method can be used to analyze the spatial distribution of the electric field to find structural vulnerability for BV in the ring corner, which will be very useful to obtain design solutions. Using the proposed simulation method, we developed a complex large-scale ring corner design in 650V-class SJ MOSFET. The meausrement data shows that the model can accurately predict both BV level and BV hot spot. In conclusion, it is noted that the proposed 3D simulation method is fast and accurate for predicting the BV and charge

imbalance process margin of SJ ring corners and can be expanded to other complex large-size devices in a cost-effective way using 3D TCAD.

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