Quantum transport simulation of synaptic FETs based on two-dimensional semiconductors

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***Abstract*—We present a quantum transport simulation of synaptic field effect transistors (FETs) based on two-dimensional (2D) semiconductors, especially the phosphorene channel as a representative example, in which the hysteresis of conduction characteristics due to the channel–gate interface trap is used as synaptic plasticity. For this purpose we generalized our previously proposed compact capacitance model for synaptic FETs to include the quantum tunneling effect based on the NEGF method. We found that although the hysteresis behavior is basically reduced when the channel length becomes shorter, appropriate design of the channel length can be beneficial to obtain better synaptic weight change due to larger tunneing leakage current.**

I. Introduction

In recent years, synaptic devices using memristors, two-terminal devices whose resistance changes according to the current flowing through them, have been attracting attention, and are expected to be applied to large-scale integrated neuromorphic systems because of their ultra high speed drive, ultra low power consumption, and high scalability [1], [2].

Two-dimensional atomic film materials, such as graphene, have been attracting attention as next-generation materials due to their unique physical characteristics, including notable electronic properties resulting from their Dirac electron system [6], [7]. In neuromorphic applications, it is believed that high-performance synaptic devices can be realized by exploiting their sensitivity to the surrounding environment, such as charge trapping, due to their very large surface area relative to volume [8]. Synaptic graphene FETs and carbon nanotube FETs have been experimentally fabricated using hysteresis of conduction properties due to interface trapped charges [9], [10]. For the numerical simulation of such devices, we have previously proposed a compact model for synaptic FETs using interface traps, and used this model to explore the synaptic FET property of graphene and graphene nanoribbons.

In our previous study we have assumed that the graphene channel is basically infinitely long and the interface trap is uniformly distributed over the graphene channel, which make it possible to simulate within the compact model. However, in reality it is also important to study the influence of finite channel length and influence of the inhomogeneous trap distribution. With such motivation in mind, in this study we study the effect of the interface trap position in the hysterisis behavior of the 2D channel FET.

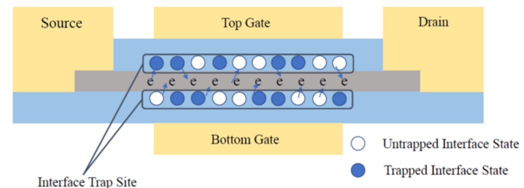

Fig. 1. Model diagram of the FET assumed in this study. Double gating improves the gate voltage effect and doubles the interface area. In addition, it is thought to be able to prevent disturbances from factors other than the channel-oxide film interface.

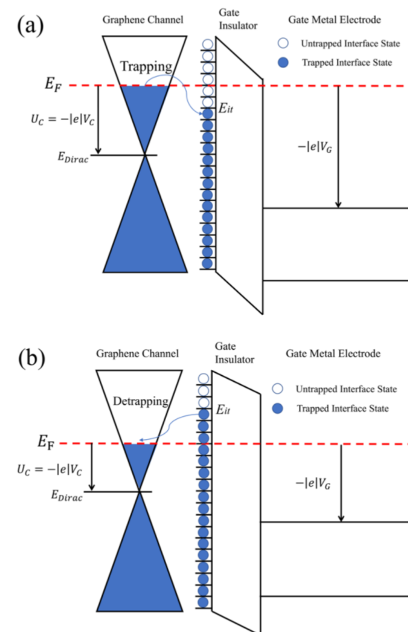

Fig. 2. Energy band diagram of FET and schematization of the interfacial trapping/de-trapping process at different bias conditons: (a) $U_{\rm it} < E_{\rm F}$, and (b) $U_{\rm it} > E_{\rm F}$. This figure is based on Figure 2 (c), (d) in Reference [14].

II. Model and Methods

Figure 1 shows a schematic diagram of the device structure considered in this study. As a representative model of the channel material we consider monolayer phosphorene. Figure 2 shows the energy band diagram of FET and schematization of the interfacial trapping/de-trapping process at different bias

conditons.

Electronic properties of phosphorene shown in Fig. 1 (left) can be analyzed effectively using the tight-binding (TB) model [11], where the band structure is calculated by solving the eigenvalue problem $H(\boldsymbol{k})\left|\psi_{l\boldsymbol{k}}\right\rangle = E_l(\boldsymbol{k})\left|\psi_{l\boldsymbol{k}}\right\rangle$ with the $\boldsymbol{k} = (k_x, k_y)$ dependent 4×4 TB Hamiltonian $H(\boldsymbol{k})$. Then the electronic band structure is obtained as shown in Fig. 2, where the band gap energy is estimated to be 1.52 eV. Although such matrix eigenvalue problem can be solved using standard eigensolver, since the method capable of solving eigenvalue problem efficiently is needed, it is also interesting to introduce quatum computational approach to calculate the electronic band structure materials based on tight-binding model, especially using Variational Quantum Eigensolver (VQE). VQE is one of hybrid quantum-classical algorithms and can compute the ground state based on the variational principle, combined with classical optimization. To calculate the excited stae, variational quantun deflation algorithm (VQD) is available [12].

Then electronic transport properties of phosphorene TFET can be modeled by the following two-band effective mass equation model [13].

$$\left[-\frac{\hbar^2}{2m_{c,x}^*}\frac{d^2}{dx^2} + E_c + V(x) + \varepsilon_c\left(k_y\right)\right]\psi_c(x) + C\frac{dV(x)}{dx}\psi_v(x) = E\psi_c(x) \tag{1}$$

$$\left[-\frac{\hbar^2}{2m_{v,x}^*}\frac{d^2}{dx^2} + E_v + V(x) + \varepsilon_v\left(k_y\right)\right]\psi_v(x) + C\frac{dV(x)}{dx}\psi_c(x) = E\psi_v(x), \tag{2}$$

where $\varepsilon_c(k_y) \equiv \hbar^2 k_y^2/(2m_{c,y}^*)$ and $\varepsilon_v(k_y) \equiv \hbar^2 k_y^2/(2m_{v,y}^*)$ are the transverse energy dispersions for the conduction and valence bands, respectively, and the effective masses for the conduction (valence) band are $m_{c(v),x}^*$ and $m_{c(v),y}^*$ for x and y directions. We choose the x direction to be the transport direction, which is either the armchair or zigzag direction. The conduction band effective masses are extracted from the TB band structure as $m_c^* = 0.152m_0$ and $0.763m_0$ for armchair and zigzag directions, respectively, and corresponding valence band values are $m_v^* = 0.203m_0$ and $1.526m_0$, respectively. The parameter C is the inter-band coupling constant [13].

We descretize the above two-band effective mass equations based on the finite difference method and then employ the standard NEGF method along with the Poisson's equation. In the presence of the interface trap sites, the Poisson's equation can be expressed as the capacitance model generalized to include the interface trap charge, which can be schematically expressed as shown in Fig. 3. The site charge Q_i within the ith mesh site is calculated based on the NEGF method self-consistently with the Poisson's equation

$$[C]\,\mathbf{V} = \mathbf{Q}\left(\mathbf{V}\right) + \mathbf{Q}_{\mathrm{it}}\left(\mathbf{V}\right), \tag{3}$$

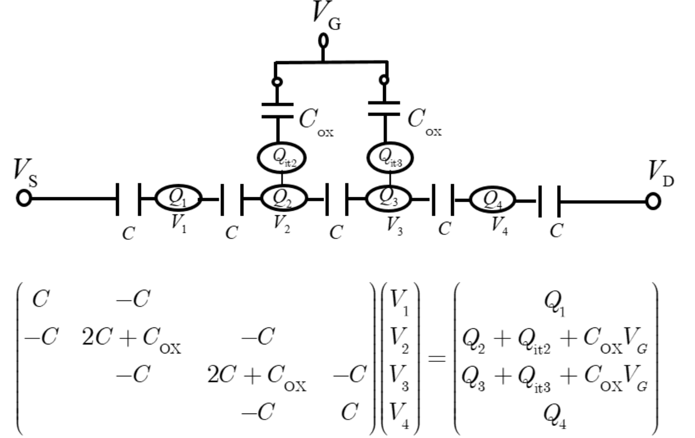

Fig. 3. Schematic illustration of the capacitance model generalized to include the interface trap charge, where C is the channel capacitance derived by finite-differentiating the Poisson's equation, and C_{OX} is the oxide layer capacitance. In this illustration there are only a few mesh sites within the channel but in the actual simulations we assume that the mesh spacing is 0.25 nm through the simulation region.

which is solved iteratively following the Newton's scheme as

$$\mathbf{V}^{(k+1)} = \mathbf{V}^{(k)} + \Delta\mathbf{V}^{(k)} \tag{4}$$

$$\left[J\left(\mathbf{V}^{(k)}\right)\right]\Delta\mathbf{V}^{(k)} = -\mathbf{f}\left(\mathbf{V}^{(k)}\right) \tag{5}$$

$$\mathbf{f}\left(\mathbf{V}^{(k)}\right) = [C]\,\mathbf{V}^{(k)} - \mathbf{Q}\left(\mathbf{V}^{(k)}\right) - \mathbf{Q}_{\mathrm{it}}\left(\mathbf{V}^{(k)}\right) \tag{6}$$

$$\left[J\left(\mathbf{V}\right)\right] = [C] + \left[C^{(\mathrm{QC})}\left(\mathbf{V}\right)\right] + \left[C^{(\mathrm{it})}\left(\mathbf{V}\right)\right] \tag{7}$$

$$\left[C^{(\mathrm{QC})}\left(\mathbf{V}\right)\right]_{ii} \equiv -\frac{\partial Q_i\left(\mathbf{V}\right)}{\partial V_i}, \quad \left[C^{(\mathrm{it})}\left(\mathbf{V}\right)\right]_{ii} \equiv -\frac{\partial Q_{\mathrm{it}}\left(\mathbf{V}\right)}{\partial V_i} \tag{8}$$

In order to study the trap-induced hysterisis behavior of the phosphorene FET based on the NEGF method, we generalize our proposed formalism in Ref.[15] to describe the interface charge density profile (vector) at the jth voltage time step $\mathbf{Q}_{\mathrm{it}}^{(j)}$ as

$$\mathbf{Q}_{\mathrm{it}}^{(j)} = \mathbf{Q}_{\mathrm{it}}^{(j-1)} + \Delta\mathbf{Q}_{\mathrm{it}}^{(j)}, \tag{9}$$

$$\Delta\mathbf{Q}_{\mathrm{it}}^{(j)} = -e\int_{E_{\mathrm{it}}^{(j-1)}}^{E_{\mathrm{it}}^{(j)}} \mathbf{D}_{\mathrm{it}}(E)dE \tag{10}$$

$$E_{\mathrm{it}}^{(j)}\left(\mathbf{r}\right) = \left(eV_{\mathrm{C}}(\mathbf{r}, V_{\mathrm{G}}^{(j)}) - E_{\mathrm{it}}^{(j-1)}\left(\mathbf{r}\right)\right) \tag{11}$$

$$\times\left(1 - \exp(-\Delta t_{\mathrm{G}}/\tau_{\mathrm{trap}})\right) + E_{\mathrm{it}}^{(j-1)}\left(\mathbf{r}\right) \tag{12}$$

$$\Delta t_{\mathrm{G}} = \frac{\Delta V_{\mathrm{G}}}{\chi_{\mathrm{sweep}}} \tag{13}$$

where E_{it} is the top of the occupied interface level measured from the Dirac point in graphene, $V_{\mathrm{C}}(V_{\mathrm{G}})$ is the graphene channel potential for a given gate voltage V_{G}, $D_{\mathrm{it}}(E)$ [eV^{-1}·m^{-2}] is the interface density of states, τ_{trap} [ms] is the trapping/de-trapping time constant, and χ_{sweep} [V/ms] is the gate voltage sweep rate. On the basis of the

experimental results of previous studies, $D_{\rm it}(E)$ is treated as energy independent constant. We note that $\Delta t_{\rm G}$ is interpreted as the time required to sweep the gate voltage by $\Delta V_{\rm G}$, and the factor $1-\exp(-\Delta t_{\rm G}/\tau_{\rm trap})$ is the the probability that the interface states are actually trapped during the gate voltage sweep by $\Delta V_{\rm G}$. The quantities such as $\mathbf{Q}_{\rm it}^{(j)}$ and $V_{\rm C}(\mathbf{r}, V_{\rm G}^{(j)})$ in the above equations are calculated sysmatically based on the NEGF method [16].

III. Results and discussions

In Fig. 4 we show the typical result of the calculated potential profiles for the gate voltage $V_{\rm G}$ forward scan from 0 to 1.5 V, followed by the backward scan from 1.5 to 0 V, where the channel length is 5 nm, and the gate insulator is SiO_2 with the thickness $t_{\rm ox} = 1$ nm. The source and the drain region are n-doped with the doping density $N_{\rm D} = 3\times10^{17}$ $\rm m^{-2}$. The interface density of states is $D_{\rm it} = 0.3D_{\rm it0}$ with $D_{\rm it0} = 3.75\times10^{16}$ $\rm m^{-2}eV^{-1}$, trap/detrap time constant is $\tau_{\rm trap} = 100$ ms, and the gate sweep rate is $\chi_{\rm sweep} = 0.01$ V/ms.

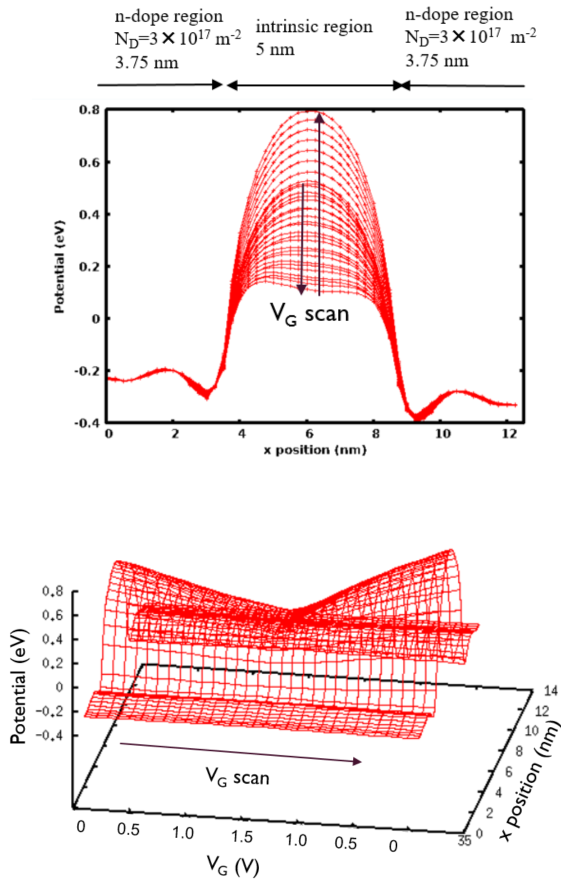

Fig. 4. Calculated potential profiles for the gate voltage $V_{\rm G}$ forward scan from 0 to 1.5 V, followed by the backward scan from 1.5 to 0 V, where the channel length is 5 nm, the interface density of states is $D_{\rm it} = 0.3D_{\rm it0}$ with $D_{\rm it0} = 3.75\times10^{16}$ $\rm m^{-2}eV^{-1}$, trap/detrap time constant is $\tau_{\rm trap} = 100$ ms, and the gate sweep rate is $\chi_{\rm sweep} = 0.01$ V/ms.

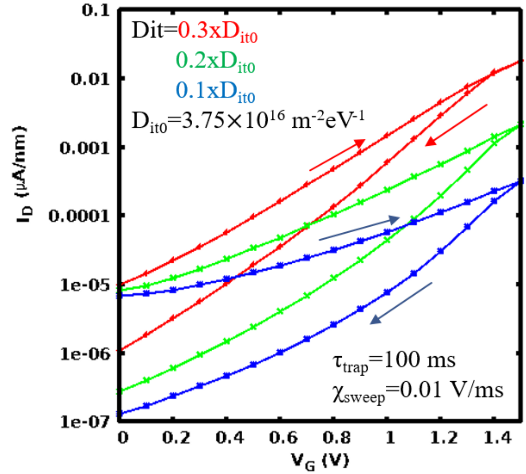

Fig. 5. Conduction characteristics of phosphorene FETs under a linear gate voltage sweep $V_{\rm G}$ 0 to 1.5 V. Drain voltage is $V_{\rm D} = 0.3$. Results for different values of the interface density of states are compared.

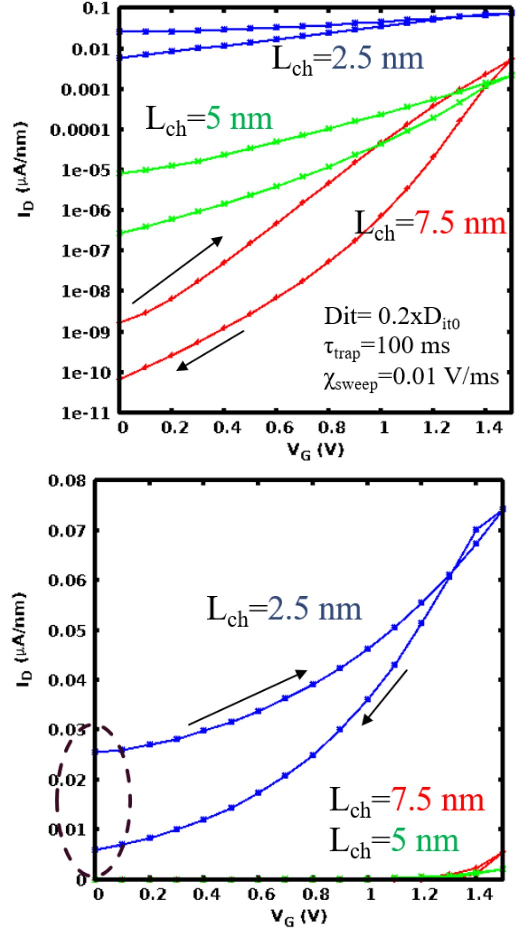

Fig. 6. Conduction characteristics of phosphorene FETs under a linear gate voltage sweep $V_{\rm G}$ 0 to 1.5 V. Drain voltage is $V_{\rm D} = 0.3$. In the top panel the results for different channel length are compared. In the bottom panel the same results are plotted in the linear scale to emphasize the result for $L_{\rm ch} = 2.5$ nm.

As we can see in Fig. 4, the potential barrier heights at the initial $V_{\mathrm{G}} = 0$ V and at the final $V_{\mathrm{G}} = 0$ V (after the backward sweep) are different, and barrier height at the final $V_{\mathrm{G}} = 0$ V is heigher than the initial one. This is due to the accumulated trap change, which suppresses the gate voltage induced change of the potential value. Such behavior results in the hysteresis behavior of the I_{D}-V_{G} characteristics as shown next.

In Fig. 5 we show the conduction characteristics under the forward V_{G} sweep from 0 to 1.5 V followed by the backward sweep from 1.5 to 0 V. Drain voltage is $V_{\mathrm{D}} = 0.3$. Results for different values of the interface density of states are compared. Here we can see the significant hysteresis behavior, and the current difference between the initial $V_{\mathrm{G}} = 0$ and the final $V_{\mathrm{G}} = 0$ is larger for larger D_{it}. Next in Fig. 6 we show the forward and backward V_{G} sweeped results for three different chanel length L_{ch}. In the top and the bottom panels the calculated current values are plotted in the log scale and the linear scale, respectively. Here we can see in the top panel that the showter channel length results in the reduced hysteresis behavior. However, it is noted that for the longer channel length the current values at $V_{\mathrm{G}} = 0$ is deep in the off-regime, which is disadvantageous for the synaptic device application because of the too small current. On the other hand, when the channel length is short, the current values at $V_{\mathrm{G}} = 0$ is relatively large. Therefore, although the hysteresis behavior is basically reduced when the channel length becomes shorter, appropriate design of the channel length can be beneficial to obtain better synaptic weight change due to larger tunneing leakage current.

IV. Conclusion

We presented a quantum transport simulation of the phosphorene channel synaptic field effect transistors (FETs), in which the hysteresis of conduction characteristics due to the channel–gate interface trap is used as synaptic plasticity. For this purpose we generalized our previously proposed compact capacitance model for synaptic FETs to include the quantum tunneling effect based on the NEGF method. We found that although the hysteresis behavior is basically reduced when the channel length becomes shorter, appropriate design of the channel length can be beneficial to obtain better synaptic weight change due to larger tunneing leakage current.

Acknowledgment

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