Source-to-drain Tunneling Analysis in p-type Si and Ge Based NWTs/NSTs

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***Abstract*—We examine the dependence of source-to-drain tunneling (SDT) leakage on the effective channel length (L_{eff}) for Si and Ge pMOS with L_{eff} ranging from 5 nm to 20 nm. The subband Boltzmann transport equation is solved including the SDT process, which is evaluated from the WKB approximation. Device architectures including nanosheet transistors (NSTs) and nanowire transistors (NWTs) with the proper specification are analyzed. The results show that SDT becomes a serious concern for Ge pNSTs with L_{eff} lower than 17 nm. However, such leakage degradation from SDT, can be further mitigated by optimizing the cross-sectional configuration.**

I. Introduction

Channel length scaling for Si MOSFETs has slowed down and is predicted to saturate at 12 nm, according to the latest edition of the technology roadmap [1]. One of the major limits that follow channel length scaling is the increased source-to-drain tunneling (SDT) leakage [2, 3], which degrades the overall performance after workfunction tuning to meet the off-state current requirements. To provide further enhancement for on-state currents, Ge p-channel [4, 5] has been introduced as a promising replacement for its Si counterpart due to the high hole mobility. However, with its small transport effective mass, Ge pMOS may be more vulnerable to SDT degradation [6, 7]. Whether the alternative Ge p-channel still benefits from its superior mobility at short-channel devices is questionable. For a quantitative assessment, we have carried out a comparative leakage analysis on Ge pMOS against Si pMOS to determine the scaling limit and fundamentally provide the design guidelines.

II. Methodology

Si and Ge p-channel nanosheet transistors (NSTs) and nanowire transistors (NWTs) shown in Fig. 1 are chosen to study the off-state current characteristics. To investigate the SDT at scaling limit, effective channel length (L_{eff}) ranging from 5 nm to 20 nm are simulated, where the two architectures can still sustain good electrostatic control. Channel orientation is set to $\langle 110 \rangle$ for both device architectures and the major confinement orientation for NST is (100), with specification listed in Table I.

To capture the quantum confinement and SDT effects, the subband Boltzmann transport equation (SBTE) solver and six-band $\mathbf{k}\cdot\mathbf{p}$ valence band parameters have been implemented for both Si and Ge pMOS. The solver allows to directly include the tunneling process by evaluating the WKB formula from the complex subband structure, which has been presented in [7–9]. For SDT, the transmission coefficients (TC) are computed from

$$TC(E_0) = \exp\left[-2\int_{x_1}^{x_2} \frac{\sqrt{2m^*(V(x)-E_0)}}{\hbar} \mathrm{d}x\right] \quad (1)$$

for each energy E_0, between classical turning points x_1 and x_2, where m^* is the transport effective mass of the complex subband. The tunneling spectral current density per subband through the barrier is then given by the Tsu-Esaki-formula,

$$j_n(E_0) = -\frac{g_v q}{\pi\hbar} TC_n(E_0)[f_n(E_0,x_1) - f_n(E_0,x_2)] \quad (2)$$

where g_v denotes the valley degeneracy and $f_n(E,x)$ is the distribution function of n-th subband at the respective turning points of each energy.

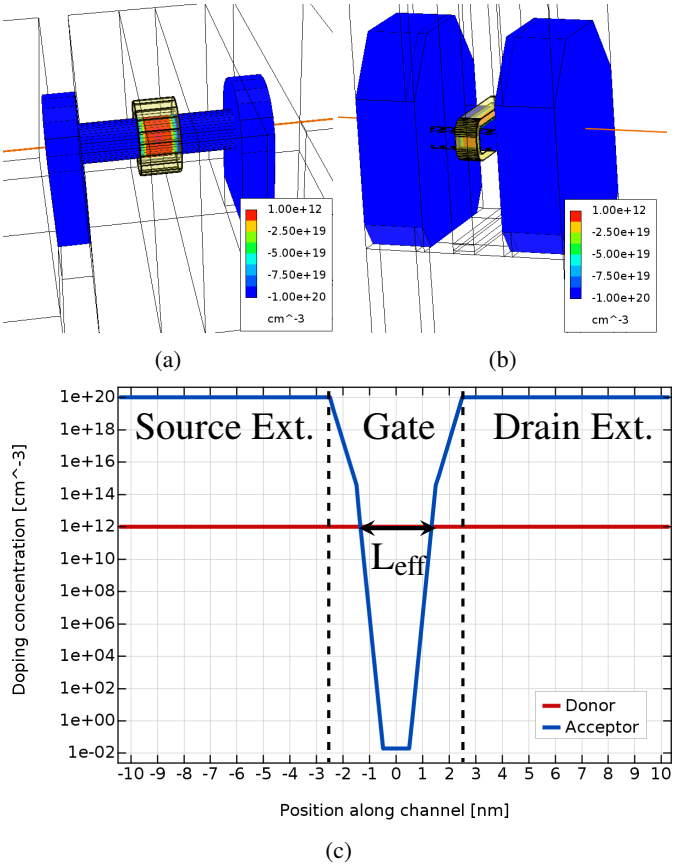

Fig. 1: Net doping (donor: +, acceptor: −) of simulated (a) NWT and (b) NST. The same graded doping profiles along the channel are applied to both device architectures, as shown in (c).

Architechture	NWT (D = 5 nm)	NST (H/W = 5/20 nm)
Spacer length	7 nm	
Channel length (L_{eff})	5–20 nm	
SiO_2 thickness	0.7 nm	
HfO_2 thickness	1.5 nm	
Channel doping	10^{12} cm^{-3}	
S/D doping	10^{20} cm^{-3}	

TABLE I: Geometry specification of studied devices.

To properly analyze the off-state characteristics between each device, we fixed the extraction conditions at $|I_D|$ = 0.1 nA and $|V_D|$ = 0.8 V. Accordingly, attributes such as potential profiles, TC, tunneling current spectra, and subthreshold-slopes (SS) are compared. In this work, we first examined the essential factors that govern the tunneling current. Afterward, the dependences of SDT on channel material and device architecture are investigated. Finally, we benchmarked the SS versus L_{eff} ranging from 5 nm to 20 nm, to check the impact of SDT on channel length for Si and Ge pMOS.

III. Result and Discussion

Eqn. 1 indicates that TC is determined by several factors: (1) potential barrier in the classically forbidden region, (2) tunneling distance between the two classical turning points, and (3) the transport effective mass derived from the complex subbands. Fig. 2 suggests that for the same off-state conditions and device architecture, both Si and Ge pMOS share similar potential profiles along channel direction. Hence in Fig. 3, the significantly larger TC for Ge pMOS originates from its complex subband structure. While NWT in general exhibits better electrostatic control (longer tunneling distance) over NST, Ge pMOS is more vulnerable to SDT due to its intrinsically small transport effective mass.

The total tunneling current spectrum is then computed from Eqn. (2) by summing over the current contribution from each subband, as shown in Figs. 4(a–d). From the total current spectra in Figs. 4(a–d), there is an obvious tunneling current peak located at energy ∼0.3 eV, which corresponds to the top-of-the barrier (ToB) of the first subband. After the carrier energy exceeds ToB, where TC by definition reaches unity, the current decays exponentially along with the carrier population. The tunneling current reaching its maximum at the ToB, indicates that the potential barrier can effectively block the SDT leakage and the off-state current is still dominated by thermionic transport. On the other hand, the other tunneling peak located around Fermi energy (0 eV) is found in Figs. 4(c, d). Ge pMOS with higher TC provides a comparable amount of tunneling current to that from ToB, which is not observed in Figs. 4(a, b). This suggests that thermionic transport no longer governs the off-state current and SDT should be taken into consideration under such highly scaled channels.

It is also worth noting from Figs. 4(b, d) that the tunneling current is mostly contributed from the ground state. Due to the additional energy split from the other confinement direction, NWT has fewer subbands engaged in tunneling process comparing with that of NST.

Finally, we examine the SS-L_{eff} dependence from the simulations with and without the SDT process, as shown in Figs. 5(a, b). By comparing the SS-L_{eff} relationship with and without the SDT process, we have managed to identify the channel length where SDT becomes non-negligible. It is shown in 5(a) that SDT degradation becomes an issue for Ge pMOS with L_{eff} below 17 nm while Si pMOS can persist in its swing control until 9 nm. Nevertheless, the degradation can be further mitigated by optimizing the cross-sectional configuration by (1) replacing from NST tp NWT, or (2) shrinkage of the cross-sectional size, as shown in Figs. 5(a) and (b), respectively. Such improvements can be attributed to the reduced number of subbands for tunneling.

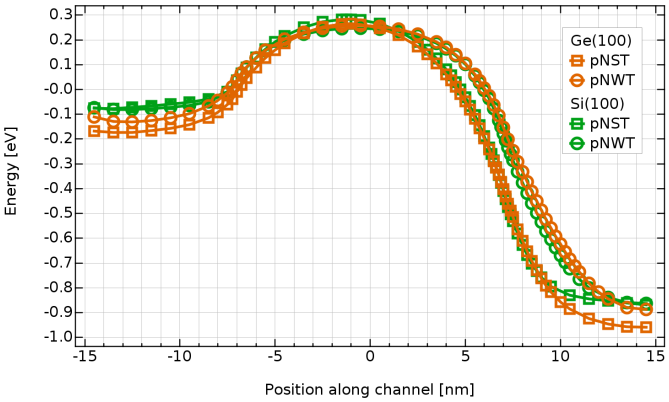

Fig. 2: Potential profiles of Si pMOS and Ge pMOS along the channel, which are denoted with green lines and orange lines, respectively. Profiles both NST (square symbol) and NWT (circle symbol) are extracted at L_{eff} = 12 nm, $|I_D| = 0.1nA$ and $|V_D| = 0.8V$.

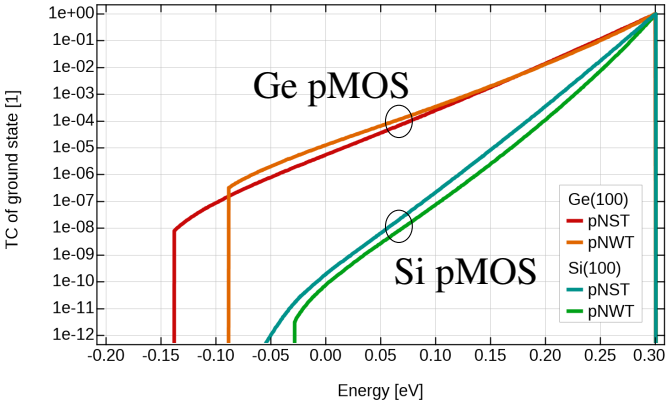

Fig. 3: TC computed from the first subband of Si and Ge pMOS with their values reach unity above the ToB. The results are extracted at L_{eff} = 12 nm, $|I_D|$ = 0.1 nA and $|V_D|$ = 0.8 V.

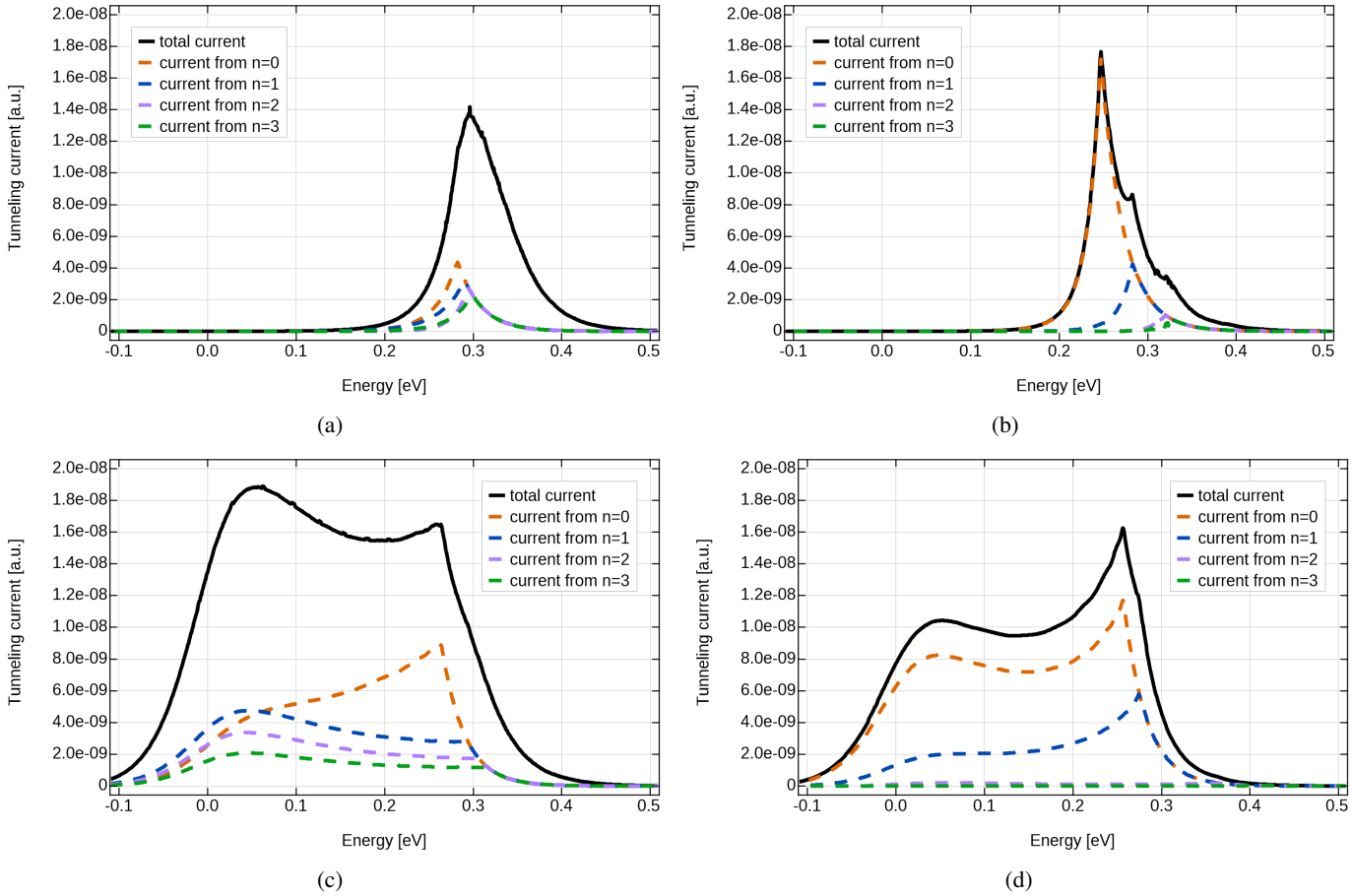

Fig. 4: Tunneling current spectra of (a) Si pNST (b) Si pNWT (c) Ge pNST and (d) Ge pNWT extracted at L_{eff} = 12 nm, $|I_D|$ = 0.1 nA and $|V_D|$ = 0.8 V. Total tunneling current spectra (solid lines) are obtained by summing over the tunneling currents from each subband (dashed lines). Shown in the figures are the first 4 subbands, marked as n = 0, 1, 2, 3.

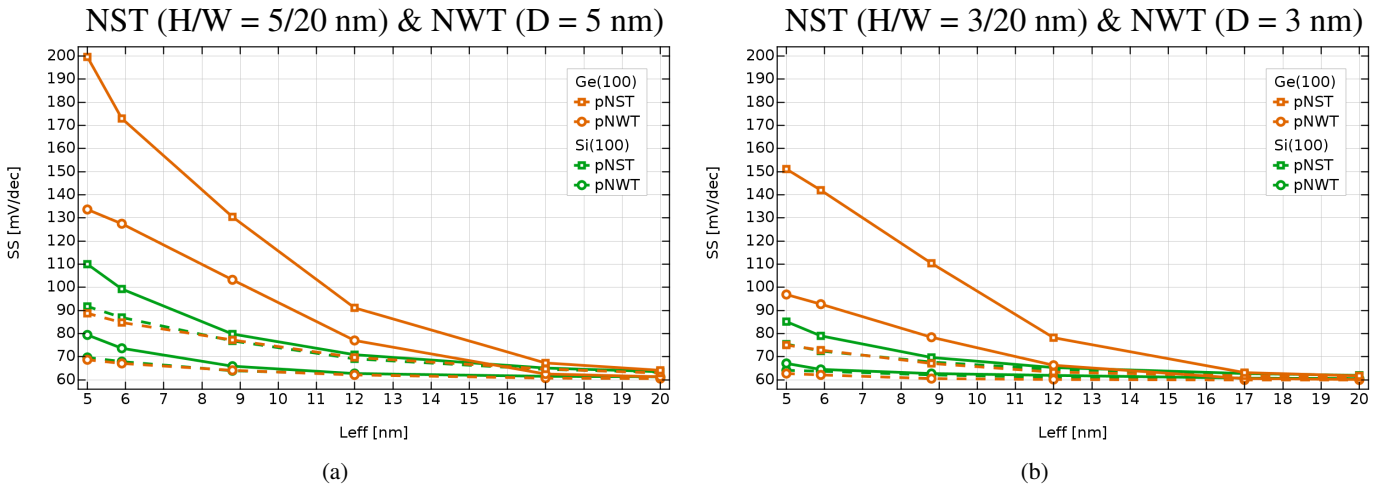

Fig. 5: Dependence of SS on L_{eff} for NSTs (square) and NWTs (circle) with (a) sheet height = wire diameter = 5 nm and (b) sheet height = wire diameter = 3 nm. Solid lines and dashed lines are extracted from simulations with and without SDT, respectively. SS are extracted at $|I_D|$ = 0.1 nA and $|V_D|$ = 0.8 V with L_{eff} varying from 5 nm to 20 nm.

IV. Conclusion

We have demonstrated that Ge pMOS compared with Si pMOS are more vulnerable to SDT for short-channel devices, primarily due to the small transport effective mass. While Si pMOS can be potentially scaled down to L_{eff} = 9 nm without suffering from SDT leakage, the effect becomes non-negligible for Ge pMOS with L_{eff} below 17 nm. As further channel length scaling, the unacceptable off-state leakage will hinder the on-state performance boost for the Ge channel. On the other hand, SS can be further improved by suppressing the number of subbands able for tunneling. This can be achieved by enhancing the confinement from the other direction, e.g., from NST to NWT, or by reducing the cross-sectional size of the device.

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