Effect of Si Separator in Forksheet FETs on Device Characteristics Investigated by Using In-House TCAD Process Emulator and Device Simulator

In Ki Kim, Seung-Cheol Han, Geonho Park, Geon-Tae Jang, and Sung-Min Hong
School of Electrical Engineering and Computer Science (EECS)
Gwangju Insititute of Science and Technology (GIST)
Gwangju, South Korea
smhong@gist.ac.kr

***Abstract*—In this work, we investigate the effect of a Si separator on the performance of a bottom dielectric isolated (BDI) forksheet field effect transistor (FSFET) using our in-house TCAD process emulator and device simulator. The in-house process emulator is implemented with the 3D multi-level-set method and the relevant fabrication process is followed. Two versions of the BDI FSFET with and without a Si separator are generated and the one with a Si separator shows a better etch profile. The electrical characteristics of each device are simulated through our in-house device simulator, G-Device. From the simulation results, it is clearly demonstrated that the electrical characteristics of the FSFET with a BDI are negligibly affected by the Si separator, when the Si separator is very thin.**

I. Introduction

The CMOS technology has undergone significant advancements of device architecture for high density integration, from the planar MOSFET to the FinFET and then to the nanosheet FET (NSFET) [1]. Thanks to the reduced N/P space, the FSFET is considered as the next generation device structure after the NSFET. However, the reduced N/P space introduces an increased difficulty in the substrate doping required for the junction-based isolation. The challenging doping process can be skipped by introducing the BDI [2-4]. Although the BDI offers a solution for eliminating the challenging substrate doping process, a geometric problem with a sloped etch profile of the sacrificial layer can be caused in the BDI formation process. Since the sloped etch profile may increase the difficulty of gate oxide and workfunction metal formation process, the etch profile needs to be improved. In [4], the geometric problem is addressed by introducing the Si separator. However, since the Si separator introduces a significant modification of the device cross section, it is essential to assess the effect of the Si separator on the device fabrication and the electrical characteristics.

In this work, the effect of the Si separator on the fabrication and the performance of a BDI FSFET is investigated with our in-house TCAD process emulator and device simulator. The organization of this extended abstract is as follows. In the process emulation (Section II), improvement of the etch profile in the BDI formation process and its effect on the overall fabrication process is investigated. And the effect of a thin Si separator on the electrical performance is investigated through the device simulation considering the quantum confinement effect in Section III. Finally, the conclusions are made in Section IV.

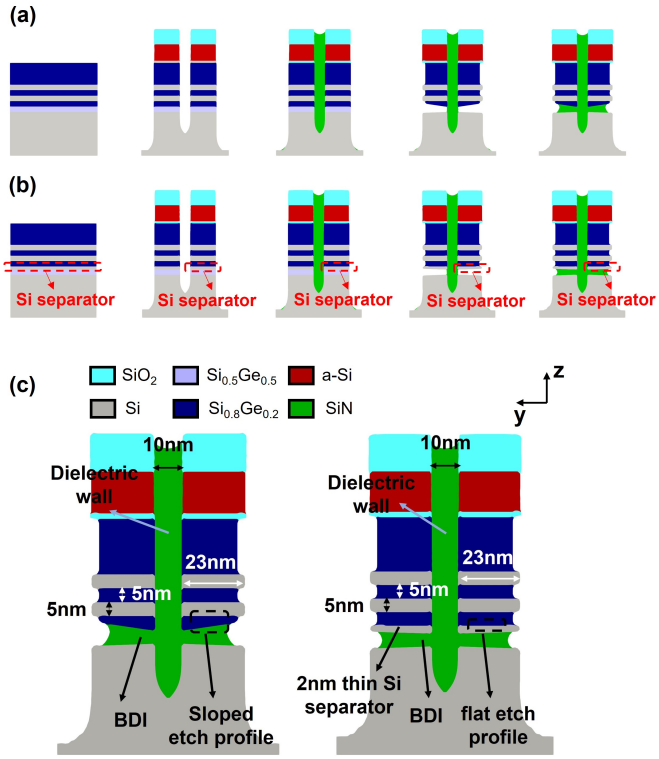

Fig. 1. (a) BDI formation process flow without a Si separator (b) BDI formation process flow with a Si separator (c) Cross sections of FSFETs after BDI formation process flow without a Si separator (left) and with a Si separator (right)

II. Process Emulation

The process emulation of the FSFET with the BDI has been conducted by using the in-house process emulator im-

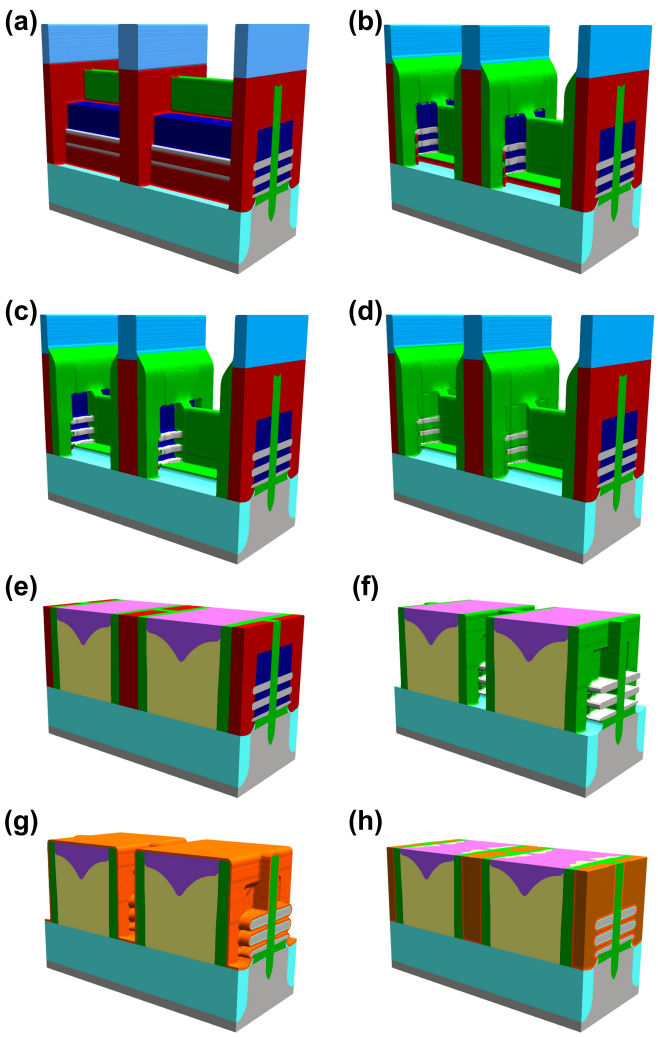

Fig. 2. Process emulation flow of the FSFET (a) Dummy gate etching (b) S/D region etching (c) $Si_{0.8}Ge_{0.2}$ sacrificial layer recess (d) Inner spacer formation (e) S/D epitaxial growth S/D contact formation (f) $Si_{0.8}Ge_{0.2}$ sacrificial layer release (g) Gate oxide formation (h) Gate metal deposition

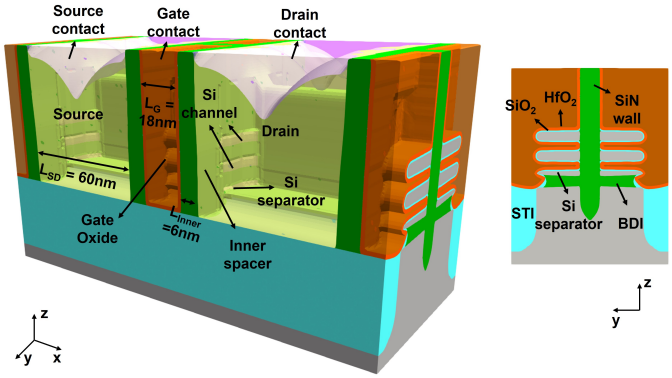

Fig. 3. Three-dimensional structure (left) and cross section (right) of the process emulated FSFET.

plemented with the 3D multi-level-set method [5]. The sparse field level-set method is also employed for fast computation and the boundary extraction is conducted by using the marching cube method [5][6]. First, the SiGe sacrificial layer profile after the BDI formation process has been investigated. Without the Si separator, the SiGe sacrificial layer exhibits a sloped profile after the SiGe replaced layer release process, as shown in Fig. 1(a). It is because the bottom side of the SiGe sacrificial layer is exposed and damaged by the etcher during the release process due to the low selectivity, which is 7:1 in this case. The reduced space between the lower Si channel and the BDI makes the gate metal filling process difficult.

On the other hand, introducing the Si separator can address such a problem. Since the bottom side of the SiGe sacrificial layer is protected by the Si separator during the release process, the flat profile of SiGe sacrificial layer is obtained, as shown in Fig. 1(b). The BDI formation results of both cases are compared in Fig. 1(c). As shown in the Fig. 1(c), when comparing the cross sections of two devices, it is seen that the etch profile of SiGe sacrificial layer is clearly improved by adding the Si separator.

The subsequent process emulation after the BDI formation has been conducted. Fig. 2 depicts the entire FSFET process flow for the case with the Si separator. Dummy gate and S/D region pattering are conducted for defining the channel region and epitaxial growth of doped Si, respectively. Next, the SiGe sacrificial layer is recessed and a 6-nm-thick inner spacer is formed, as shown in Figs. 2(c) and 2(d). After the inner spacer formation, the epitaxial growth of source/drain and the source/drain contact formation have been conducted in the etched region. To form the gate oxide (SiO_2 and HfO_2) and the gate metal, the SiGe sacrificial layer and the dummy gate are released, and the gate oxide formation and the gate metal deposition have followed, as shown in Figs. 2(f) - 2(h). The thicknesses of SiO_2 and HfO_2 layers are set as 0.7 nm and 1.5 nm, respectively.

The three-dimensional structure and the cross section of the generated device structure are shown in Fig. 3. The geometric parameters are as follows. The contacted poly pitch (CPP) is 90 nm, which is defined with a 6 nm-thick inner spacer, the channel length of 18 nm, and the source/drain length of 60 nm. And the thickness and the width of the Si channel are 5 nm and 23 nm, respectively. Thanks to the flat profile of SiGe sacrificial layer, the device is successfully fabricated without gate oxide merging, as shown in Fig. 3.

III. Device Simulation

The device simulation is conducted to evaluate the effect of the Si separator on electrical characteristics by using the in-house device simulator, G-Device [7]. The half of the device structure with a shorter source/drain length (5 nm) is simulated for efficient computation. The mesh for the device simulation is generated by using TetGen [8].

In order to compare the difference due to the Si separator, the device structures are generated with and without the Si separator. The cut sections of two simulated device structures are presented for the cases with and without Si separator in

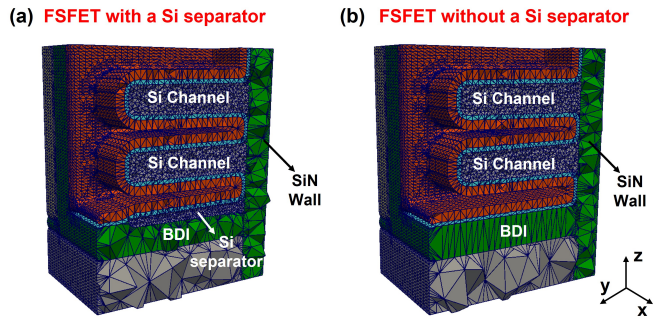

Fig. 4. Generated mesh for device simulation. The cut views are represented. (a) FSFET with a Si separator (b) FSFET without a Si separator.

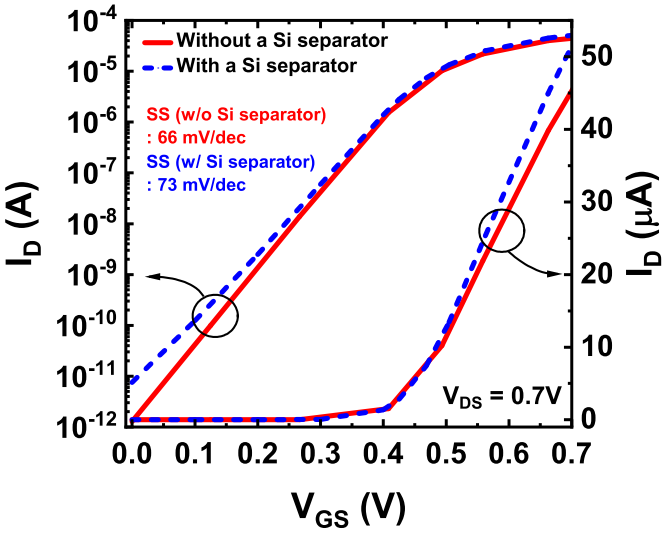

Fig. 5. Input characteristics of the FSFETs from the simulation without considering the density gradient equation at V_{DS} = 0.7 V.

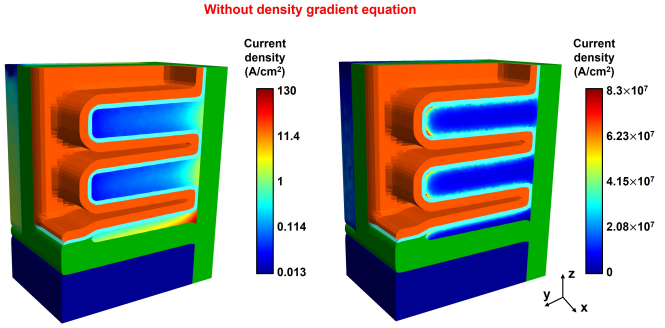

Fig. 6. Current density profiles of the FSFETs with a Si separator at V_{DS} = 0.7 V and V_{GS} = 0 V (left), V_{DS} = 0.7 V and V_{GS} = 1 V (right).

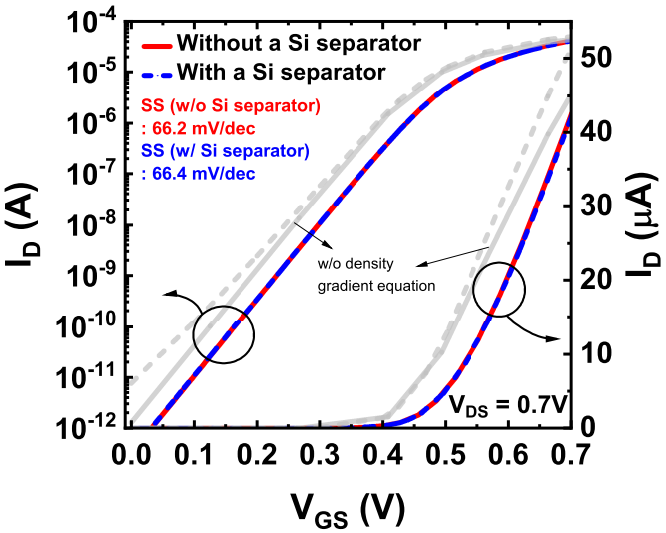

Fig. 7. Input characteristics of the FSFETs from the simulation considering the density gradient equation at V_{DS} = 0.7 V. Gray lines represent the simulation results without the density-gradient equation, already shown in Fig. 5.

Figs. 4(a) and 4(b), respectively. In the device simulation, the drift-diffusion simulation is conducted by considering the high field saturation, the inversion layer mobility model, and the SRH recombination model. By comparing the simulation results with and without the density gradient equation, the impact of the quantum confinement effect is investigated.

First, the input characteristics of two devices at V_{DS} of 0.7 V are investigated from the simulation without considering the density gradient equation. In the simulation without the density gradient equation, the off and on currents are increased by adding the Si separator and the sub-threshold swing (SS) is also increased, as shown in Fig. 5. It is because the added Si separator has non-negligible current density at the off and on states, as shown in Fig. 6.

However, when the density gradient equation is employed, the simulated input curves with and without the Si separator becomes almost indistinguishable, as shown in Fig. 7. The quantities such as the SS, the off and on currents are also identical. It is because when the density gradient equation is considered, the added Si separator has negligible current density at the off and on states, as shown in Figs. 8 and 9. In the thin Si separator whose thickness is 2 nm, the calculated quantum potential is very high. As a result, the carrier density in the Si separator becomes much lower and the current density is negligible. Since the simulation result is significantly affected by the presence or absence of the density gradient equation, the consideration of the quantum confinement effect is essential to accurately assess the effect of the Si separator. The insertion of a thin Si separator to improve the etch profile of the device does not degrade the electrical performance of the device. The device parameters and performances are summarized in Table I.

IV. Conclusions

In conclusion, the effect of Si separator on the FSFET with the BDI has been investigated by using the in-house TCAD process emulator and device simulator. In the process emulation, it has been shown that the geometrical profile of device can be improved by adding a Si separator. It has been also shown that the added Si separator does not degrade the

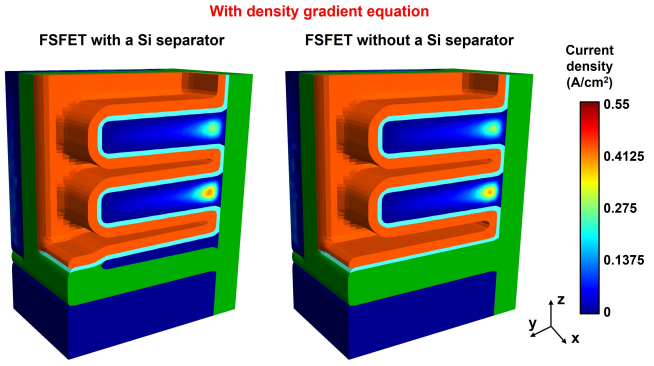

Fig. 8. Current density profiles of the FSFETs at V_{DS} = 0.7 V and V_{GS} = 0 V.

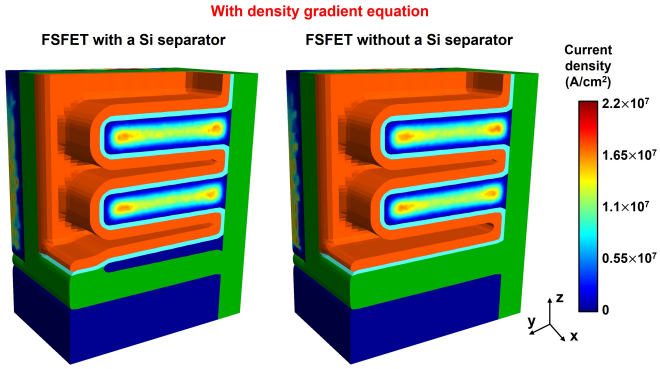

Fig. 9. Current density profiles of the FSFETs at V_{DS} = 0.7 V and V_{GS} = 0.7 V.

	w/ Si separator	w/o Si separator
L_G (nm)	18	18
L_{SD} (nm)	30	30
CPP (nm)	90	90
$W_{channel}$ (nm)	23	23
$T_{channel}$ (nm)	5	5
$T_{separator}$ (nm)	2	N/A
I_{ON} (μA)	42.3	42.6
I_{OFF} (pA)	0.337	0.328
SS (mV/dec)	66.4	66.2

TABLE I
SUMMARY OF DEVICE PARAMETERS AND CHARACTERISTICS. I_{ON} (V_{GS} = 0.7 V) AND I_{OFF} (V_{GS} = 0 V) ARE CALCULATED AT V_{DS} = 0.7 V.

electrical characteristics of the FSFET in the device simulation. It is expected that a further improved FSFET design can be proposed with help of the implemented TCAD framework.

V. Acknowledgement

This research was supported by the National Research Foundation of Korea (NRF) grant funded by the Korea government (NRF-2020M3H4A3081800 and NRF-2023R1A2C2007417).

References

[1] S. B. Samavedam, J. Ryckaert, E. Beyne, K. Ronse, N. Horiguchi, Z. Tokei, I. Radu, M. G. Bardon, M. H. Na, A. Spessot, and S. Biesemans, "Future logic scaling: towards atomic channels and deconstructed chips," in 2020 International Electron Device Meeting, pp. 1–1, December 2020.

[2] P. Weckx, J. Ryckaert, E.Dentoni Litta, D. Yakimets, P. Matagne, P. Schuddinck, D. Jang, B. Chehab, R. Baert, M. Gupta, Y. Oniki, L.-A. Ragnarsson, N. Horiguchi, A. Spessot, and D. Verkest, "Novel forksheet device architecture as ultimate logic scaling device towards 2nm," in 2019 International Electron Device Meeting, pp. 36.5.1–36.5.4, December 2020.

[3] H. Mertens, R. Ritzenthaler, Y. Oniki, B. Briggs, B.T. Chan, A. Hikavyy, T. Hopf, G. Mannaert, Z. Tao, F. Sebaai, A. Peter, K. Vandersmissen, E. Dupuy, E. Rosseel, D. Batuk, J. Geypen, G. T. Martinez, D. Abigail, E. Grieten, K. Dehave, J. Mitard, S. Subramanian, L. A. Ragnarsson, P. Weckx, D. Jang, B. Chehab, G. Hellings, J. Ryckaert, E. Dentoni Litta, and N. Horiguchi, "Forksheet FETs for advanced CMOS scaling: forksheet-nanosheet co-integration and dual work function metal gates at 17nm N-P space," in 2021 Symposium on VLSI Technology, pp.1–2, June 2021.

[4] H. Mertens, R. Ritzenthaler, Y. Oniki, P. Puttarame Gowda, G. Mannaert, F. Sebaai, A. Hikavyy, E. Rosseel, E. Dupuy, A. Peter, K. Vandersmissen, D. Radisic, B. Briggs, D. Batuk, J. Geypen, G. Martinez-Alanis, F. Seidel, O. Richard, B.T. Chan, J. Mitard, E. Dentoni Litta, and N. Horiguchi, "Forksheet FETs with bottom dielectric isolation, self-aligned gate cut, and isolation between adjacent source-drain structures ," in 2022 International Electron Device Meeting, pp. 23.1.1–23.1.4, December 2022.

[5] O. Ertl and S. Selberherr, "A fast level set framework for large three-dimensional topography simulations," Comput. Phys. Commun., pp. 1242–1250, February 2009.

[6] T. S. Newman and H. Yi, "A survey of the marching cubes algorithm," Comput. Graph, pp. 854–879, October 2006.

[7] S.-M. Hong and J. H . Jang, "Transient simulation of semiconductor devices using a deterministic Boltzmann equation solver," IEEE J. Elect. Dev. Soc., 6, pp. 156–163, December 2017.

[8] S. Hang, "TetGen, a Delaunay-based quality tetrahedral mesh generator," ACM Trans. Math. Softw., 41(2), 11, 2015.