How the Flat Field Transistor (FFT) can enable the continuation of DRAM scaling

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Abstract— In this paper we present a detailed simulation study of the the advantages of the Flat Field Transistor (FFT) developed by Semiwise as a solution to the DRAM scaling problems. The FFT meets all present and future requirements of the DRAM sense amplifiers and peripheries. The improvements cover all related requirements including low variability, low noise, low leakage, high performance, and high reliability. The FFT performance is highlighted in comparison with typical 20 nm bulk CMOS technology transistors. Results illustrating the transistor performance improvement are presented, and the corresponding improvement in the circuit performance is illustrated using sense amplifier.

***Keywords*: Performance, DRAM, variability, noise, sense amplifier, leakage current, Sense Amplifier.**

I. MOTIVATION

Although the DRAM cell transistors have undergone a dramatic revolution from recess gate to saddle FinFET, for cost reasons, the DRAM sense amplifiers and periphery continue to be manufactured using conventional bulk MOSFETs [1]. The scaling of the DRAM (Fig. 1) is particularly challenging in respect of the performance and the area of the sense amplifier (SA) as key elements of the DRAM chips [2]. With the relentless scaling of the DRAM the margins of the sense amplifier (SA) dramatically decrease. The statistical variability (mismatch) of the bulk MOSFETs [3] is the main factor eroding the SA margins. The addition of offset compensation circuits to the SA, adopted by most of the DRAM manufacturers, increases the SA related 'dark' area on the DRAM chips (Fig. 2), further eroding the DRAM scaling. The recently published recess gate (Fig. 3a) transistors are designed to tackle the DRAM SA statistical variability problem, but comes at increased manufacturing complexity and costs, and reduced performance [4].

The novel FFT (Fig. 3b) devices developed by Semiwise [5] offers a solution to the DRAM scaling problems by improving dramatically the margins of the DRAM sense amplifiers in terms of variability, noise, leakage, and reliability. In this paper we illustrate how the FFT significantly improves the desirable performance metrics of the DRAM periphery.

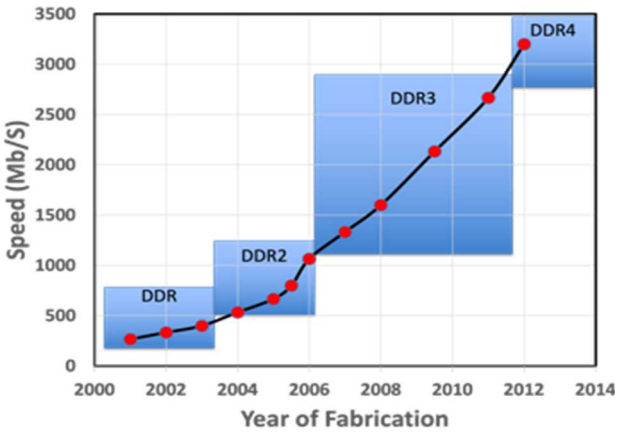


Fig. 1: Evolution of DRAM product in the past two decades.

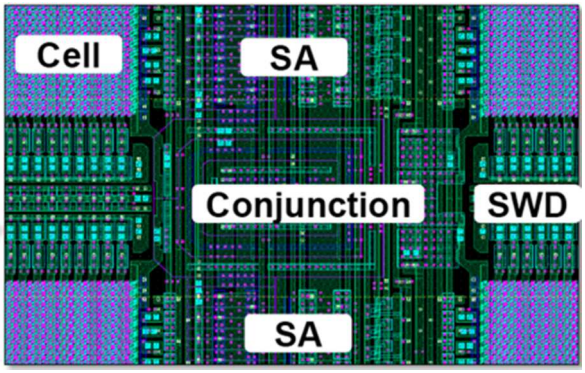


Fig. 2: Sense amplifier and periphery circuit in modern DRAM chip.

The concept of the *n*-channel FFT is illustrated in Fig. 3-4 in comparison with an equivalent 22 nm Bulk CMOS MOSFET. The two transistors have 25 nm physical channel length and 0.85 nm equivalent oxide thickness. In this paper we consider high-k/metal gate stack. Fig. 4d shows the potential distribution in FFT, and the extension of depletion layer with the corresponding field lines. The simulations are carried out with the drift-diffusion (DD) module of the Synopsys 'atomistic' device simulator GARAND [6] calibrated to EMC simulations. Due to purely geometrical effects the drain potential in the FFT controls a much smaller fraction of the depletion layer charge under the channel. This helps the FFT at equivalent subthershold slope (SS) and drain induced barrier lowering (DIBL) to tolerates low channel doping of 5×10^{17}cm-3 compared to channel doping of ~1×10^{19} cm-3 in bulk.

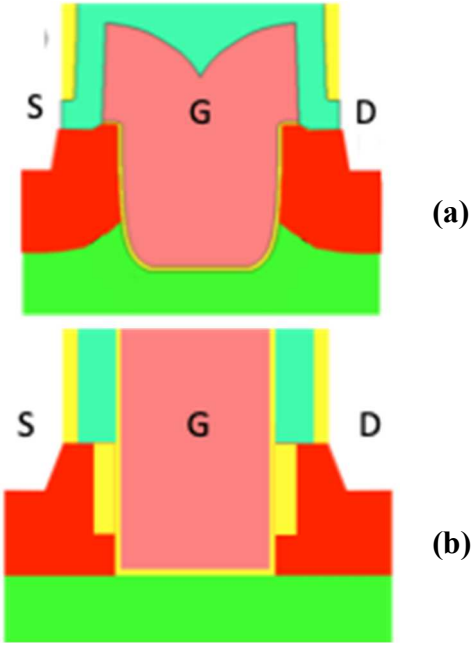
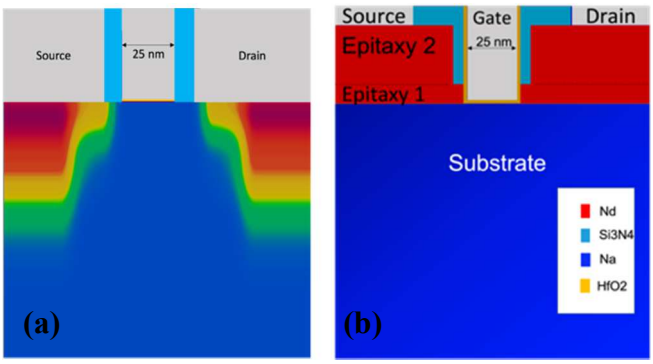


Fig. 3: Structure of (a) recess gate transistor [3], and (b) improved FFT structure.



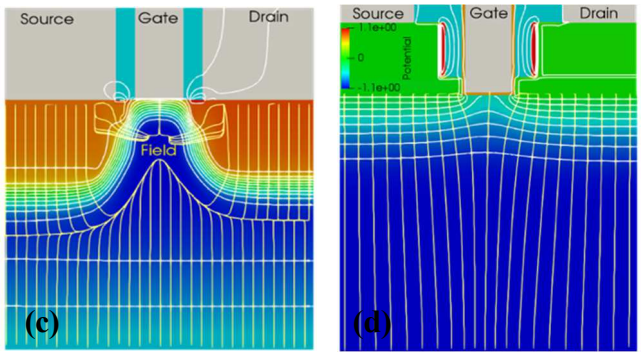


Fig. 4 Electron distribution profile in conventional 22nm Bulk device (a), doping profile in optimized FFT (b). Potential distribution in conventional 22nm Bulk device (c), and FFT (d) under operational condition.

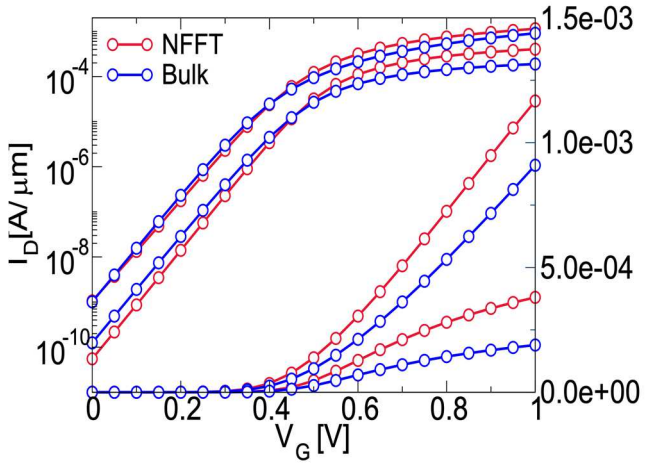


Fig.5: Comparison of Id-Vg between bulk and FFT *n*-type transistors

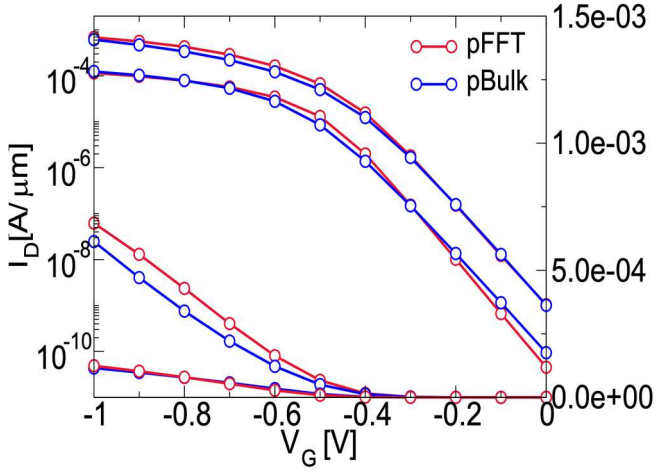


Fig. 6: Comparison of Id-Vg between bulk and FFT *p*-type transistors

II. Methodology, Results and Discussions

Transfer characteristics of *n*- and *p*-type bulk and FFT transistors are shown in Fig. 5-6 showing significant performance advantage. Statistical simulations including Random Discrete Dopants (*RDD*), Metal Gate Granularity (*MGG*), and Line Edge Roughness (*LER*) [3] were caried out to compare FFT and bulk MOSFET statistical variability. The threshold voltage (V_T) variability due to each of the variability sources acting alone and all together is shown in Fig. 7. There is almost 50% reduced variability in the case of FFT compared to the Bulk device. Reliability is also a major concern, and FFT has an advantage too as shown in Fig. 8, which shows the dispersion of ΔV_T is larger for bulk compared to the FFT. For some extreme devices the ΔV_T of bulk reach more than 50 mV, while it's less than 20mV in the case of FFT.

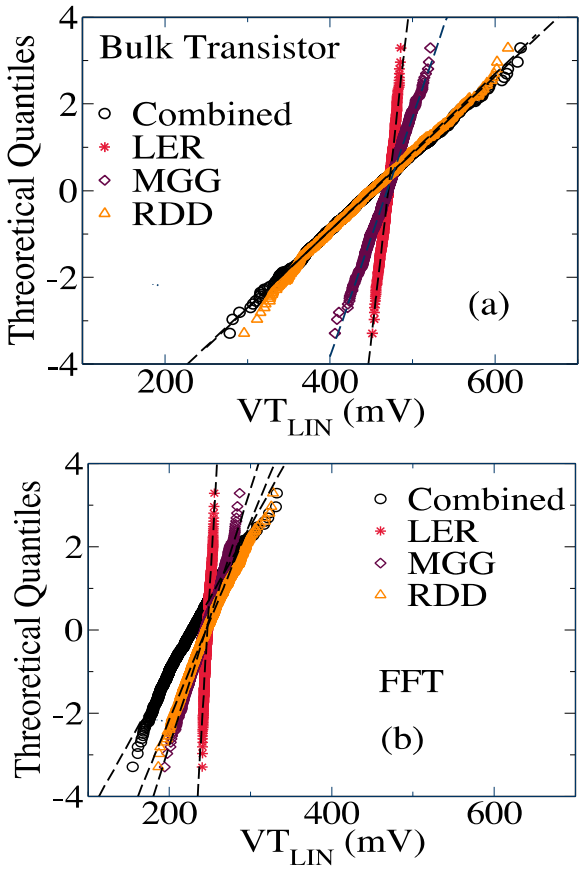


Fig. 7 Q-Q plot of VT distribution of Bulk and FFT transistor.

To illustrate the impact of the statistical variability on the DRAM design, first we performed SPICE parameter extraction for the *n*- and *p*-type FFT and bulk devices. Then we simulated a *sense-amplifier* circuit (for DRAM application) and evaluated the variability in the offset voltage using Monte-Carlo runs. Fig. 9 shows the typical sense-amplifier circuit schematic. As shown in Fig. 10 inset, at 22nm bulk CMOS, the FFT delivers more than 50% reduction in the SA offset variability. This can be translated to more than 4-time reduction in the FFT SA area compared to the bulk MOSFET SA at identical offset variability distributions.

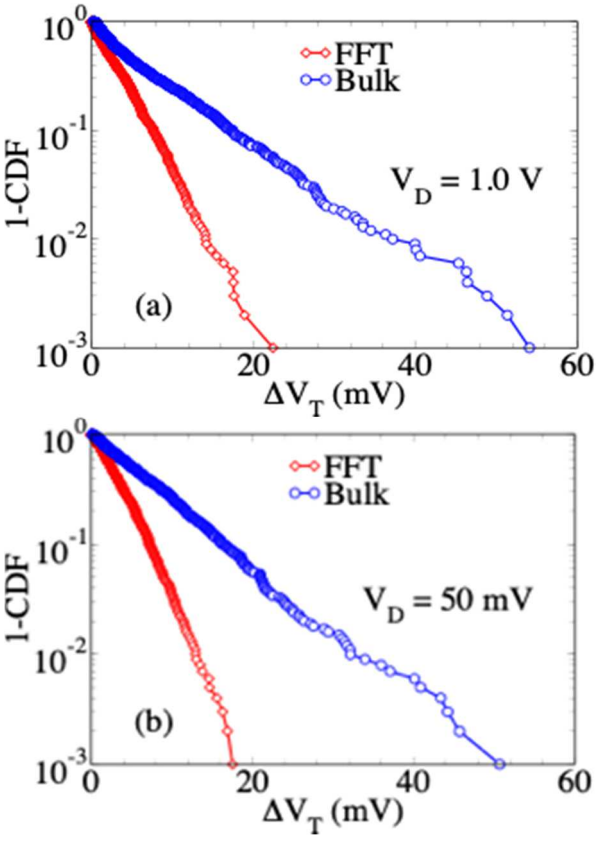


Fig 8: RTS amplitudes distribution at (a) high and (b) low drain bias conditions for both bulk and FFT devices.

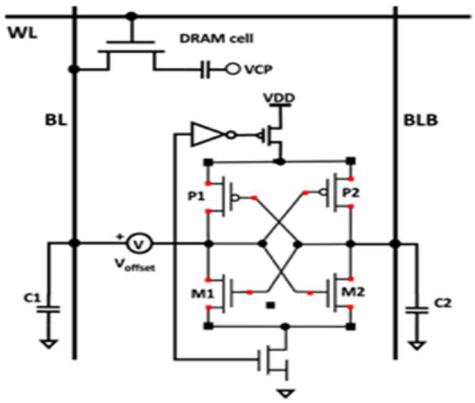


Fig. 9: Typical DRAM sense amplifier

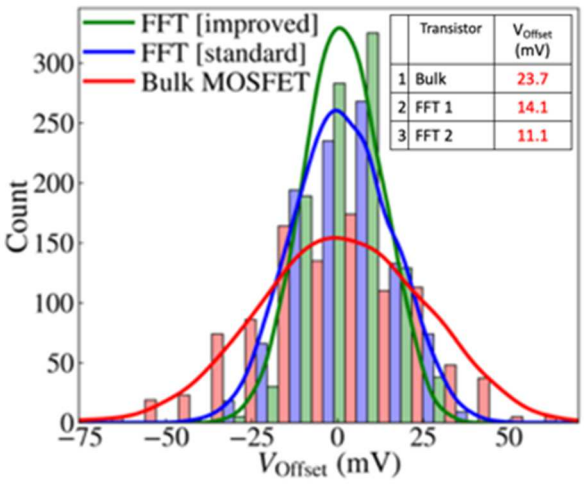


Fig. 10: Variation of Offset voltage in bulk and FFT

III. Conclusion

In this paper we have demonstrated the benefits of using the Flat Field Transistor in DRAM sense amplifier. The use of the FFT substantially improves all requirements for the DRAM sense amplifiers and periphery as illustrated in tables 1-3. FFT's advantage can be sustained down to 22nm bulk CMOS offering long-term DRAM scaling solution. amplifier. The use of the FFT substantially improves all requirements for the DRAM sense amplifiers and periphery as illustrated in tables 1-3. FFT's advantage can be sustained down to 22nm bulk CMOS offering long-term DRAM scaling solution.

Table 1: FFTs is better than the corresponding bulk MOSFETS in respect of all DRAM Sense Amp (SA) and Periphery (P) requirements

	Requierments	Scaled Bulk MOSFET	Scaled FFT
SA	Lower σV_T	No	Yes
SA	Lower Noise	No	Yes
SA, P	Lower leakage	No	Yes
SA, P	High reliability	No	Yes
P	High performance	No	Yes
SA, P	Low noise	No	Yes

Table 2: FFT variability is reduced by 50% compared to the reference Bulk transistors.

Type	VDD (V)	FFT			Bulk		
		σV_T	$C1$	Av	σV_T	$C1$	Av
n	0.05	27	0.68	0.95	57	1.43	2.02
	1	33	0.83	1.17	64	1.6	2.26
p	0.05	38	0.95	1.34	65	1.63	2.3
	1	43	1.08	1.52	70	1.75	2.47

Table 3: The performance improvement of FFT with respect to bulk transistor

Type	VDD (V)	FFT I_{on} $(mA/\mu m)$	Bulk I_{on} $(mA/\mu m)$	Improvement (%)
n	0.05	0.36	0.201	79
	1	1.5	1.2	25
p	0.05	0.207	0.129	60
	1	1.255	0.99	26
n	I_{eff} (n)	0.904	0.67	34
p	I_{eff} (p)	0.697	0.496	40

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