Description of Gate-to-Channel Tunneling Leakage Mechanism in a 2D Monte Carlo Simulator

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***Abstract*—Quantum tunneling effects have become a critical issue in the behavior of ultrascaled nanoelectronic devices. One of such overriding phenomena is the leakage current flowing across the gate insulator since it may lead to increased power dissipation, reduced reliability and limited performance. In this work, we present the implementation of the gate-to-channel leakage mechanism in a 2D Multi-Subband Ensemble Monte Carlo (MS-EMC) tool by means of a novel module that accounts for both direct and trap assisted tunneling across the insulator. We apply our code to FDSOI and FinFET devices and elucidate the effects of this deleterious leakage current.**

***Index Terms*—gate leakage mechanism, direct oxide tunneling, trap assisted tunneling, MS-EMC, FDSOI, FinFET**

I. Introduction

The utilization of Monte Carlo (MC) techniques for simulating the behavior of nanoelectronic devices benefits from the statistical power of stochastic processes. Traditionally, MC simulators were essentially semi-classical tools [1], [2]. However, the inclusion of quantum tunneling has become mandatory since the reduction in size of transistors has made tunneling phenomena alter their expected performance [3]. In particular, the leakage tunneling across the gate insulator may induce an increase in static power consumption or cause reliability issues due to premature failures of the devices [4]. Moreover, the existence of this tunneling can lead to variations in the electrical characteristics, which eventually reduce the operational speed of the devices and increase their noise. This effect is known as the gate leakage mechanism (GLM) and involves the tunneling to/from the channel substrate from/to the metal gate. Furthermore, not only does it account for the direct tunneling (DT) through the gate oxide, but GLM is also taking into consideration the events related to the existence of defect states in the oxide region. In this last case, since the tunneling events are conditioned by the position of the traps (spatially and energetically speaking), this kind of phenomena are commonly referred as trap assisted tunneling (TAT).

The novelty of this work lies in the description of these tunneling phenomena consisting in the injection of carriers from the gate to the channel in nanoelectronic devices. This has been achieved by the development of a new module incorporated into a 2D Multi-Subband Ensemble MC (MS-EMC) simulator, and which has been applied to compare the performance of Fully-Depleted Silicon-On-Insulator (FDSOI) and FinFET devices.

II. Methodology

The starting point of the simulation frame is a MS-EMC code whose main blocks are depicted in black boxes in the flowchart of Fig. 1. It has already shown its effectiveness in modeling electron transport, scattering, and other types of tunneling [5] by means of an efficient computational scheme allowing the description of large numbers of electrons in a relatively moderate period of time.

The new gate-to-channel tunneling implementation herein presented completes the whole framework of the GLM simulation capabilities so far developed for the MS-EMC tool (the modules corresponding to the tunneling contributions of carriers coming from the channel had already been developed in the past [6]). Therefore, in this work, we also account

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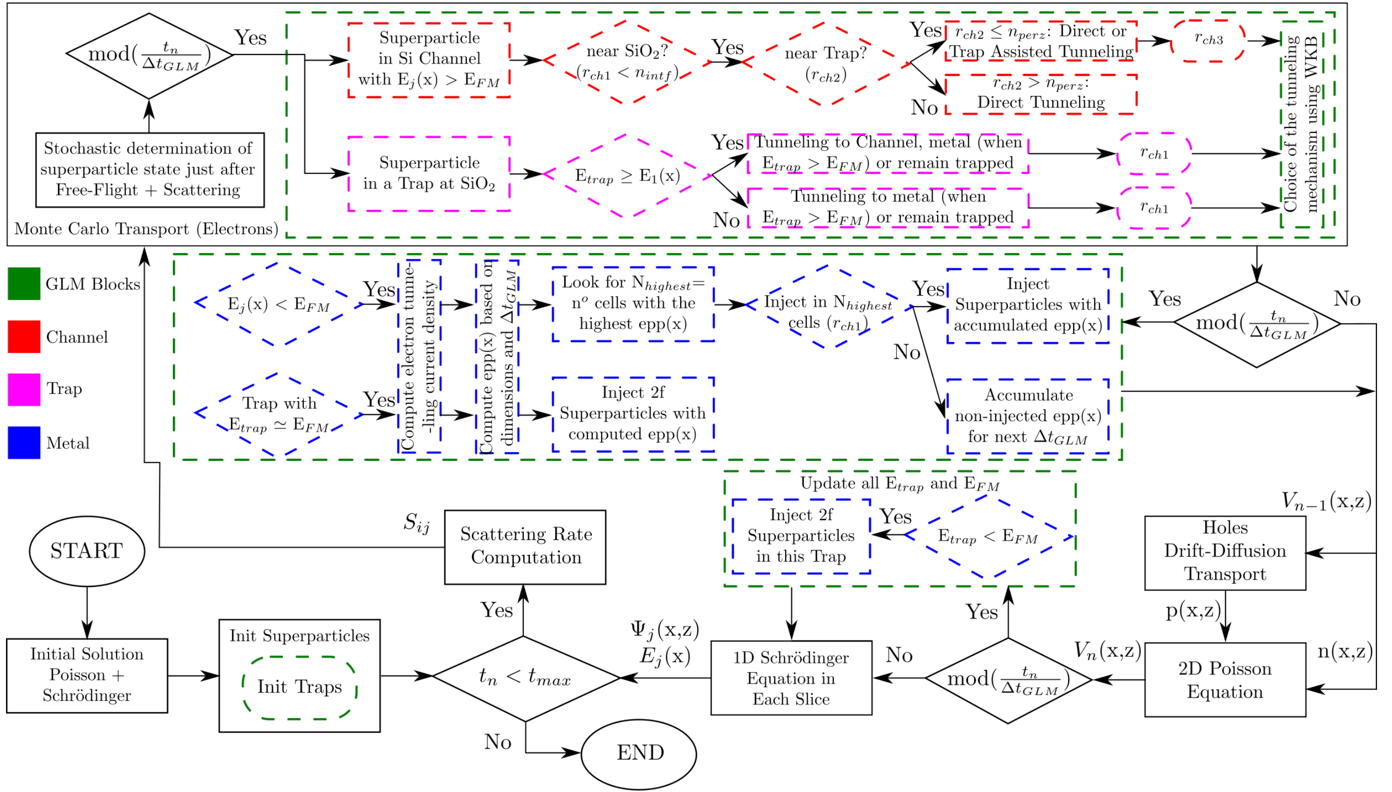

Fig. 1. Flowchart of the MS-EMC simulator along with the additional blocks of the GLM implemented in this work. x is the transport direction, z is the confinement direction, n(x,z) and p(x,z) are the electron and hole concentrations, respectively, V(x,z) is the potential profile, E_j(x) is the energy of the subband j, Ψ_j(x,z) are the subband eigenfunctions, S_{ij} are the scattering rates, the subscript n stands for the iteration number, and Δt_{GLM} is the time step for GLM calculation. In the GLM blocks: E$_{trap}$ is the trap energy, E$_{FM}$ is the Fermi level in the metal, f is the trap vacancy coefficient (0, 0.5, or 1), $r_{ch1/2/3}$ are uniformly distributed random numbers, n_{intf} is the percentage of particles near the interface between the substrate and the oxide, and n_{perz} is the percentage of charge that can be located near a trap taking into account the 3D direction.

for the new particles that need to be injected in the channel from the gate [7]. It is worth mentioning that the whole GLM implementation developed in the simulator takes into account the description of both DT and TAT events regardless of the direction of the tunnel. All these considerations have been diagrammatically depicted in Fig. 2, which illustrates all the tunneling mechanisms that can now be described by the MS-EMC simulator. We observe that, apart from carriers coming from the channel (that might either tunnel to the gate or to a trap), the novel tunneling events are those arising from the metal. Notice that the inclusion of this new type of tunneling also affects the tunneling processes from carriers trapped in the oxide, since the origin of these carriers might have been now either the gate or the channel. Thus, since TAT is simultaneously affected by carriers coming from both sides of the barrier, the development and addition of the new GLM module implies a more accurate description of the actual behavior of the net leakage tunneling current across the gate insulator.

The global setup of a simulation run has been represented with detail in Fig. 1. The parts of the new GLM module from metal are depicted in blue boxes and, as for the rest of the GLM events, they are only executed with larger time intervals (Δt_{GLM}) than the MC time step (t_n) due to the their

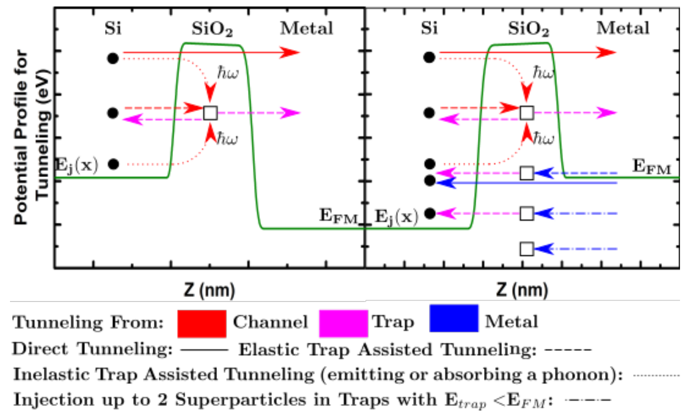

Fig. 2. Schematic depiction of a MOS structure where the gate leakage mechanisms accounted for by the MS-EMC simulator are sketched for $E_{FM} < E_j(x)$ (left) and $E_{FM} > E_j(x)$ (right).

low occurrence. The ensemble of the simulation scheme has been rearranged to accommodate the mutual influence between the different types of GLM caused by the presence of TAT, as already discussed. Focusing on the new tunneling events coming from the gate when $E_{FM} > E_j(x)$, Fig. 2(b) shows that they can occur: (i) to a trap when $E_{FM} \geq E_{trap}$) (notice that different trap energies are marked as small black squares

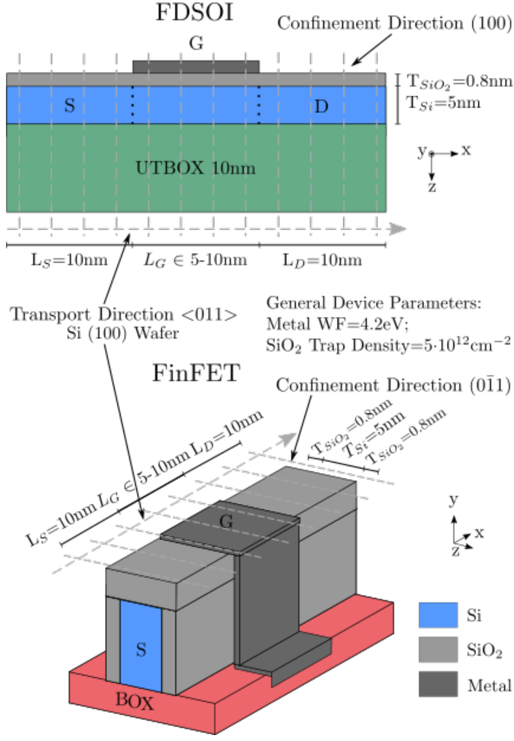

Fig. 3. Schematic Si FDSOI and FinFET devices. The confinement direction for these devices on standard wafers [100] changes from (100) for FDSOI to (0$\bar{1}$1) for FinFET. The transport direction $< 011 >$ is the same for both.

in Fig. 2(b)); or (ii) to the channel when E_{FM} lies above the energy level of the j subband ($E_j(x)$) of the semiconductor. For the case with $E_{FM} > E_{trap}$, carriers are automatically injected if the trap is available at each Δt_{GLM} respecting the Pauli exclusion principle (i.e., if the trap were not full at that moment). As for the situation when $E_{FM} \approx E_{trap}$, as well as for the injection to the semiconductor, carrier injection is estimated from the calculation of the tunneling current density [7] (provided that in the case of the trap, it is not full). On the other hand, DT injection to the channel requires the additional estimation of the particular location(s) along the transport direction where it will take place. That will be calculated according to a random procedure based on a probability distribution estimated from the DT current density computation at each grid position along the gate.

III. Results

Our code has been tested for the FDSOI and FinFET devices sketched in Fig.3. Recall that the confinement direction of these devices on standard wafers changes from (100) for the planar FDSOI to (0$\bar{1}$1) for FinFET, whereas the transport direction remains constant <011>. In general, this difference in the confinement orientation modifies the electron distribution and the carrier confinement effective mass (m_z^*). Since in this study the gate length ranges from L_G=5 nm to L_G=10 nm, the S/D tunneling module included in the MS-EMC tool has been activated too due to the known degradation of the subthreshold behavior in sub-10 nm nodes [5], [8]. The rest of the parameters remains constant: the channel thickness T_{Si}=5 nm, the SiO_2 gate oxide of 0.8 nm, and the gate work function of 4.2 eV. For the FDSOI device, a Back-Plane with a UTBOX=10 nm, Back-Bias polarization of V_{BB}=0 V, and Back-Plane work function of 5.17 eV have been chosen. As far as TAT is concerned, the number of traps is deterministically calculated according to the oxide dimensions and the trap density, which, in turn, has been chosen to be fixed at $5\cdot10^{12}$ cm^{-2} for the SiO_2. For comparison purposes, the spatial location of the traps as well as their energies have been set to be identical in both devices.

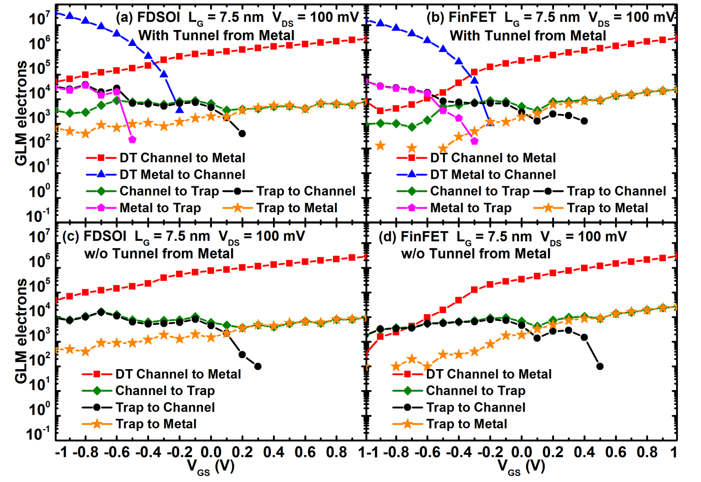

Fig. 4. Average number of injected electrons per MC time step (t_n=1 fs) due to GLM including both direct and trap assisted tunneling from the metal for FDSOI (left plots) and FinFET (right plots) with L_G=7.5 nm and V_{DS}=100 mV.

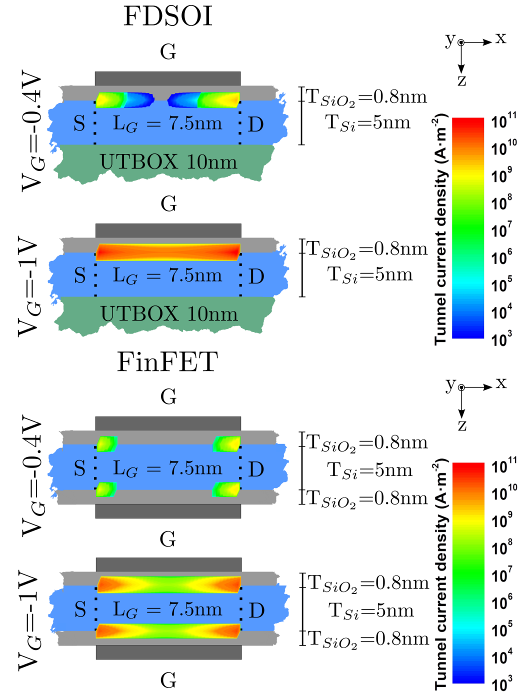

Fig. 5. Tunneling current density from the metal in A·m^{-2} for FDSOI and FinFET devices with L_G=7.5 nm, V_{DS}=100 mV. We have taken V_{GS}=−0.4 V and V_{GS}=−1 V for each structure.

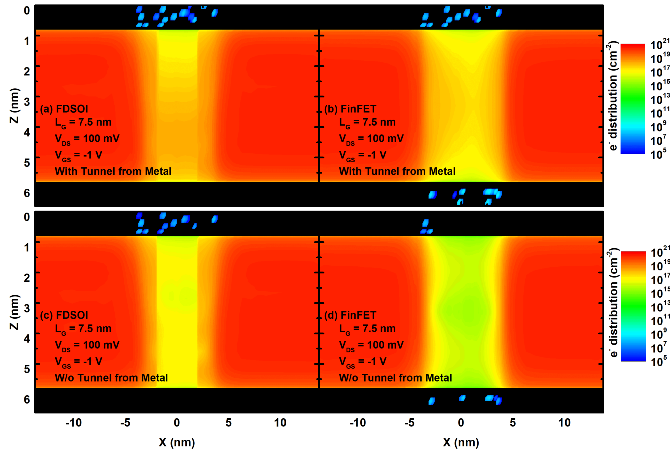

Fig. 6. Electron distribution in cm^{-2} along the transport (X) and confinement (Z) directions when GLM from the gate is enabled (a-b) and disabled (c-d) for FDSOI and FinFET devices with L$_G$=7.5 nm, V$_{DS}$=100 mV, and V$_{GS}$=-1 V.

Once all leakage mechanisms are taken into account, Fig. 4 illustrates their relative importance in terms of the number of electrons affected by them for a gate voltage ramping from negative to positive voltages. The importance of the electrons coming from the metal is apparent taking into account the injection into the channel by DT. This type of leakage proves to be even more critical than that corresponding to the electrons escaping from the channel. The contribution of the GLM assisted by traps remains clearly below the DT contributions for all the considered gate polarizations as expected. Since the subbands arising from the quantization of the conduction band inside the channel along the z direction are not uniform in energy in the transport direction, the tunneling current density is not homogeneous through the gate oxide (Fig. 5) for both devices and for different V$_{GS}$ values. It can be seen how the main leakage contributions are always located at the sides of the gate since the semiconductor subbands bend down as we move away from the central region beneath the insulator.

The logical effect of the charge injection from the metal by means of the new simulation module is to modify the charge distribution inside the channel, as well as the electron concentration within the traps located at the gate oxides (Fig. 6). The extreme case with V$_{GS}$=-1 V shows that the GLM coming from the metal increases the peaks of the electron concentration inside the channel by at least one order of magnitude for both the FDSOI and the FinFET. Finally, the total net leakage current across the channel/insulator interface is displayed in Fig. 7 for different gate lengths. Each curve corresponds to the result of adding up the currents associated to the GLM mechanisms of Fig. 4 that involve carriers going to (or coming from) the channel, assigning each one of them a sign depending on its tunneling direction. Namely, negative terms correspond to electrons injected to the channel (DT from metal, and trap-to-channel events), whereas positive terms are those related to electrons escaping from the the channel (DT from channel, and channel-to-trap events).

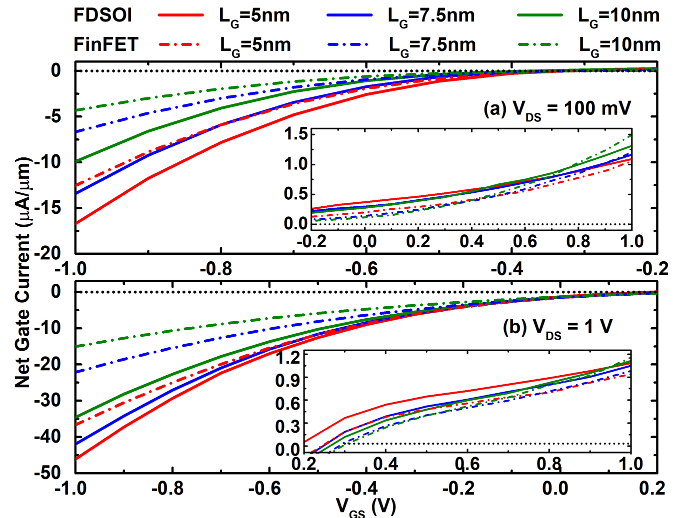

Fig. 7. Net leakage current as a function of V$_{GS}$. (a) V$_{DS}$=100 mV, (b)V$_{DS}$=1 V. The prevailing type of tunneling (from channel/to channel) determines in each case the resulting direction of the current.

IV. Conclusions

We have presented the implementation of a simulation module that completes the description of GLM modeling in a MS-EMC tool. This module accounts for the tunneling current contributions coming from the gate electrode either caused by direct injection into the channel, or assisted by the traps located in the gate insulator. We have shown results demonstrating that for $E_{FM} > E_j(x)$ the importance of this type of tunneling should not be neglected in order to achieve an accurate description of the performance degradation of ultrascaled FDSOI and FinFET devices.

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