# Monte-Carlo Based Simulation Method for Ferroelectric Memory Devices Including Polarization Switching and Trap Behaviors

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***Abstract*— Charge trapping is widely known to affect the characteristics of ferroelectric-based memory devices, especially ferroelectric field effect transistors (FeFETs). We have developed a Kinetic Monte Carlo based simulation platform for ferroelectric memory devices, which allows for the interplay between charge trapping and polarization switching. The role of interfacial layer traps in FeFET is investigated, which is weakly coupled to polarization switching and mainly contributes to the read-after-write delay and the gate leakage.**

***Keywords*— FeFET, trap, Monte Carlo Simulation**

## I. Introduction

Charge trapping is widely known to affect the characteristics of ferroelectric-based memory devices, especially ferroelectric field effect transistors (FeFETs) [1-6]. Device simulation allows us to explore the potential coupling between the polarization switching (PS) and charge trapping (CT), which is still under intensive research. Some previous works consider the quasi-static or half-static coupling between them [7, 8], while others includes their dynamic interplay. The latter are mostly based on compact models [9-12] and a few are based on Technology Computer Aided Design (TCAD) simulations [13]. In this work, we propose a Kinetic Monte Carlo (KMC) based simulation method which allows for the fully dynamic interplay between PS and CT.

## II. Simulation Framework

Fig. 1 shows our KMC based simulation platform for ferroelectric memory devices, which couples the polarization switching and the trap (de-)trapping via the device electrostatics. The core of the simulator is composed of three modules, each of which solves one of the key variables: the temporal and spatial distribution of ①polarization charges $P_{FE}(\boldsymbol{r},t)$, ②trapped charges $Q_t(\boldsymbol{r},t)$ ③electrostatic potential $\varphi(\boldsymbol{r},t)$ (or equivalently, the electric field $E(\boldsymbol{r},t)$). Based on the evolution of these key variables, we can analyze the performance, reliability and variability of the ferroelectric devices. The device electrostatics module could be any electrical device simulator that solves the coupled Poisson equation and carrier transports in semiconductor.

Both the PS and CT processes are time-dependent and stochastic. The probabilities of these processes are listed in TABLE I. During a short time interval $\Delta t$, the switching probability of a ferroelectric domain $p_{sw}(\Delta t)$ is described by the nucleation-limited switching (NLS) model [14] as shown by (1-3). The probability of electron capture $p_c(\Delta t)$ and emission $p_e(\Delta t)$ by the trap is determined by (4-10) based on the two-state non-radiative multi-phonon (NMP) model [15]. CT between the semiconductor channel and gate are both considered. Given the probabilities of the PS and CT events, we can simulate these events using the Monte Carlo method.

Fig. 2 shows the flow chart of our simulator. The three key modules are placed in the nested loops. The outer loop discretizes the input bias and the inner loop controls the time step $\Delta t$ for fields updating. As the PS can be characterized by the switching time constant $\tau_{sw}$, the CT is also characterized by its own time constants: the capture time constant $\tau_c$ and

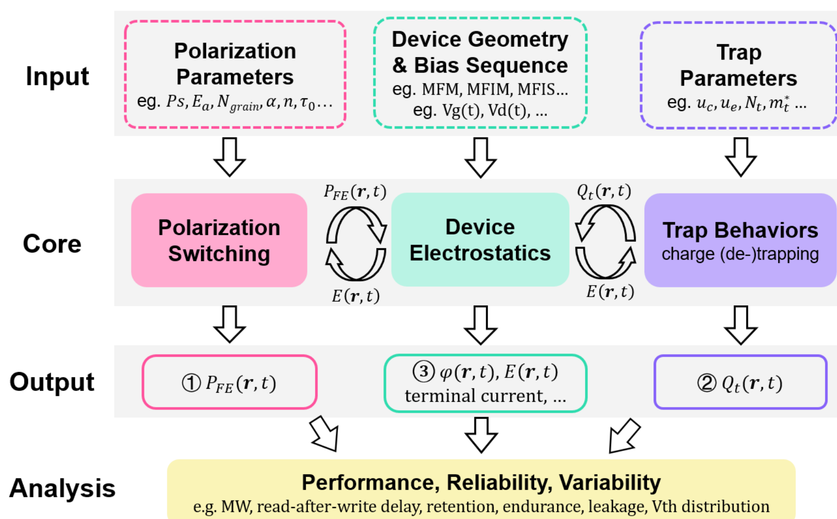


Fig. 1 Monte-Carlo based simulator for ferroelectric memory devices.

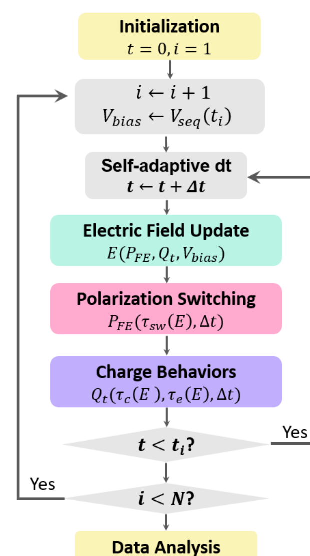


Fig. 2 Simulation flowchart.

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TABLE I. PROBABILITIES FOR PS AND CT

| Polarization Switching (PS) | |
|---|---|
| $p_{sw}(\Delta t) = 1 - \exp(-[h(t+\Delta t)]^n + [h(t)]^n)$ | (1) |
| $h(t+\Delta t) = h(t) + \dfrac{\Delta t}{\tau_{sw}}$ | (2) |
| $\tau_{sw}(E) = \tau_0 \exp[(E_a/\lvert E\rvert)^\alpha]$ | (3) |
| **Trap Behaviors (CT)** | |
| $p_c(\Delta t) = \Delta t/\tau_c$ | (4) |
| $p_e(\Delta t) = \Delta t/\tau_e$ | (5) |
| $\dfrac{1}{\tau_c} = \delta_{n,c} \cdot v_n \cdot n \cdot \exp\left(-\dfrac{\mathcal{E}_c}{k_B T}\right)$ | (6) |
| $\dfrac{1}{\tau_e} = \delta_{n,e} \cdot v_n \cdot N_c \cdot \exp\left(-\dfrac{\mathcal{E}_e}{k_B T}\right)$ | (7) |
| $\mathcal{E}_c = u_{c0} + \lambda \cdot \Delta E_{21}$ | (8) |
| $\mathcal{E}_e = u_{e0} - (1-\lambda) \cdot \Delta E_{21}$ | (9) |
| $\delta_{n,g} = \delta_n \cdot \exp(-\gamma(L - z_t))$ | (10) |

$\alpha, n$ are both unitless fitting parameter for NLS model.

$\tau_0$: switching time constants when the domain electric field $E$ is infinite.

$v_n$: electron thermal velocity.

$\delta_n$: capture cross-section of electrons that includes the elastic WKB tunneling probability. The electron tunneling through the thick FE layer is treated as an inelastic process where an exponential decay factor is also included to account for the energy dissipation in the real space as shown in (10), where $L$ is total thickness of the gate dielectric and $z_t$ is the trap distance from the Si interface. $\gamma = 0.95\text{nm}^{-1}$

$k_B$ is Boltzamn constant and $T$ the lattice temperature.

$\mathcal{E}_c$ and $\mathcal{E}_e$: electron capture and emission barrier, which, for simplicity, is assumes to linearly depend on the potential drop $\Delta E_{21}$ between the trap and Si. In other words, $\tau_e$ and $\tau_c$ are electric-field dependent. $\lambda$ is the barrier tuning factor and $\lambda = 0.7$. $u_{c0}$ and $u_{e0}$ are the capture and emission barrier under zero bias.

$E_a$ for each FE domain, $u_{c0}$ and $u_{e0}$ for each trap, are sampled from Gaussian distribution.

emission time constant $\tau_e$. These time constants and hence the event probabilities are sensitive to the devices electrostatics and span a wide range (more than 10 decades). On the other hand, the change of $Q_t$ and $P_{FE}$ in turn alters the device electrostatics. Therefore, it is critical the update the electric field in time. A self-adaptive scheme for $\Delta t$ is adopted to achieve balance between computation accuracy and efficiency: small $\Delta t$ relative to the event time constants means that few events happen during the $\Delta t$ and a waste of iteration time, whereas large $\Delta t$ might incur numerical oscillation because lots of CT and/or PS events happens during $\Delta t$, resulting in drastic change in $Q_t$ and/or $P_{FE}$.

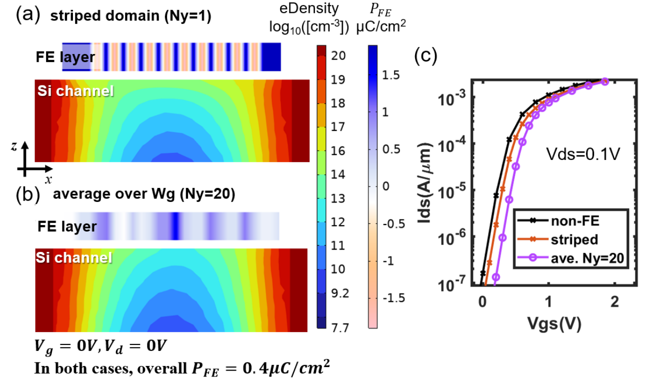


Fig. 4 Electron density distribution in Si channel with different polarization distribution pattern: (a) striped domains; (b) average $P_{FE}$ using the projection scheme in Fig.3(c); and (c) the corresponding Id-Vg curves.

As an example, we investigate the FeFET shown in Fig. 3(b) and simulate the impacts of the traps in IL layer on the FeFET performance. The ferroelectric thin film is assumed to be composed of a single layer of $N_x$ by $N_y$ domains as shown in Fig.3 (a). Each FE domain is either polarized up or down (represented by cyan and magenta cube respectively), with a fixed spontaneous polarization charge $Ps_{FE}$. As for the trap ensemble, each trap is also switched between two charge states, either empty or filled with one single electron, illustrated in Fig. 3(c) as open or filled circle. To enhance the simulation efficiency, the simulation is carried out in 2D, which is valid for large area devices. The trapped charge distribution obtained from 3D KMC CT simulation is projected to the *x-z* plane. Similarly, the polarization charge distribution $P_{FE}(x)$ along the gate length is obtained by averaging over the gate width (*y*-direction). $P_{FE}(x)$ averaging over multiple layers in *y*-direction is also necessary to avoid the non-linear relationship between the polarization charges and the channel conductance as shown in Fig. 4. For the same overall $P_{FE} = 0.4$ μC/cm$^2$, the channel electron density in the striped domain case (Fig. 4(a)) is much higher, resulting in only a slight $V_{th}$ shift compared to the non-FE MOSFET, as shown in Fig. 4(c) while the averaging case (Fig. 4(b)) produces the same $V_{th}$ shift as estimated by the sheet charge density method: $\Delta V_{th} = P_{FE}/C_{FE}$, where the $C_{FE}$ denotes the capacitance of FE layer.

The FeFET is subjected to the gate voltage $V_{gs}$ as shown in Fig. 5(a). It is first initialized with a -5V, 1ms negative square pulse. After 10 s delay, it is programmed with a positive pulse with varying amplitude $V_{pul}$ and width $T_{pul}$. When the programing pulse is removed, the device is relaxed for a period of $T_{relaxation}$ before the $V_{th}$ is measured via $I_d$-$V_g$

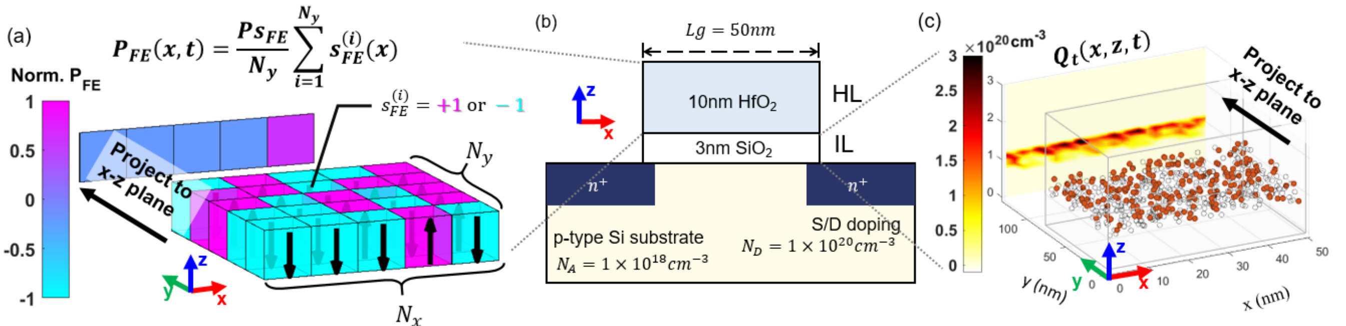


Fig. 3 (a) Simulated FeFET structure. The 2D projection scheme of (b) the trapped charge density and (c) the polarization charge density. Each circle in (b) represent a single trap, while each cube in (c) is a FE domain.

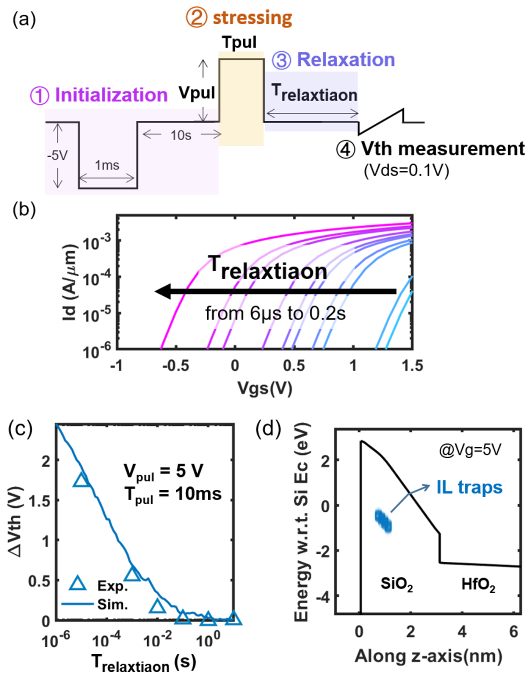


Fig. 5 Calibration of the IL traps parameters. (a) Bias sequence. (b) The simulated Id-Vg curves during relaxation and (c) the ΔVth (w.r.t. Vth at $T_{relaxtion} = 10s$) over time.

curves. As shown in Fig. 5(b), the $I_d$-$V_g$ curves is continuously shifting left due to electron detrapping. The transient change of device $V_{th}$ after the removal of programing pulse, which lasts for about 1s, is referred to as pulse response in this paper.

As shown in Fig. 5(c), the IL trap parameters is calibrated against the (5V, 10ms) pulse response. The $\Delta V_{th}$ here is referenced to the steady-state $V_{th}$ at $T_{relaxation} = 10s$. The fitted trap density $N_{t,IL}$ is $2.5\times10^{13}$ cm$^{-2}$. The fitted capture barriers $u_{c0}$ and emission barriers $u_{e0}$ are $N$(0.75eV, 0.05eV) and $N$(0.4eV, 0.12eV), where $N$(μ, σ) denotes the Gaussian distribution with mean value μ and standard variation σ. Fig. 5(d) sketches the energetic and spatial distribution of the IL traps, which is close to the conduction band edge of Si.

## III. Results And Discussion

Fig. 6 (a-b) shows simulated the pulse response of FeFET with and without the IL traps. The $V_{pul}$ is fixed at 5V and the $T_{pul}$ is varied from 0.1μs to 1ms. For the ideal FeFET with no traps, the $\Delta V_{th}$ increases over time simply as a result of $P_{FE}$ depolarization. In contrast, the $\Delta V_{th}$ of the FeFET with IL traps decreases over time due to electron detrapping. The $\Delta V_{th}$ of the FeFET can be decomposed into PS-induced $\Delta V_{th}^{\mathrm{FE}}$ and CT-induced $\Delta V_{th}^{\mathrm{Trap}}$, as shown in Fig. 6(c) and Fig. 6(d). The depolarization also exists in this case as observed in the experiment [5], but it is shadowed by the electron detrapping. As $T_{pul}$ increases, both polarization and electron trapping are enhanced during the stressing stage (Fig. 5(a)). Subsequently, the $\Delta V_{th}^{\mathrm{FE}}$ and $\Delta V_{th}^{\mathrm{Trap}}$ increases during the relaxation. Nonetheless, for $T_{pul}$ longer than 1μs, the steady-state $V_{th}$ of FeFET is saturated.

Fig. 7 shows simulated the Schmoo plots of FeFET steady-state (10s after the programming pulse) memory window (MW) using the bias scheme in Fig. 5(a). On the whole, the IL traps did not remarkably alter the steady-state memory window landscape compared to the ideal FeFET,

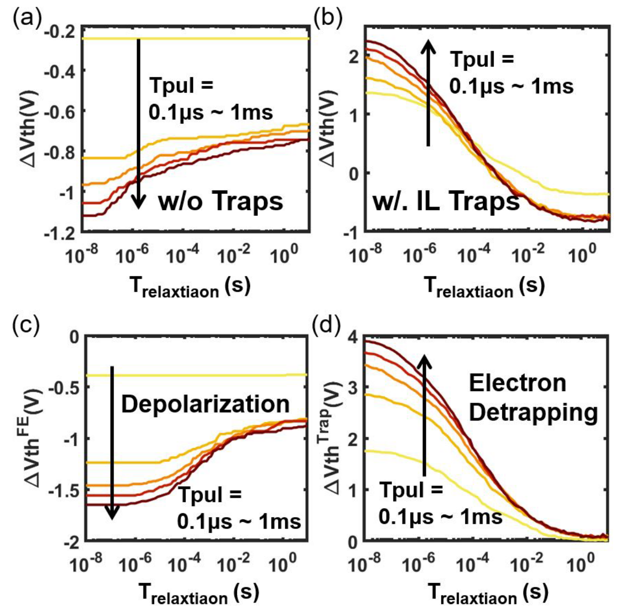


Fig. 6 Simulated ΔVth (w.r.t MOSFET Vth) of FeFET during pulse relaxation: (a) without and (b) with IL traps. The latter can be decomposed into (c) polarization charges-induced $\Delta Vth^{FE}$ and (d) trapped charges-induced $\Delta Vth^{Trap}$. $T_{pul}$ is varied from 0.1μs to 1ms with $V_{pul}$ fixed at 5V.

corroborating the assumption in [3] that these electrons are 'unstable and unrelated to ferroelectricity', except for a slight boost under longer $T_{pul}$ and larger $V_{pul}$ stress, where CT are more likely to involved, even though they all quickly detrapped during the relaxation (see the first panel in Fig. 7(c)). During the stressing stage, the trapped electrons partially screen the depolarization field $E_{dep}$ (as evidenced by smaller $E_{dep}$ at the start of relaxation), so the $P_{FE}$ could reach higher value. As the electrons detrap, the $E_{dep}$ increases which accelerates the depolarization. The decreased $P_{FE}$ partially counteract the $E_{dep}$ (since $E_{dep} \propto P_{FE}$ [16]). Finally,

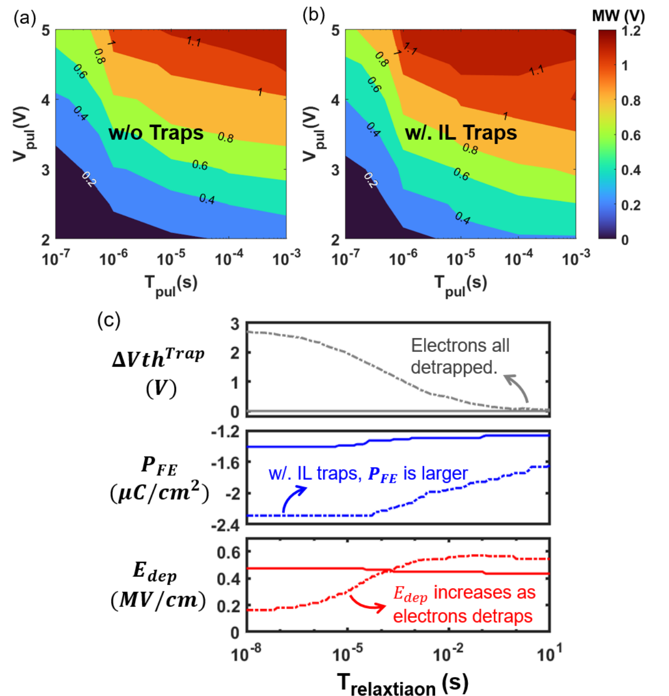


Fig.7 Steady state MW for FeFET: (a) without traps and (b) with IL traps. (c) For $T_{pul}$=0.1ms $V_{pul}$=4V, the evolution of the three key variables with (dashed) and without (solid) IL traps.

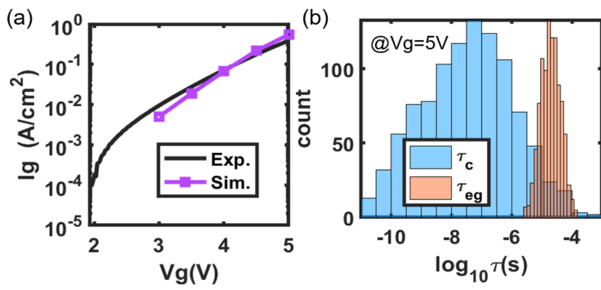


Fig. 8 (a) Measured and simulated gate leakage current. (b) distribution of $\tau_c$ and $\tau_{eg}$ at Vg=5V. The FeFET is initialize with 5V 10ms pulse before leakage measurement.

the FeFET is stabilized at a higher $E_{dep}$ level than the no-trap case, meanwhile retaining part of the bonus $P_{FE}$ bestowed by the previously trapped electrons.

In addition, the IL traps are also responsible for the trap-assisted tunneling (TAT) leakage as shown in Fig. 8(a). Assuming two-step tunneling, the simulated result agrees well with the experiment. Fig. 8(b) plots the histogram of the time constants $\tau_c$ for electron capture from Si channel and $\tau_{e.g}$ for electron emission to the metal gate. The latter is much larger than the former, due to the inelastic tunneling through the thick FE layer as described by the decay factor in (10).

## IV. Summary

A Monte-Carlo based simulation method which couples the PS and CT is proposed, allowing us to investigate the impacts of their dynamic interplay on the characteristics of FE memory devices. IL traps in FeFET is found to slightly improve the steady-state MW through transient screening effect, and is responsible for the TAT current.

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