A Compact Model of FDSOI based 1-T Pixel Sensor for Design of In-sensor Computing

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Abstract—A compact model for photoresponse of Fully-Depleted Silicon-on-Insulator (FDSOI) based one-transistor (1-T) pixel sensor is proposed for the design of in-sensor computing. The model describes the photoresponse as the photoelectrons charging the device equivalent capacitors to obtain the threshold voltage (V_{th}) change and it is verified by both the TCAD and device in 22nm FDSOI technology node. By integrating the model into BSIM-IMG, the accuracy of array-scale in-sensor Vector-Matrix Multiplication (VMM) affected by device doping variation is evaluated using HSPICE.

Keywords—Compact model, 1-T pixel sensor, In-sensor Computing, FDSOI

I. INTRODUCTION

To reduce redundant data movement for efficient machine vision systems, the in-sensor computing (ISC) paradigm [1, 2] has been proposed recently by integrating parts of post-processing into the sensor. Various process functions have been implemented in the pixel array, such as move detection [3] and VMM operation [4], which significantly improved the overall performance. Benefit from the excellent CMOS compatibility and pixel functions monolithic integration, the novel 1-T pixel sensor based on FDSOI technology [5, 6] is an outstanding candidate for ISC. The compact model of this sensor is vital for the efficient evaluation of the array-scale photoelectric characteristics, as well as for the design in ISC applications. In this work, we propose a compact model for the photoresponse of FDSOI 1-T sensor to obtain its light-induced V_{th} change (ΔV_{th}). It is integrated into the BSIM-IMG [7, 8] to quantify the current characteristic with both optical and electrical bias, by which the array-scale in-sensor VMM performance and the influence of device variation can be evaluated using HSPICE.

II. MODEL DESCRIPTION & VERIFICATION

As shown in Fig.1(a), the FDSOI based 1-T pixel sensor is composed of a FDSOI MOSFET with p-doped substrate under the buried oxide (BOX). It has four terminals: drain,
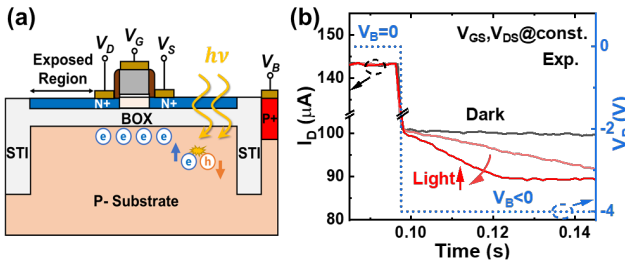
Fig.1 a) The schematic of FDSOI based 1-T pixel sensor. The gathered photoelectrons under the BOX cause the back-gate modulation to transistor. **b)** The measured device photoresponse characteristic. After applying negative V_B, the I_D decreases and then saturated over time under light exposure.
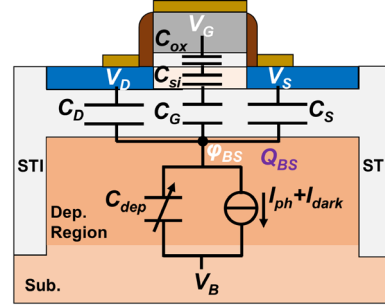
Fig.2 The photoresponse model description. The response is described as photo-e current (I_{ph}) and dark-e current (I_{dark}) charging the device equivalent capacitors. There are Q_{BS} electrons accumulated under BOX in the exposure time and φ_{BS} is consequently pulled down. The V_{th} of transistor is increased because the φ_{BS} acts as the back-gate bias.

gate, source on transistor and back bias on substrate. The exposure region is the part without the block of metal lines and gate. As shown in Fig.1(b), Its I_D decreases with exposure after applying negative V_B, which is measured from the device fabricated by 22nm FDSOI technology [5, 9]. The photoresponse mechanism is that depletion region under the BOX is pulled out by V_B and the photoelectrons together with dark-electrons are gradually accumulated by it. The potential under the BOX (φ_{BS}) is consequently decreased and the transistor V_{th} is increased due to back-gate modulation.

As shown in Fig.2, in our model, the photoresponse process is described as the charging process of photoelectrons and dark-electrons to the device equivalent capacitors, which are composed of the serial capacitors in the channel region ($C_{OX}||C_{si}||C_G$), the drain/source BOX capacitors (C_D/C_S) and the depletion region capacitor (C_{dep}). Regarding the depletion region as a half p-n junction with only p-part, the photo-electron current (I_{ph}) and the dark-electron current (I_{dark}) in our model are calculated by the same solutions of the hypothetical half p-part modified from typical photodiode models [10, 11]. The I_{ph} is written as:

$$I_{ph} = A_{ph} * (J_{dr} + J_{diff}) \tag{1}$$

where A_{ph} is the exposure area of the device. J_{dr}/J_{diff} is the drifting/diffusing current density of photoelectron, which are:

$$J_{dr} = q\Phi_{ph}[\exp(-\alpha W_{dep}) - 1] \tag{2}$$

$$J_{diff} = \frac{q\Phi_{ph}\alpha^2 L_n^2}{\alpha^2 L_n^2 - 1}\exp(-\alpha W_{dep}) \tag{3}$$

where $\Phi_{ph}=(1-R)P_{opt}/(hv)$, R is the light reflectivity, P_{opt} is the light intensity, hv is the photon energy. The α is the light absorption coefficient of Si, W_{dep} is the depletion width and the L_n is the electron diffusion length.

The I_{dark} is composed of three parts similar to the complete photodiode, which is written as:

$$I_{Dark} = A_{tot} * (J_S + J_{SRH} + J_{BBT}) \tag{4}$$

where A_{tot} is the total area of the device. $J_S/J_{SRH}/J_{BBT}$ is the intrinsic/Shockley-Read-Hall/Band-to-Band Tunnel current density [11], which are written as:

$$J_S = \frac{qn_i^2 D_n}{N_A L_n}[\exp(\frac{qV_{AK}}{kT})-1] \tag{5}$$

$$J_{SRH} = C_{SRH} F_{TD}[\exp(\frac{qV_{AK}}{2kT})-1]\omega_{SRH}W_{dep} \tag{6}$$

$$J_{BBT} = C_{BBT}V_{AK}F_{max}^2 \exp(\frac{-F_{BBT}}{F_{max}}) \tag{7}$$

where the $C_{SRH}/C_{BBT}/F_{BBT}$ are the adjustable model parameters and the other parameters are with the same meanings as described in [11]. The V_{AK} is the difference between the applied voltage and the equilibrium voltage across the depletion region. For the hypothetical half p-part in this model, it is written as:

$$V_{AK} = 2\phi_{Fp} - \varphi_{BS} + V_B \tag{8}$$

where the ϕ_{Fp} is the flat band voltage of the substrate and V_B is the voltage applied on the substrate.

Furthermore, the accumulated electrons (Q_{BS}) in the exposure time (t_{int}) are the integration result of the I_{ph} and I_{dark}, which is:

$$Q_{BS} = -\int_{t_{int}} (I_{ph} + I_{dark})dt \tag{9}$$

After that, solved from the voltage distribution relationships between $C_D/(C_{ox}\|C_{Si}\|C_G)/C_S/C_{dep}$, the φ_{BS} affected by the Q_{BS} under the BOX is written as:

$$\varphi_{BS} = \frac{2B - 4AC - 2\sqrt{B^2 - 4ABC}}{4A^2} + V_B \tag{10}$$

where intermediate variable A, B, C are written as:

$$A = C_D + C_S + (C_G \| C_{Si} \| C_{ox}) \tag{11}$$

$$B = 2q\varepsilon_{si}N_A A_{tot}^2 \tag{12}$$

$$C = Q_{BS} - C_D(V_D - V_B) - C_S(V_S - V_B) - (C_G \| C_{Si} \| C_{ox})(V_G - V_B) \tag{13}$$

where ε_{Si} is the dielectric constant of Si, N_A is the doping concentration of substrate, $V_D/V_S/V_G$ is the voltage applied on the Drain/Source/Gate terminal. Finally, the ΔV_{th} is obtained from the change of φ_{BS} in the t_{int} ($\Delta\varphi_{BS}$) based on the back-gate bias sensitivity in the typical SOI MOSFET model [7, 8], which is written as:

$$\Delta V_{th} = -\frac{C_G C_{si}}{(C_G + C_{si})C_{ox}}\Delta\varphi_{BS} \tag{14}$$

As shown in Fig.3(a) and (b), the model results show good agreement with the TCAD for the $\Delta\varphi_{BS}$ and ΔV_{th}
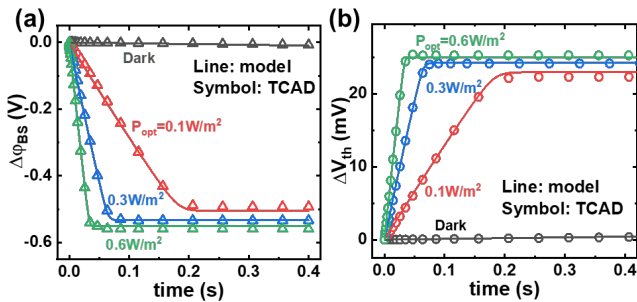
Fig.3 The evolution of **a)** $\Delta\varphi_{BS}$ and **b)** ΔV_{th} for device over the time under different incident light intensity (P_{opt}). Both these two model results show good agreement with the results from the TCAD.
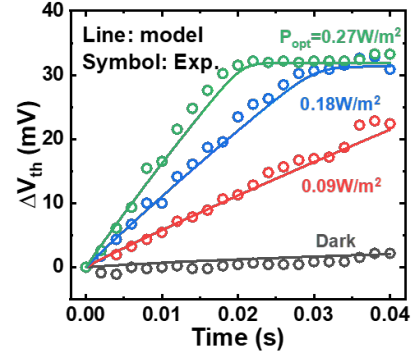
Fig.4 The ΔV_{th} under different P_{opt} obtained by the model agrees well with the experiment.

Tab.1 The adjustable model parameters for measured device. Their roles in the model are also listed.

Parameter	Role in	Value
R	I_{ph}	0.25
N_A	$\Delta\varphi_{BS}$	$1.1\times10^{18}cm^{-3}$
C_{SRH}	I_{dark}	$4\times10^3 A/V^3$
C_{BBT}	I_{dark}	$1\times10^3 A/V^3$
F_{BBT}	I_{dark}	$3\times10^9 V/m$

evolution by the exposure time. The model also shows good agreement with the measured ΔV_{th} evolution, as shown in Fig.4. There is no fitting parameter in the model. The adjustable parameters are the R affecting the I_{ph}, the N_A determining the effect of the Q_{BS} to the $\Delta\varphi_{BS}$, and the $C_{SRH}/C_{BBT}/F_{BBT}$ affecting the I_{dark}. These adjustable parameters used for measured device fabricated by 22nm FDSOI technology are listed in Tab.1.

Moreover, the proposed model can be added into the BSIM-IMG [7, 8], the typical FDSOI MOSFET model, to obtain the I_D affected by light as shown in Fig.5. The BSIM-IMG is composed of its core long-gate current model, V_{th} modification models, transport modification and other models. The proposed model describes the light-induced V_{th} change so it is added as an extra V_{th} model into the BSIM-IMG. The I_D results of the model combined with BSIM-IMG can be obtained from HSPICE. As shown in Fig.6(a), the initial dark-state I_D agrees well with the experiments under different V_B. The pixel I_D related to the P_{opt} under different V_{DS} also shows good agreement with the measured data, which verifies our model and enables the array-scale evaluation for the ISC performance of the FDSOI 1-T pixel using HSPICE.
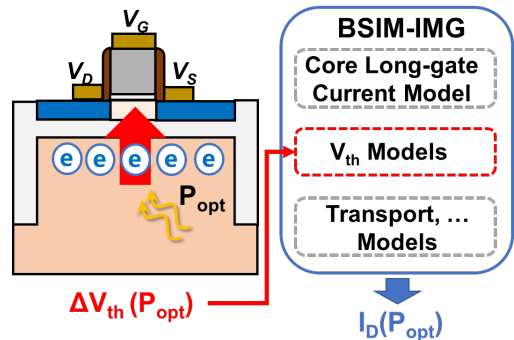
Fig.5 The light-induced ΔV_{th} of our model is integrated into the V_{th} models of the BSIM-IMG to obtain the device I_D affected by P_{opt}.

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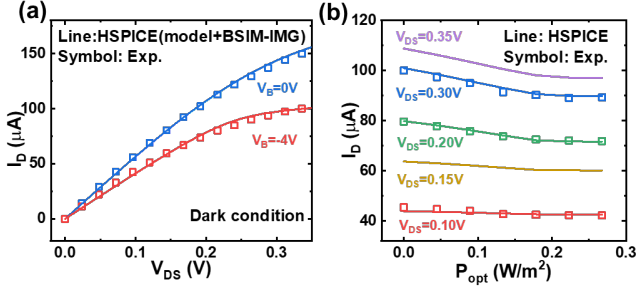
Fig.6 a) The dark I_D obtained from HSPICE (based on model combined with BSIM-IMG) agrees well with the experiment. **b)** The I_D related to P_{opt} obtained by the HSPICE shows good agreement with experiment.
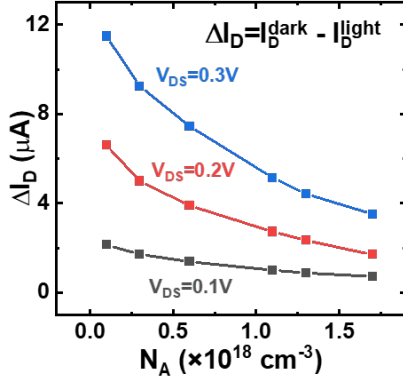

**Fig.7** The device light-induced ΔI_D related to the N_A predicted from the model.

III. ISC EVALUATION

Using the model combined with BSIM-IMG, the array-scale ISC performance affected by the device design size and process variation can be evaluated. The N_A variation is taken as evaluated example in this paper. As shown in Fig.7, predicted from our model, with higher N_A, the I_D difference between dark and light condition (ΔI_D) is decreased. Note that the I_{ph} keeps almost constant with N_A varying around 1×10^{18} because $W_{dep} \ll \alpha$ and $\alpha^2 L_n^2 \gg 1$ in the Eq.2 and Eq.3. The reason for the decreased ΔI_D is that the φ_{BS} decreased more with the increasing N_A according to the Eq.10 with the almost unchanged Q_{BS}.

Based on the effect of N_A variation to the photoresponse of the pixel cell, the effect of N_A variation to the in-sensor VMM is evaluated. As shown in Fig.8, the strategy of the VMM realized by the sensor array for evaluation is similar to
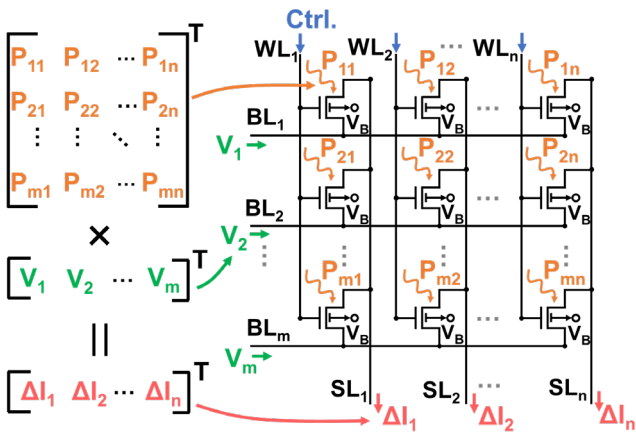
Fig.8 The strategy schematic of the in-sensor VMM using the FDSOI based 1-T pixel sensor array.
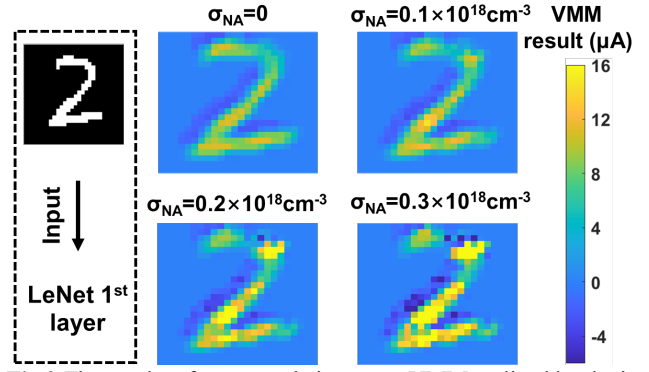
Fig.9 The results of an example in-sensor VMM realized by device array with different N_A variations. These results are simulated by HSPICE using the model combined with BSIM-IMG. The mean value of N_A variation is set as 1.1×10^{18} cm^{-3}.
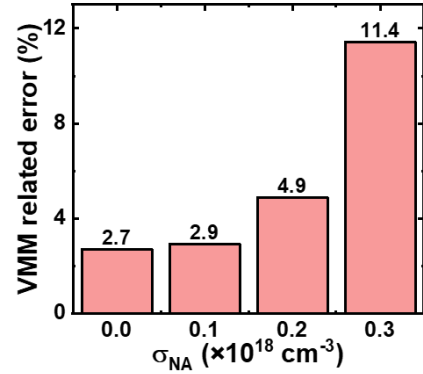
Fig.10 The related error of the VMM with N_A variations compared to the ideal result. With larger N_A variation, the calculation error of VMM is enlarged. The error without variation mainly results from the non-linear ΔI_D response to V_{DS}.

our previous work [5]. The pixels are wired in the crossbar-like array. The signal applied on the WL is the enabling signal of the VMM operation. The input matrix is mapped as the light intensities of the input image. The vector is mapped to the V_{DS} on the BLs. The operation results are obtained as the ΔI_Ds on the SLs. The positive vector elements and the negative elements are applied in the two different periods and their results are subtracted outside the array. The evaluated VMM results with different standard deviation of N_A (σ_{NA}) are shown in the Fig.9. It shows that the larger/smaller result tends to be even larger/smaller with larger σ_{NA}. The reason is that smaller N_A tends to occur with larger σ_{NA}, whose ΔI_D becomes larger according to the Fig.7. As shown in Fig.10, with the widened range of the results obtained from the pixel array with larger σ_{NA}, the related error to ideal is increased.

IV. CONCLUSION

A compact model for photoresponse of FDSOI based 1-T pixel sensor is proposed for ISC and verified by both TCAD and experiment. By adding into BSIM-IMG, the photoresponse I_D is obtained and the array-scale in-sensor VMM affected by N_A variation is evaluated. The proposed model can help for the design of ISC applications based on FDSOI 1-T pixel sensor.

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