Body resistance model for Partially Depleted SOI device: charge-based approach, extraction and Verilog-A implementation

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***Abstract*—The Partially Depleted Silicon On Insulator (PDSOI) transistor is used for a wide range of applications, in particular for RF. The current standard compact model of SOI-like transistor does not take into account a bias dependence of the body resistance. Building upon our experience developing the PSP model, we propose here a stand-alone Verilog-A model of body resistance. This nonlinear resistance model is validated against 3D TCAD and 65nm PDSOI experimental data.**

***Index Terms*—Body resistance, PDSOI, PSP, compact model, SPICE, Verilog-A**

I. Introduction

In addition to the four terminals (gate, source, drain and substrate), the Partially Depleted Silicon On Insulator (PDSOI) transistor has a fifth terminal: the body contact (cf fig. 1). It connects the silicon film and thus makes it possible to control its potential. In particular, it avoids the instability of the threshold voltage. This additional contact introduces capacitances associated with the extrinsic gate but also an additional nonlinear resistance, the so-called "body resistance" (Rbody), which is a crucial point in PDSOI modeling. It varies with the different biases and depends on the doping profile, the thickness of the channel, the silicon film, etc. This has an impact on the frequency characteristics of the transistor. Previous work [1], [2] gives an insight into the behavior of such a resistance included in the PSP-SOI model. In contrast, BSIM-SOI [6] introduces this feature through a constant resistance value (RBDB and RBSB parameters).

In this paper, we present our stand-alone Rbody model. In Section II, we focus on the core charge model. Then, in section III, the model is validated against experiments on 65nm PDSOI technology. Finally, in section III the stand-alone Rbody model is connected to PSP to show the frequency dependence effect.

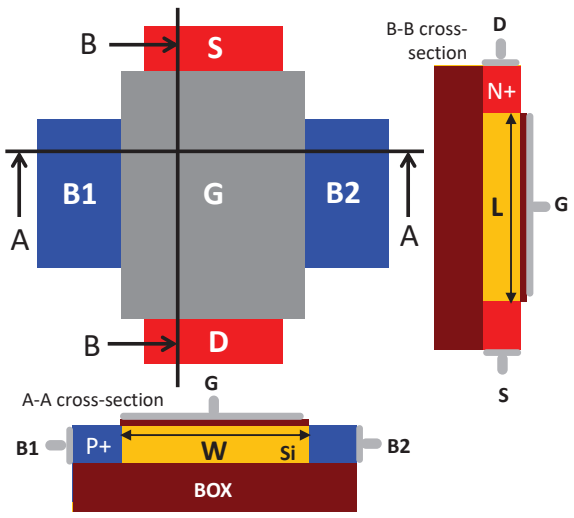


Fig. 1. PDSOI structure and definition of the main geometrical, doping and electrical parameters (contacts B1 and B2 are used for body resistance measurements).

TABLE I
Main model parameters

	Default value	Parameter definition
TOX	2.0E-9	Front gate equivalent oxide thickness
TSI	1.0E-8	Silicon film thickness
TBOX	1.0E-7	Back gate equivalent oxide thickness
VFB	-1	Flat band voltage at TR (V)
NEFF	5.00E+23	Effective substrate doping (m-3)
DPHIB	0	Offset parameter for ϕ_b (V)
CF	0	DIBL-parameter
MUB	0.1	Majority carrier mobility (m2/V/s)
PEXP	0.5	Grading coefficient of junction
CJOR	1.0E-03	Zero-bias capacitance per unit-of-area
VBIR	1	Built-in voltage (V)
FACDEPC	1	Factor related to doping charge
FACBC	0	Factor related to body charge
FACXC	0	Factor related to shift of xc

II. Core model: from explicit charge solution to implementation of stand-alone solution

The main parameters of the model presented here are given in Table I. To take into account the nonlinear or bias-dependent nature of the body resistance, we use the body resistance expression given in [1], in particular:

$$R_b = \mathbf{W}/\left(\mathbf{L}\cdot\mathbf{MUB}\cdot Q_{tot}\right) \quad (1)$$

where the total charge Q_{tot} is the total mobile charge in the quasi-neutral body region. It can be expressed as:

$$Q_{tot} = \mathbf{FACDEP}\cdot q\cdot\mathbf{NEFF}\cdot\mathbf{TSI} - \left(\mathbf{TSI}\cdot\left(Q_{jS}+Q_{jD}\right)+Q_b+Q_e\right) \quad (2)$$

where the first term is the depletion due to substrate doping and the second term is the total bulk charge which includes the bulk charge induced by the front-gate voltage Q_b, the bulk charge induced by the back-gate voltage Q_e and the junction depletion charge at source side Q_{jS} and drain side Q_{jD}. Equations 1 and 2 lead to majority current flowing between the contacts B1 and B2 (holes for n-channel MOSFET) [1], [2].

The calculation of Q_b uses the front surface potential from the PSP model [3], [4] at the midpoint x_m to ensure Gummel symmetry:

$$Q_b = C_{ox}\cdot sign(x_g)\cdot\sqrt{x_m - 1 + e^{x_m}} \quad (3)$$

where $x_m = \left(x_s + x_d\right)/2$ is the surface potential midpoint, C_{ox} is the oxide capacitance, x_g is the gate potential normalized to the thermal voltage ϕ_T. Note that this expression includes the depletion term (linear term) and the hole accumulation (exponential term) induced by the front gate voltage. The calculation of $Q_{jS,D}$ is similar to the Juncap model [4]:

$$Q_j = \frac{C_{j0}\,V_{bi}}{1-\mathbf{PEXP}}\left[1-\left(1-V_j/\phi_b\right)\right] + 2\,C_{j0}\left(V_{AK}-V_j\right) \quad (4)$$

$$C_{j0} = \mathbf{CJOR}/\left(\mathbf{VBIR}\cdot\phi_b\right) \quad (5)$$

For the calculation of Q_{jS}, V_{AK} is equal to V_{SB}, while for Q_{jD}, V_{AK} is equal to V_{SD}.

Finally, the back-gate-induced bulk charge Q_e is expressed as:

$$Q_e = \mathbf{FACFBC}\cdot C_{box}\cdot\left(x_{sub}-x_{bm}\right) \quad (6)$$

where x_{sub} is the normalized substrate voltage, and x_{bm} is the mid-point back surface potential calculated as:

$$x_{bm} = \frac{1}{1+\frac{C_{box}}{C_{si}}}\ln\left(\frac{1+e^{x_m-\left(x_c-\frac{C_{box}}{C_{si}}x_{sub}\right)}}{1+e^{-\left(x_c-\frac{C_{box}}{C_{si}}x_{sub}\right)}}\right) \quad (7)$$

where C_{box} and C_{si} are the buried oxide and silicon capacitances and:

$$x_c = \mathbf{FACXC}\cdot q\cdot\mathbf{NEFF}\cdot\mathbf{TSI}\left(2\cdot C_{si}\cdot\phi_T\right) \quad (8)$$

For the sake of simplicity, the full explicit solution proposed in [2] was not used. Instead, a similar coupling was introduced between the front and the back interfaces (eq. 7) while the front surface potential was calculated from the bulk model (eq. 3).

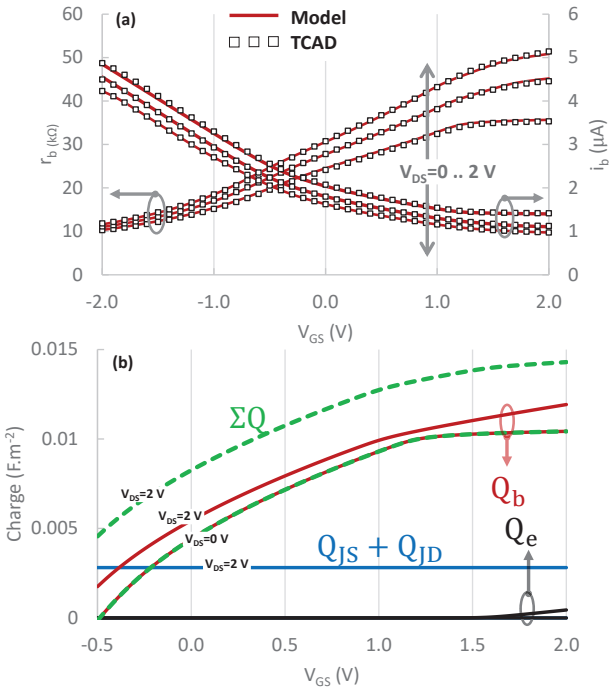


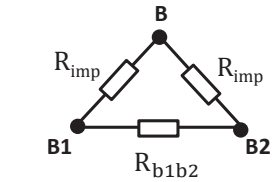
Fig. 2. (a) Model vs 3D TCAD simulations on r_b and i_b vs V_{GS} for V_{DS}=0, 1 and 2 V. (b) Bulk charge, source/drain junction charge and empirical body charge vs V_{GS} for $V_{DS}=0$ V and $V_{DS}=2$ V. 3D TCAD parameters are **NEFF** $=5\cdot10^{18}$cm^{-3}, $t_{ox}=2$ nm, $t_{si}=40$ nm, $t_{BOX}=100$ nm, $L=80$ nm and $W=5\mu$ m

Figure 2.a shows the agreement between the model and 3D TCAD simulations of a PDSOI device using Drift-Diffusion with constant mobility and high field saturation. The current i_b is measured between B1 and B2, as shown in fig. 1. In fig. 2.b, the charges Q_b, $Q_{jS,D}$ and Q_e are plotted as a function of the gate voltage. As expected, the main contribution comes from Q_b. Then, the junction capacitance charge $Q_{jS}+Q_{jD}$ is significant for large V_{DS}, but becomes negligible at low V_{DS}. Finally, the back-gate-induced charge Q_e is the least significant. However, it remains useful to fit the body resistance at large V_{GS}.

For this stand-alone resistance model, the topology presented in Fig.3 was chosen. Thus, the user can switch between two modes: the "measured" mode to extract the parameters on measured data and the "implemented" mode where the stand-alone model is connected to a bulk MOSFET model. The latter includes the distributed effects through a 1/3 factor and the parameter **NBCON**, which is the number of body contacts.

III. Parameter extraction methodology and experimental validation

Figure 4 illustrates the accuracy of the model with experimental data on 65nm PDSOI [7] for various geometries



$$R_{imp} = 2.\left(\frac{R_b}{3\,\mathbf{NBCON}^2} + \frac{\mathbf{Ra}}{\mathbf{NBCON}}\right)$$

$$R_{b1b2} = \frac{R_{imp}.(R_b + \mathbf{NBCON}.\mathbf{Ra})}{R_{imp} - (R_b + \mathbf{NBCON}.\mathbf{Ra})}$$

Mode	Resistance value	Verilog-A topology
"Measured" (resistance measurement using 2 body contacts)	$R_b + \mathbf{NBCON}.\mathbf{Ra}$	Rimp, B1=B, Rb1b2, B2
"Implemented" (including MOS)	$\frac{R_b}{3\,\mathbf{NBCON}^2} + \frac{\mathbf{R_a}}{\mathbf{NBCON}}$	Rimp, B1=B2, Rimp, B

Fig. 3. Model topology for measurement and coupled with bulk transistor model. Note that B, B1 and B2 are electrical node of Verilog-A module

and for several biases. After setting the process parameters, the extraction procedure is done in the following way: adjust doping and mobility parameters (**FACDEPC**, **MUB**); then tune **VFB**, **NEFF**, **DPHIB**, **FACDEPC** and **MUB**; then extract capacitance and DIBL parameters (**CJOR**, **PEXP**, **CF**); finally, extract Q_e-related parameters **FACBC** and **FACXC**.

The L and W dependences of each parameter P in Table I are captured with a scaling law similar to the one found in PSP [4]:

$$P = P_O + P_L \cdot (L_{EN}/L_E)^{P_{LEXP}} + P_W \cdot (W_{EN}/W_E)^{P_{WEXP}} + P_{LW} \cdot (L_{EN} \cdot W_{EN}/L_E/W_E) \quad (9)$$

For temperature scaling, a similar description is used: **VFB** is shifted by **STVFB** $\cdot\,(TKD - TKR)$ and **MUB** and **FACDEPC** are multiplied by $(TKR/TKR)^{ST_i}$, where TKR is the reference temperature (25°C) and TKD is the given temperature. Note that ST_i is also L and W dependent. The improved accuracy compared to previous PDSOI models [5] can be explained by the full decorrelation between the main transistor parameters (such as substrate doping) and the body resistance model.

Figure 5 shows a comparison of model vs experiment on the smallest devices. The same extraction strategy was used. Moreover, the effect of temperature variation is shown in Fig. 5b.

IV. Basic application on frequency dependence using PSP and Rbody model

To illustrate the frequency dependence induced by the body resistance, Figure 6 shows the simulation of small-signal quantities with or without the body resistance. Here, the model is set to "implemented" mode, as explained in Fig. 3.

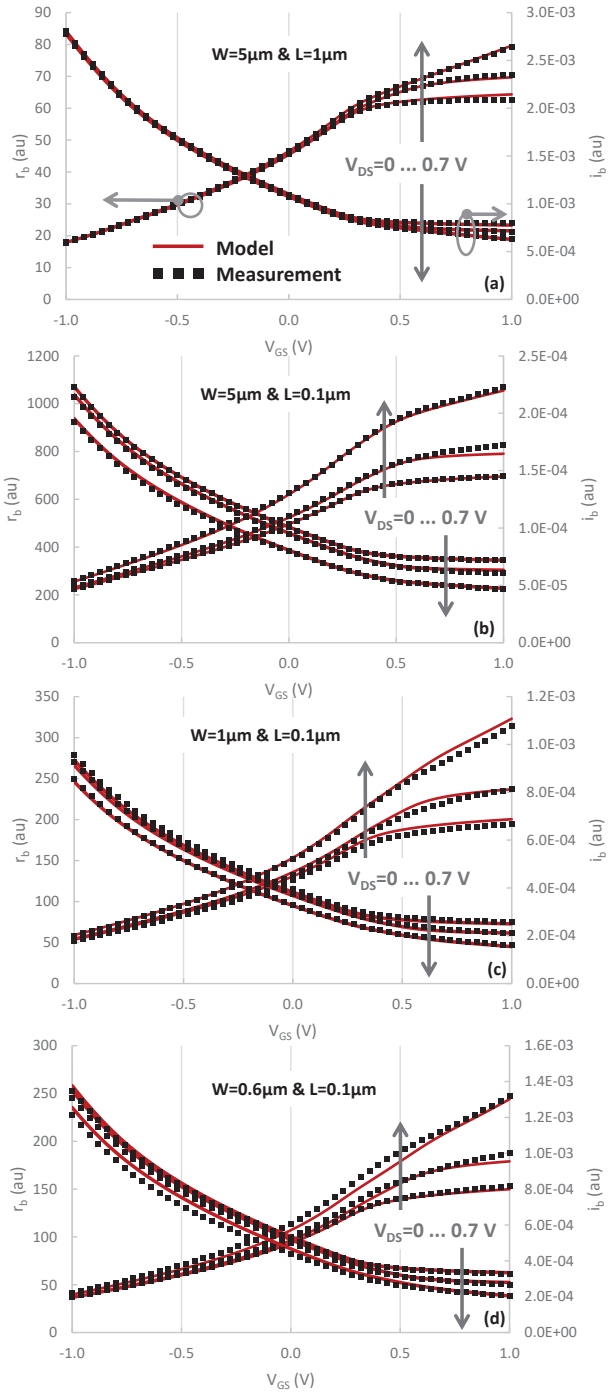


Fig. 4. Experiments from 65nm PDSOI technology (symbols) vs Rbody model (lines) in global mode vs V_{GS} for $V_{DS} = 0,\ 0.2$ and 0.7 V for different geometries: (a) $W = 5\,\mu$m and $L = 1\,\mu$m, (b) $W = 5\,\mu$m and $L = 0.1\,\mu$m, (c) $W = 1\,\mu$m and $L = 0.1\,\mu$m and (d) $W = 0.6\,\mu$m and $L = 0.1\,\mu$m. Note that the scale is in arbitrary units.

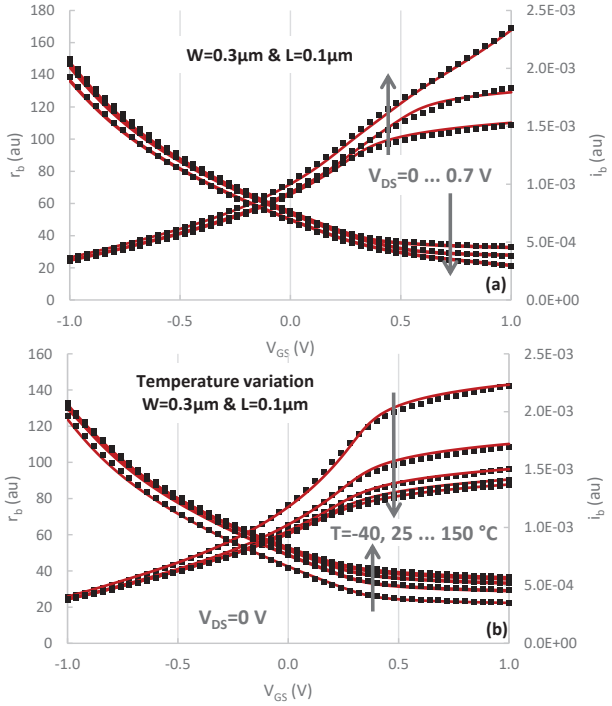


Fig. 5. Experiments from 65nm PDSOI technology (symbols) vs Rbody model (lines) in global mode (a) vs V_{GS} for V_{DS} = 0, 0.2 and 0.7 V for $W = 0.3\,\mu m$ and $L = 0.1\,\mu m$ and (b) vs V_{GS} for $V_{DS} = 0\,V$ for various temperature values. Note that the scale is in arbitrary units.

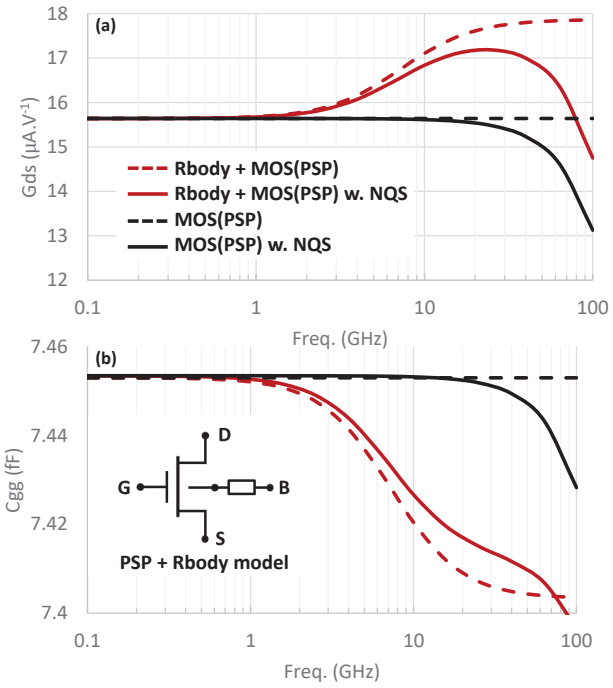


Fig. 6. Simulations of the Rbody model connected to a MOS transistor using PSP with the NQS model switched on or off (SWNQS=9 corresponding to 9 colocation points [4]): (a) Gds vs freq. and (b) Cgg vs freq. for large V_{DS} =V_{GS}= 2.0V.

As expected, our charge-based model is able to capture the frequency dependence caused by a change in body resistance. The NQS (Non-Quasi Static) model is added to capture the whole frequency dependence. Note that the NQS model uses the colocation points feature (SWNQS=9) as in PSP [4]. In conclusion, the proposed stand-alone model takes into account the bias dependence through explicit formulation of the charge and can be connected to any MOS transistor SPICE model. The proposed model is a good trade-off between runtime, accuracy and simplicity.

V. Conclusion

In this paper, we have presented a stand-alone bias-dependent body resistance model based that builds upon previous development of bulk [4] and SOI charge models [1]. This model reproduces all the main physical effects of a PDSOI body resistance. Moreover, we are able to capture the scaling effect and the bias dependence. Finally, we have shown that this stand-alone resistance model can be connected to a MOSFET to take into account the distributed effects. In a future work, this approach could be included in the core model of PSP.

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