A Compact Model of FTJ Covering the **Trapping/De-trapping Charateristics**

Ning Feng School of Electronic and Computer Engineering Peking University Shenzhen, China Ning0372@stu.pku.edu.cn

Yu Li School of Electronic and Computer Engineering Peking University Shenzhen, China 2101212717@stu.pku.edu.cn

Lining Zhang* School of Electronic and Computer Engineering Peking University Shenzhen, China lnzhang@ieee.org

Ning Ji School of Electronic and **Computer Engineering** Peking University Shenzhen, China Ningji@stu.pku.edu.cn

Puvang Cai School of Integrated Circuits Peking University Beijing, China. Caipy@stu.pku.edu.cn

Runsheng Wang School of Integrated Circuits Peking University Beijing, China. r.wang@pku.edu.cn

Abstract—Trap effects in the metal-ferroelectric-silicon (MFS) FTJs are modeled in this work. From the charge process under

conservation and voltage balancing principles, traps at the interface between the ferroelectric (FE) layer and silicon are incorporated into the FTJs' current-voltage characteristics. The trapping/de-trapping dynamics are coupled to the polarizations via a two-state model framework. The electrostatic potentials hence the barriers of tunneling, the trap charge state, and relaxations are all captured. Implications on FTJ operations under different frequencies are discussed around the trap effects on TER.

Keywords—TCAD, Trapping/De-trapping, self-consistent, dynamic Compact model, Ferroelectric tunnel junction

I. INTRODUCTION

In recent years, research on ferroelectric non-volatile memory has become increasingly in-depth and has received widespread attention from the physical mechanisms to the application [1-5]. Due to the simple structure and low power consumption, Ferroelectric tunnel junctions have become powerful candidate devices for NVM arrays and neuromorphic circuits. For MFS and MFIS structured FTJs, the trapping/de-trapping process at the interface can change the internal bias and barrier height of the FTJ [6-7], thereby affecting the critical characteristic TER, which is essential for the performance of FTJ in large-scale circuit applications. However, compact models for FTJ encompassing the trapping/de-trapping characteristics have yet to be studied. The simulation-friendly FTJ model with trapping/de-trapping needs to possess the following characteristics: 1) reflect the



Fig. 1. (a) Schematic of MFS-FTJ used in numerical simulation with interface trap. (b) Band diagram of MFS-FTJ with & without interface trap and the settings of physical features for numerical simulation is also listed.

Fangxing Zhang School of Electronic and **Computer Engineering** Peking University Shenzhen, China Fangxing.zhang@stu.pku.edu.cn

> Hao Li School of Electronic and **Computer Engineering** Peking University Shenzhen, China 2101212745@stu.pku.edu.

Ru Huang School of Integrated Circuits Peking University Beijing, China. ruhuang@pku.edu.cn

influence of different DOS distributions and trap density on FTJ characteristics; 2) describe the trapping/de-trapping different donor/acceptor-traps and deep/shallow levels; 3) describe the process of trap capture and emission in the time domain.

II. NUMERICAL SIMULATIONS & ANALYSIS

Fig. 1 shows the schematic diagram of the MFS-FTJ, the band diagram, and the settings of physical features in TCAD numerical simulation.

To analyze the physical characteristics more clearly, only acceptor-trap is introduced [8], which is charged (uncharged) by one electron when the trap levels below (above) the E_{f} . For n-type Si in the accumulation state, many acceptor-traps are occupied by electrons, allowing Si to maintain charge conservation without excessively bending the energy band, as shown in Fig. 1(b). However, when V_{si} is in the strong inversion state, the effect of acceptor-trap on FTJ will gradually decrease until it disappears.

Ultimately, acceptor-traps lead to a higher V_{fe} under the same external bias of FTJ, increasing the barrier height and reducing the tunneling current, as shown in Fig. 2. Furthermore, with the increase of trap density, the tunneling current in the depletion and accumulation states becomes smaller, and the numerical simulation result in the inset is calibrated against experimental data [9].



Fig. 2. Numerical simulation results of Current-voltage(I-V) with different trap density. Inset: calibration results between experimental data and numerical simulation.

III. MODELING THEORY & METHOD

There are two types of traps (acceptor and donor) at the interface and only acceptor-traps are focused on. The DOS distribution of traps in energy is approximated by an exponential distribution [10].

As shown in Fig. 3(a), two independent exponential distributions are used to accurately describe the DOS of the shallow trap and deep trap. Shallow traps (acceptor) are considered in this work.



Fig. 3. (a)Density-Of-States distribution in silicon band for acceptor-trap and donor-trap. (b) States transition of acceptor(donor)-trap for capturing and emitting electron(hole). (c) Equivalent sub-circuit of the trap kinetic equation. (d) The equivalent circuit of MFS-FTJ with considering interface trap.

The DOS of acceptor-traps in energy is given below:

$$N_{\iota A} = E_s \cdot g_c \cdot \frac{\frac{kT}{E_s}}{\sin\left(\frac{kT}{E_s}\right)} \cdot \exp\left[\frac{E_f - E_c}{E_s}\right]$$
(1)

where E_s represents the slope of the density of states distribution, and g_c represents the energy difference between the Fermi level and the conduction band edge.

The value of $E_f E_c$ is calculated by Eq. (2).

$$E_f - E_c = q \cdot V_{Si} - k \cdot T \cdot \ln\left(\frac{n_i}{N_d}\right) - \frac{E_g}{2} \qquad (2)$$

The captures charge density of acceptor-trap is given below:

$$Q_{tA}(V_{Si}) = q \cdot N_{tA} \tag{3}$$

Referred to references [11-12], captures charge density could be calculated in the time domain, as shown in Fig. 3(b). $p_{1/2}(t)$ represents the trap unoccupation/occupation probability and the net probability of occupied is derived as Eq. (4).

$$\frac{dp_2(t)}{dt} = K_{12} \cdot [1 - p_2(t)] + K_{21} \cdot p_2(t)$$
(4)

 $K_{12/21}$ is the transition rate (probability per unit time) as given below.

$$K_{12} = v_{th,n} \cdot \sigma_n \cdot n \tag{5a}$$

$$K_{21} = v_{ih,p} \cdot \sigma_p \cdot p \tag{5b}$$

For Eq. (5), $v_{th,n/p}$ represents the thermal velocity of carriers and $\sigma_{n/p}$ is the capture cross-sections.

For the dynamic trapped electrons, Eq. 4 can be rewritten as follows:

$$\frac{dN_{\iotaA,NQS}(t)}{dt} = \frac{N_{\iotaA} - N_{\iotaA,NQS}(t)}{\tau_c} - \frac{N_{\iotaA,NQS}(t)}{\tau_e}$$
(6)

The calculation of Eq. 6 can be facilitated by using the subcircuit approach, as shown in Fig. 3(c). $\tau_{c/e}$ represents the capture and emission time constants, expressed by Eq. 7, and α is a fitting parameter.

$$\tau_c = \frac{1}{K_{12}} = \tau_{c0} \cdot \exp\left[\frac{-qV_{Si}(t)}{\alpha \cdot kT}\right]$$
(7a)

$$\tau_e = \frac{1}{K_{21}} = \tau_{e0} \cdot \exp\left[\frac{qV_{Si}(t)}{\alpha \cdot kT}\right]$$
(7b)

The dynamic captures charge density of acceptor-trap is given below:

$$Q_{tA}(t) = q \cdot N_{tA,NQS} \tag{8}$$

The trapping and de-trapping characteristics of interface traps can be equivalent to a parallel capacitor C_{trap} connected on both sides of C_{si} . Due to charge balance, Eq. 9 can be derived as follow:

$$Q_{Fe} + Q_{Si} + Q_{tA} + Q_{tD} = 0 \tag{9}$$

The equivalent circuit of MFS-FTJ is shown in Fig. 3(d) and the voltage control equation is given by:

$$V_{FTJ} = V_{Fe} + V_{Si} + V_{fb}$$
(10)

Where V_{fb} represents the work-function difference.

Combined with references [3-4], calculations can be performed for the polarization characteristics (such as minor loops and dynamic polarization), potential, and current of the MFS-FTJ.

The overall model flowchart is shown in Fig. 4 and the calculation of the non-quasi-static module is based on the results of the quasi-static module.



Fig. 4. A flow chart of MFS-FTJ with trapping/detrapping characteristic, including a quasi-static module and a non-quasi-static module

IV. SIMULATION RESULTS & DISCUSSIONS

The trapping and detrapping process of MFS-FTJ is simulated with the proposed model and only acceptor-traps are considered with different E_s and g_c . The model simulation results and numerical simulation results are shown in Fig. 5.



Fig. 5. The charge density, captured by interface acceptor-trap, versus (a)(b) V_{si} and (c)(d) V_{FTJ} in quasi-static cases with different g_c and E_s . A hysteresis is shown at (c)(d) for the influence of polarization. P_{fe} versus V_{FTJ} for different (e) g_c and (f) E_s with agreements between model and numerical simulations. (g)(h) Si surface potentials and (i)(j) FE voltages from the model in comparison to numerical simulations. (k) and (l) plot Current density versus V_{FTJ} with the influence of trap.



Fig. 6. (a) and (b) show the corresponding tunneling electro-resistance (TER) and the read current of the ON and OFF states at $V_{read} = -0.2$ V.

Fig. 5(a-d) show the relationship of Q_{trap} with V_{si} and V_{FTJ} , as the Si surface potential decreases, the Q_{trap} exhibits an exponential decrease, which is well-fitted by the model and numerical simulation. In addition, due to the effect of polarization, the Q_{trap} exhibits a hysteresis curve as the V_{FTJ} scanning direction changes. Fig. 5(e-f) shows the effect of acceptor-traps with different distributions and densities on the polarization, and it can be seen that when Si is depletion state, more traps will increase the polarization under the same V_{FTJ} . Fig. 5(g-j) shows the voltages crossing the FE layer and Si layer. Due to the compensation of Q_{trap} for part of the polarization charge, the surface potential of silicon decreases, V_{fe} increases, and the situation becomes more evident as Q_{trap} increases. Fig. 5(k-l) show the characteristics of tunneling current with different g_c and E_s . Under the influence of traps, the increase in barrier height causes the tunneling current to decrease overall in the depletion region. For inversion states of Si, acceptor-traps have little effect on tunneling current characteristics.

Fig. 6(a) and Fig. 6(b) show the effects of g_c and E_s on TER and read current. It can be seen that with the increase of g_c , TER first increases and then decreases. There is an optical value for TER. For the increase of E_s , although the read current decreases overall, TER shows an increasing trend.

Our dynamic model couples the dynamic response of polarization and Q_{trap} . The relationship between V_{si} and $\tau_{c/e}$ is shown in Fig. 7(a) and 7(b), which follow the exponential distribution according to SRH theory. According to Eq. 7, $Q_{LA}(t)$ is directly related to $\tau_{c/e}$ corresponding to V_{si} . It can be observed that different V_{FTJ} scan directions correspond to different $\tau_{c/e}$ values in Fig. 7(c) and Fig. 7(d), affecting the hysteresis window of Q_{trap} - V_{FTJ} . It means that TER is affected by dynamic trapped charge.



Fig. 7. The relationship between the capture(emission) time constant and V_{si}/V_{FTJ} . According to SRH theory, there is exponential relationship between τ and V_{si} . τ exhibits a hysteresis curve as the V_{FTJ} scanning direction changes.



Fig. 8. Response of the interface trapped charge to the applied scan voltages.

We simulated the trap capture under triangular wave scan frequencies of 100kHz and 500kHz, respectively. The responses of Q_{trap} to triangular waves are shown in Fig. 8. With the increase of the triangular wave number, Q_{trap} shows a gradually increasing accumulation effect. In contrast, the amount of trapped charge is lower at higher frequencies, as shown in Fig. 8(b). This is because the rate of trapping/detrapping cannot keep up with the frequency of voltage.

Fig. 9(a) shows the gradual distortion of the *I-V* curve with the increase of the triangular wave number at 100kHz. Obviously, the accumulation of $Q_{tA}(t)$ with the increase in the number of triangle waves also affects TER. Fig. 9(b) shows the *I-V* curve at the fifth triangular wave for different frequencies and with the frequency increases, the distortion of the current curve becomes more severe. With or without interface trap, the trends of TER and read current are consistent, as shown in Fig. 9(c) and Fig. 9(d). It means that trapping/de-trapping and the dynamic switching process of polarization are tightly coupled.



Fig. 9. Current characteristic responding to (a) the numbers of triangle wave voltage and (b) the different frequency. Coupling dynamic polarization response, the TER and read current density under different frequencies (c) without considering trapping/detrapping and (d) with considering trapping/detrapping.

V. CONCLUSION

In this work, a compact model is proposed for MFS-FTJ with coupling dynamic polarization and trapping/de-trapping process, which could effectively reflect the influence of different trap type, density and frequency dependency. The compensating effect of interface traps on the band bending of Si surface is revealed and analyzed with model and numerical simulation.

ACKNOWLEDGMENT

This work is supported by the Natural Science Foundation of China under grants T2293700, T2293703, 62074006, the ShenZhen Science and Technology Project under grant GXWD20200827114656001, and the 111 Project under grant B18001.

REFERENCES

- Y. Peng *et al.*, "HfZrO x Hybrid DRAM/FRAM Arrays Featuring Excellent Endurance and Low Latency," *IEEE Electron Device Lett.*, vol. 43, no. 12, pp. 2101–2104, Dec. 2022, doi: 10.1109/LED.2022.3218862.
- [2] S.-H. Kuk et al., "Logic and Memory Ferroelectric Field-Effect-Transistor Using Reversible and Irreversible Domain Wall Polarization," *IEEE Electron Device Lett.*, vol. 44, no. 1, pp. 36–39, Jan. 2023, doi: 10.1109/LED.2022.3219247.
- [3] N. Feng et al., "A Dynamic Compact Model for Ferroelectric Capacitance," *IEEE Electron Device Letters*, vol. 43, no. 3, pp. 390– 393, Mar. 2022, doi: 10.1109/LED.2022.3141413.
- [4] N. Feng et al., "A Physics-Based Dynamic Compact Model of Ferroelectric Tunnel Junctions," *IEEE Electron Device Lett.*, vol. 44, no. 2, pp. 261–264, Feb. 2023, doi: 10.1109/LED.2022.3233456.
- [5] Z. Luo *et al.*, "High-precision and linear weight updates by subnanosecond pulses in ferroelectric tunnel junction for neuroinspired computing," *Nat Commun*, vol. 13, no. 1, p. 699, Feb. 2022, doi: 10.1038/s41467-022-28303-x.
- [6] R. Fontanini *et al.*, "Charge-Trapping-Induced Compensation of the Ferroelectric Polarization in FTJs: Optimal Conditions for a Synaptic Device Operation," *IEEE Trans. Electron Devices*, vol. 69, no. 7, pp. 3694–3699, Jul. 2022, doi: 10.1109/TED.2022.3175684.
- [7] X. Wang et al., "Deep insights into the Interplay of Polarization Switching, Charge Trapping, and Soft Breakdown in Metal-Ferroelectric-Metal-Insulator-Semiconductor Structure: Experiment and Modeling," in 2022 International Electron Devices Meeting (IEDM), San Francisco, CA, USA: IEEE, Dec. 2022, p. 13.3.1-13.3.4. doi: 10.1109/IEDM45625.2022.10019390.
- [8] TCAD Sentaurus Device Manual, Synopsys, Mountain View, CA, USA, 2021.
- [9] M. Kobayashi, Y. Tagawa, F. Mo, T. Saraya, and T. Hiramoto, "Ferroelectric HfO₂ Tunnel Junction Memory With High TER and Multi-Level Operation Featuring Metal Replacement Process," *IEEE J. Electron Devices Soc.*, vol. 7, pp. 134–139, 2019, doi: 10.1109/JEDS.2018.2885932.
- [10] M. Miura-Mattausch, H. Kikuchihara, T. K. Maiti, D. Navarro, and H. J. Mattausch, "Modeling of Carrier Trapping and Its Impact on Switching Performance," *IEEE J. Electron Devices Soc.*, vol. 6, pp. 1056–1063, 2018, doi: 10.1109/JEDS.2018.2862916.
- [11] W. Shockley and W. T. Read, "Statistics of the Recombinations of Holes and Electrons," *Phys. Rev.*, vol. 87, no. 5, pp. 835–842, Sep. 1952, doi: 10.1103/PhysRev.87.835
- [12] Y. Li et al., "A dynamic current hysteresis model for IGZO-TFT," Solid-State Electronics, vol. 197, p. 108459, Nov. 2022, doi: 10.1016/j.sse.2022.108459.