Random Telegraph Noise Simulation and the Impact on Noise Sensitive Design

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***Abstract*— Adopting SPICE simulation to access the impact from various noise sources of transistor such as flicker noise, thermal noise as well as shot noise on circuit performance has been a common way for circuit design. However, the implementation of Random Telegraph Noise (RTN) on existing design considerations is rarely addressed. In this paper, a practical model approach to simulate RTN through TSMC Model Interface (TMI) has been disclosed. The RTN simulation approaches are also demonstrated with a case that shows how to mitigate RTN for the noise sensitive circuit. Therefore, the RTN related simulations can be executed more correctly with the right expectation.**

Keywords—TMI, RTN Model

I. INTRODUCTION

Random Telegraph Noise (RTN) has been taken as a serious concern as device size is keeping scaling down with technology migration [1-7]. Meanwhile, RTN also shows significant impacts on various products under low bias operation such as wearable and Internet of Things (IoT) applications in both analog as well as RF oriented platform [8-10]. So, how to mitigate the impact of RTN in the early stage of design is important. On the other hand, even with continual process enhancement, the noise sensitive design will still suffer from RTN issues due to its inherently localized charge trapping and de-trapping near the channel of transistor or even in the gate dielectric which possibly leads to significant noise influence on circuit performance. Furthermore, Random Dopant Fluctuations (RDF) also plays a role as decreasing the driving voltage since the percolation paths could be the key to further increase the impact of RTN [11-12]. Under these circumstances and increasing complexity of circuit topology, the enablement of RTN model and corresponding design considerations are crucial for evaluating the robustness, functionality as well as competitive-ness of product.

II. RTN FUNDAMENTALS AND MODELING

Due to the trapping/de-trapping of the existent trap, the localized potential energy varies over time, leading to discrete current fluctuation/levels in time domain and denoted as RTN. Regarding the frequency response, the power spectrum density (PSD) of each trap is a Lorentzian shape as shown in Fig. 1.

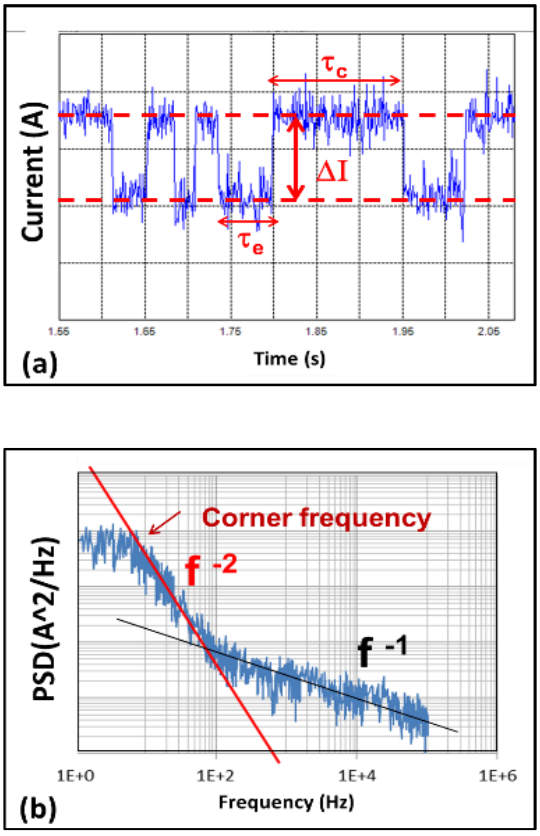
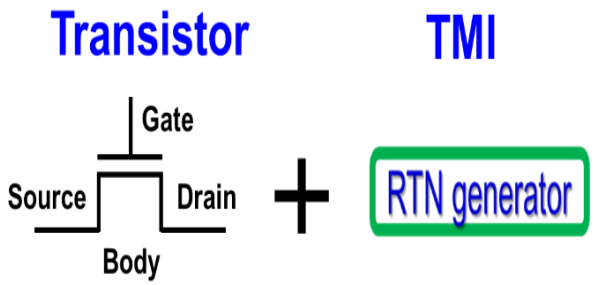
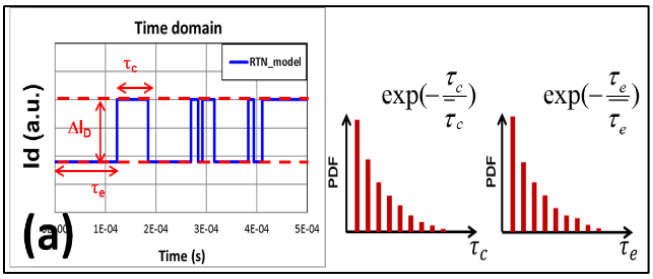
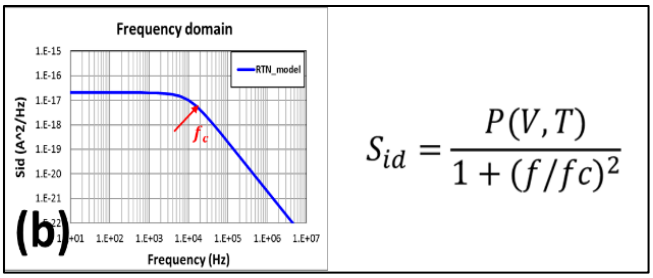


Fig.1 The Si data show RTN behavior in (a) time domain, and (b) frequency domain.

Based on the fundamental trap kinetics, each trap has its own transition rate across gate driving bias. Both the time to emission τ_e and capture τ_c follow the Poisson distribution with bias independent time constant τ_0. Instead of capturing each mesoscopic characteristic, the macroscopic behaviours that most represent Si trend are at the most forefront from design point of view. Therefore, the approximations of two discrete states with its equivalent magnitude as well as calibrated probability out of meaningful sample size have been deployed. For the randomness of switching, the time constant has been introduced into the model with reasonable $\bar{\tau}_e/\bar{\tau}_c$ ratio. To describe important RTN signatures in both time domain and frequency domain, the TMI, the industry standard model interface for circuit simulators, based RTN generator has been proposed as shown in Fig. 2.







$$S_{id} = \frac{P(V,T)}{1+(f/fc)^2}$$

Fig. 2 TMI-based RTN model simulation in (a) Time domain follows Poisson process (b) Frequency domain behaves as a Lorentzian shape. (c) Consistency between Fourier Transform of time domain and frequency domain

For time domain simulation, the transition probability matrix (Pij) is used to model the random switching behaviours. As shown in Fig. 2 (a), the probability density function (PDF) is exponential distributed ($\sim \exp(1/\tau_{c,e})$) and can be theoretically consistent with the Poisson process. Regarding frequency response as shown in Fig. 2 (b), the corner frequency (f_c) of the Lorentzian spectrum is set to $1/2\pi\tau_0$. In Fig. 2 (c), the proposed model is validated through the consistency examination between frequency domain and Fourier Transform of time domain. As you can see, the model is physically self-consistent. To faithfully reflect Si behaviours, the bias, temperature, and geometry dependencies are needed and adequately calibrated. The Si to simulation comparison of RTN is shown in Fig. 3, the RTN distribution can be well reflected. Furthermore, the equations adopted for modelling are listed in Table 1. Note that RTN is highly process-dependent, a TMI based infrastructure with its superior flexibility and efficiency in terms of formulation is the key for industrial-scale model construction with satisfactory accuracy as well as time to market.

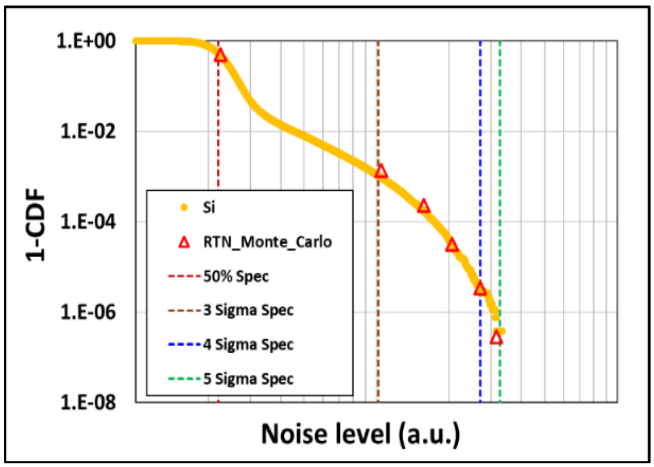


Fig. 3. Si to Simulation comparison of RTN tailing behavior. The distribution can be reflected.

Table 1. Eq (1) ~ (5) are adopted for RTN modeling. The bias, geometry and temperature dependence can be depicted.

$$\Delta V_{th} \propto c_1 {V_{gs}}^2 + c_2 V_{gs} + c_3 \quad (1)$$

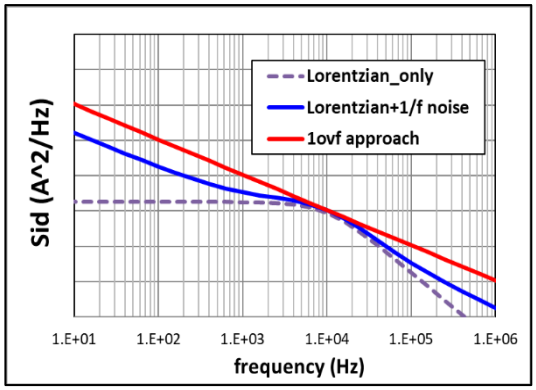
$$\Delta I_d = \Delta V_{th} \times G_m \quad (2)$$

$$S_{id} = 4\Delta {I_d}^2 (\tau_0/\bar{\tau}_c + \bar{\tau}_e)(\tau_0/1 + (2\pi f \tau_0)^2) \quad (3)$$

$$\Delta V_{th} \propto W^{a_1} L^{a_2} \quad (4)$$

$$\Delta V_{th}, f_c \propto \exp(b_1, b_2 \times (1/kT - 1/kT_0)) \quad (5)$$

When it comes to RTN, its statics is an important aspect because the randomness in RTN yield a prolonged distribution tailing. Instead of resorting to Monte Carlo approach that is costly and time consuming, a simplified alternative by using Flicker-like-Corner (1ovf) model approach is proposed for circuit-RTN simulation, as shown in Fig. 4. It can be regarded as a special corner model, in which we consider all the possibility with respect to the time constant of RTN under same magnitude at the worst condition (for example, δV at 0.1% cumulation).



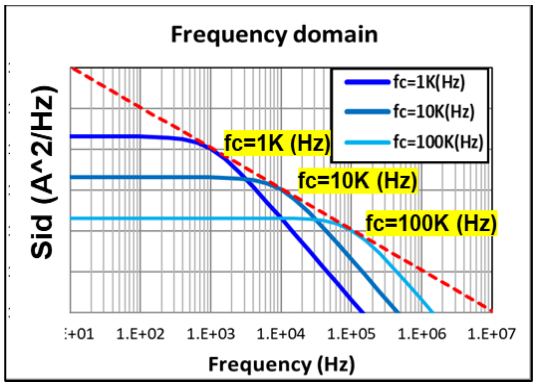


Fig. 4. Schematics of 1ovf model which is a versatile and efficient approach for RTN judgement in early stage.

This assumption could be somewhat pessimistic, but 1ovf model can provide some meaningful insights in the early design stage. Specifically, it's useful to identify the major RTN contributors efficiently even for complicated circuitries or large-scale systems and helpful to ease the loading regarding following analysis and optimization.

III. CIRCUIT SIMULATION WITH RTN MODEL

Based on the aforementioned model approaches, the design optimization techniques to take RTN into account have been demonstrated in this section. Three distinct types of RTN models are as follows: Lorentz, 1ovf (Worst linear) and Monte Carlo methods are utilized for design judgment. A full block diagram of oscillator design has been shown in Fig. 5 which is inherent sensitive to noise. The sub-blocks such as inverter buffer, constant-gm and current controlled oscillator (ICO) have been identified as RTN sensitive parts.

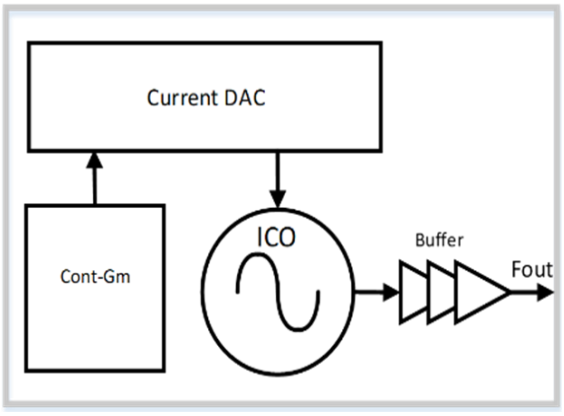


Fig. 5. The block diagram of the current control oscillator which is composed of several circuitries.

The buffer consists of 6-stage inverters with an input clock frequency of 5GHz which has been depicted in Fig 6 (a). Regarding the performance of the inverter buffer, the phase noise can be considered as the most critical figure of merit (FoM) in terms of noise analysis. By applying three types of RTN simulation approaches as shown in Fig 6 (b), the simulation result of phase noise analysis with Lorentz model shows similar spectrum as for transistor level counterpart with corner frequency in the vicinity of 1 kHz. Regarding the simulation result of 1ovf model, it shows a relative conservative prediction over all frequency range like as mentioned in section II. However, the 1ovf model is suitable for buffer-based design sign-off since it provides better efficiency without sacrificing accuracy for the design of interest region. On the other hand, the Monte Carlo method is the most accurate approach since it reflects the randomness of RTN in terms of amplitude, corner frequency as well as the chance to happen for all transistors in the inverter buffer. However, designers will need to consider the simulation time overhead if they would like to adopt Monte Carlo method to check how much margin is still reserved.

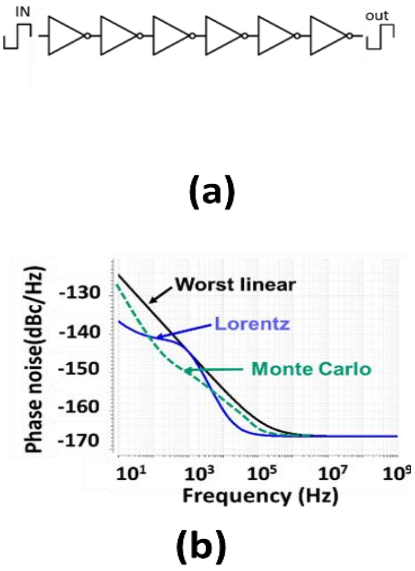
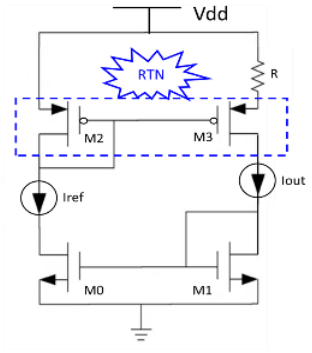
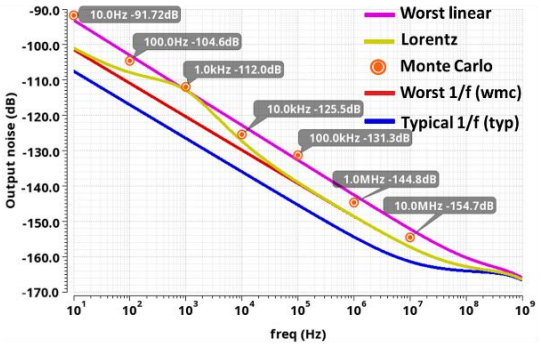


Fig. 6. (a) Schematic of 6-stages inverter buffer. (b) The phase noise simulation results of the buffer with 3 different RTN model.

The schematic of the constant gm current source has been shown in Fig. 7 (a) which is composed of NMOS M0/M1, PMOS M2/M3 and a fixed resistor R since the M3 is N times larger than M2 where N is an integer number. With similar analysis methodologies, the output noise simulation results of constant gm block by different noise model are shown in Fig. 7 (b). RTN 1ovf model shows almost 7dB worse than the worst 1/f noise case. Therefore, design optimization is needed to mitigate RTN for the constant gm circuitry. Based on the analysis, the upper two transistors M2 and M3 can be identified as the major RTN contributors. It's quite reasonable because M3 needs to be operated in sub-threshold region and M2 is the transistor with much smaller gate area than M3. As far as we know, both the conditions could lead to significant RTN influence easily. To mitigate RTN impact, enlarging the gate area of M2 and M3 is the most effective way to mitigate the impact of RTN. The simulation results of output noise show an obvious improvement in Fig. 7 (c). The RTN impact becomes much smaller after size tuning.



(a)



(b)

Original:

Frequency (Hz)	10	100	1k	10k	100k	1M	10M
RTN impact (dB)	**6.8**	**6.0**	**5.3**	**2.9**	**3.1**	**1.5**	**1.4**

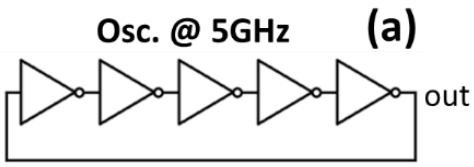
Area increased:

Frequency (Hz)	10	100	1k	10k	100k	1M	10M
RTN impact (dB)	**1.2**	**1.0**	**0.9**	**0.6**	**0.6**	**0.5**	**0.3**

(c)

Fig. 7. (a) Constant gm current source schematic. (b) Output noise simulation of constang gm current source in different noise model. (c) The reduction of RTN influence after design optimization.

Regarding the oscillator design, the ICO usually plays a key role to contribute most of the noise and the phase noise is also considered as the critical FoM. To reach a high-quality design requirement, the statistical distribution of phase noise should be taken care of as well. In Fig. 8., the simulation results show an obvious long tail which is attributed to RTN based on Monte Carlo analysis with respect to phase noise of oscillator. Following the same concept to make more secure design, the transistor size has been optimized so that the distribution of phase noise can be greatly improved. Under actual PPA consideration, the quantitatively analysis out of dedicated RTN model could be quite beneficial.



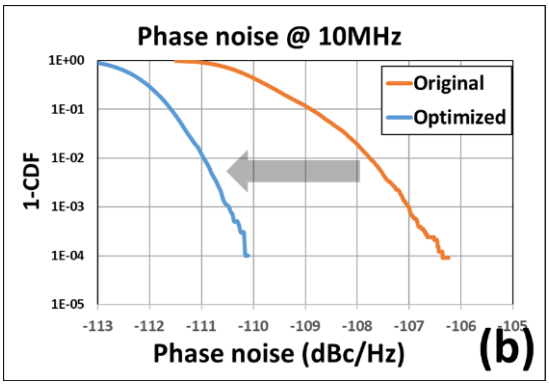


Fig. 8. (a) Schematic of ICO. (b) Phase noise simulation of ICO shows the reduction of distribution tailing after design optimization.

IV. Conclusion

In this paper, we've disclosed a TMI-based RTN model which is feasible for industrial usage and beneficial for noise-oriented designs as well. Several simulation approaches have also been demonstrated for RTN analysis. With RTN model, designers can optimize the circuitries more comprehensively and efficiently. In summary, yield improvements as well as shorten development cycle could be expected.

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