Self-Heating Influence on Hot Carrier Degradation Reliability of GAA FET by 3D KMC Method

Songhan Zhao, Pan Zhao, Yandong He, Gang Du*
School of Integrated Circuits, Peking University, Beijing 100871, China
Beijing Advanced Innovation Center for Integrated Circuits
* Email: gangdu@pku.edu.cn

***Abstract*—The self-heating coupling of the hot carrier degradation effect is studied in detail. The results show that self-heating has a strong activation impact on hot carrier degradation. By simulating the influence of various temperature driving forces on reliability assessment, the necessity of using temperature gradient driving forces in the evaluation and prediction process is demonstrated. The temperature gradient inside the channel causes the trapped defects to concentrate toward the drain side. The threshold voltage degradation of each channel is separated from the multi-stack GAA device, which indicates that the reliability degradation of the intermediate channel is evidently different from the overall threshold voltage drift due to severe thermal effects.**

Keywords—self-heating, hot carrier degradation, threshold voltage degradation, temperature driving forces

I. INTRODUCTION

Node scaling and innovations in device architecture perpetuate Moore's Law to meet performance demands. However, the intensification of the quantum confinement exacerbates the serious self-heating effect (SHE), which seriously affects the reliability of the device [1-8], including hot carrier injection (HCI) [9-10] , bias temperature instability (BTI) [11] , and time-dependent dielectric breakdown (TDDB) [12]. The persistent self-heating effect not only degrades the device performance and lifetime, but also directly influences the normal operation of the circuit. Therefore, the self-heating and reliability issue for nanoscale devices, particularly in sub-7nm technology node, is still worth to continuing and in-depth study. Moreover, IC and device testing still faces the challenge of difficult operation and limited accuracy [13]. In that case, simulation methods and simulation rehearsals play a key role in avoiding early failures and providing predictive solutions.

In the circuit operating state, self-heating has a significant impact on HCI. As the stress conditions of HCI mode inevitably excites the transient thermal response of the device, especially for the nanoscale devices. Until now, in HCI studies, the impact of the self-heating effect is usually calculated and quantified through the maximum lattice temperature [14], and few articles introduce the effect of SHE on the defect behavior of HCI and the difference in reliability evaluation by using various temperature driving forces. In this work, reliability degradation affected by self-heating acceleration and temperature-driven forces is investigated, and the necessity of using temperature gradient for evaluation system is indicated.

II. SIMULATION AND RESULTS DISCUSSION

The hot carrier degradation (HCD) coupled with the self-heating effect is systematically studied. Kinetic Monte Carlo (KMC) method based on multi-defect process coupling is adopted to simulate the dynamic behavior of traps under different stress states by statistically calculating the probability of defect processes. In addition, the two-state nonradiative multiphonon (NMP) theory is adopted to calculate the time constant of stress-dependent defect behavior, and for the defect tunneling (defect coupling) phenomenon, the WKB method is used [15]. For the electrical properties, TCAD simulation method is used to obtain the initial device characteristics. The detailed simulation framework is plotted in Fig. 1. Device structure parameters and the model-related physical quantity parameters are shown in Table 1.

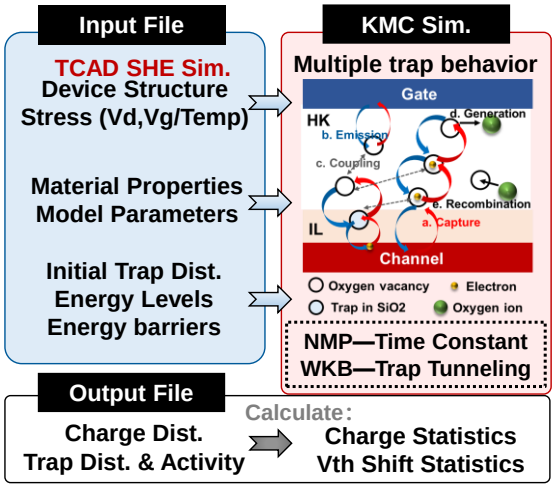

Fig. 1. The simulation process block diagram, including input and output and statistical results of trap dynamic behaviors.

TABLE I. Device and Model Parameters

Para.	*Specific meaning*	*Value*
Device Structure Parameters		
Lg	Channel length	12nm
Wsh	Sheet width	25nm
Hsh	Sheet height	5nm
Tox-HK	High-K layer	3.5nm
Tox-IL	SiO2 layer	0.4nm
Interface States Parameters		
hω	Oscillator levels	0.075eV
Eb	Bond dissociation	1.5eV
fe	Vibration frequency	$0.1ps^{-1}$

Fig. 2 describes the degradation of the threshold voltage of nanosheet device with or without thermal acceleration. The fluctuation amplitude of the HCD due to self-heating activated increased by a factor of 6.52 at 1000s. Trapped charges at random times along the direction of the gate dielectric are calculated and shown in Fig. 3. In the absence of SHE, the captured charge is uniformly distributed along the gate dielectric layer. However, with the participation of self-

heating effect, the captured charge mostly appears in the channel and interfacial layer (IL) interface, while less charge is trapped in the HK layer. Fig. 4 shows the cumulative distribution of ΔVth based on statistics of 200 sample devices. The cumulative distribution of ΔVth is significantly enhanced by self-heating, thus the trailing is obvious. The defect activity statistics along gate dielectric distribution are shown in Fig. 5 (right), indicating that degradation mechanism of hot carriers strongly depends on self-heating acceleration, with obvious activity of defects observed at the channel and IL interface.

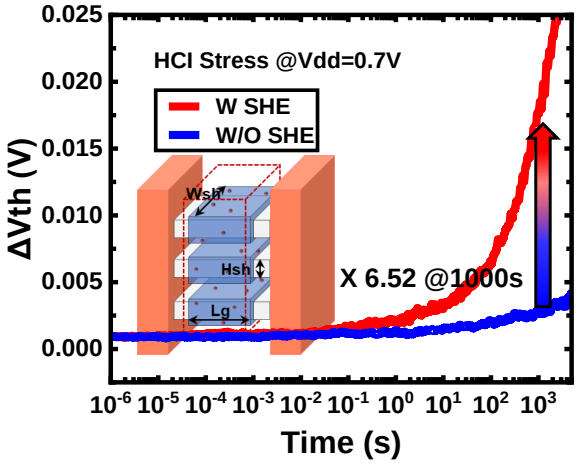

Fig. 2. The time-dependent degradation of the threshold voltage, with and without self-heating effect at nominal voltage.

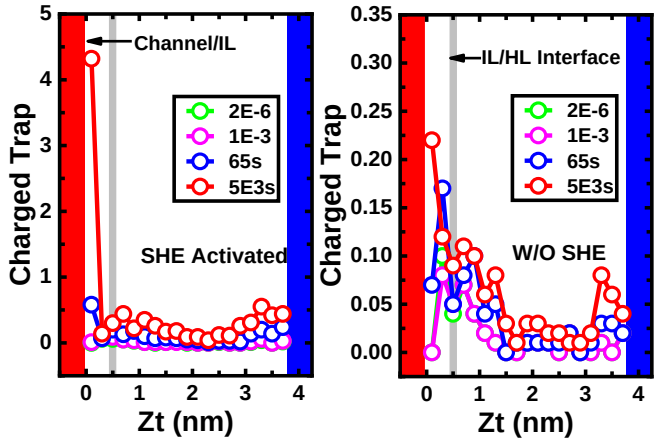

Fig. 3. Count of charged traps along the thickness of the gate dielectric at different random times.

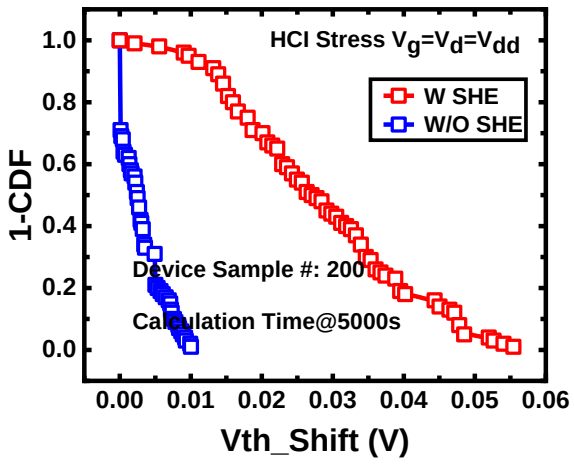

Fig. 4. Cumulative distribution of device under HCI stress, with and without SHE at nominal condition.

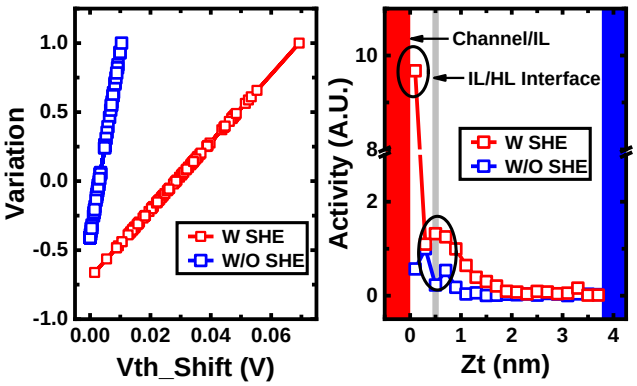

Fig. 5. Threshold voltage variation in both cases (left), and trap activity along the gate dielectric thickness(right).

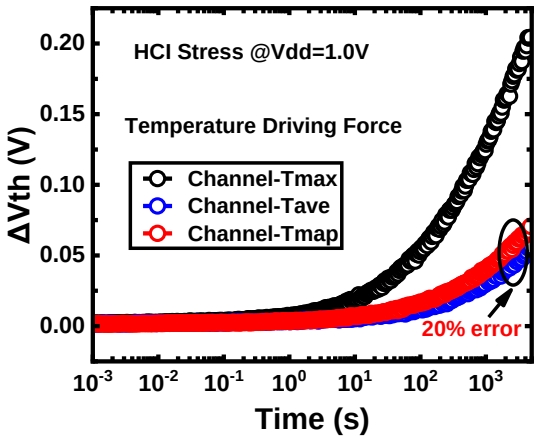

Fig. 6. Threshold voltage degradation under different temperature driving forces @Vdd=1.0V.

Maximum lattice temperature (Tmax) is widely used to quantify and evaluate HCD. The inaccuracy of estimation by using the Tmax and channel average temperature (Tave) is demonstrated in this part. Fig. 6 shows the time evolution curves of the threshold voltages extracted by the Tmax, Tave, and Tmap (channel temperature gradient), respectively. Even with Tave estimation, it still exhibits a 20% error with the degradation of the hot carrier driven by the Tmap. At 1000s, IL interface defects contributed 23.38% of the error ratio, while the HK layer contributed about 10%, as shown in Fig. 7. Fig. 8 shows the schematic diagram of the defect distribution under the corresponding driving force. Temperature gradient driving exhibits a phenomenon similar to gradient wind, which makes the defect distribution closer to the drain side.

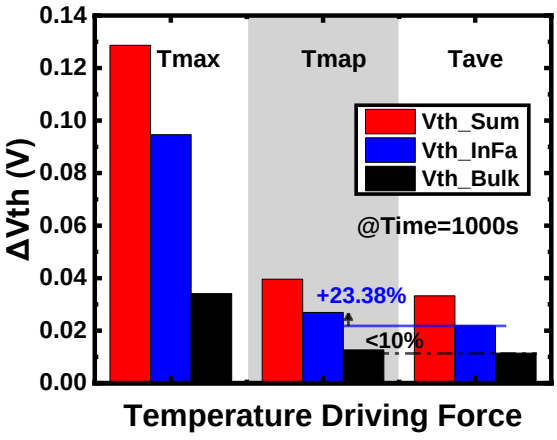

Fig. 7. Comparison of threshold voltage degradation and component degradation after 1000s stress.

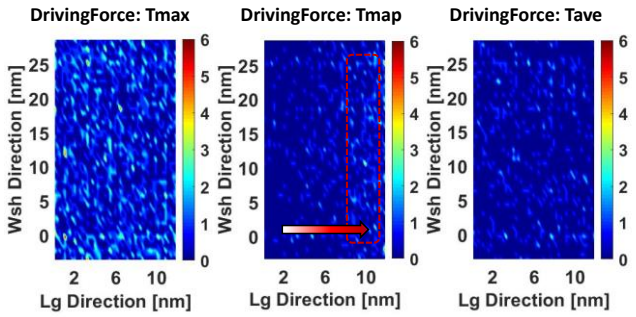

Fig. 8. Average statistical plot of charge distribution along channel direction of multichannel stacked devices driven by different temperature stresses.

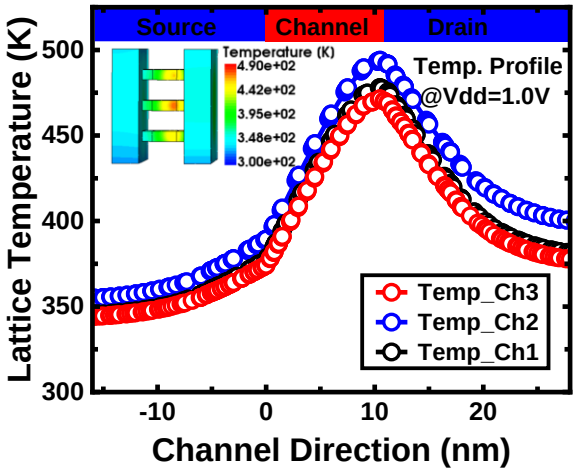

Fig. 9. Lattice temperature rise caused by self-heating effect of different channels is obtained by TCAD simulation.

The temperature profile along the channel direction based on TCAD simulation, as shown in Fig. 9, reveals that multi-stacked device have different characteristics in terms of SHE between channels. The defect statistical distribution for different channels is shown in Fig. 10, Channel 3 (Ch3) generates the fewest number of defects, mainly for the reason of closer distance to the substrate that favors heat dissipation and weaker SHE, see in Fig. 9, which to some extent limits the defect growth. Fig. 11 shows a schematic diagram of the contribution separation of threshold voltage fluctuation for multi-stacked devices, which demonstrates that the large threshold voltage fluctuation of Channel 2 (Ch2) is the main contribution source for the overall device threshold drift.

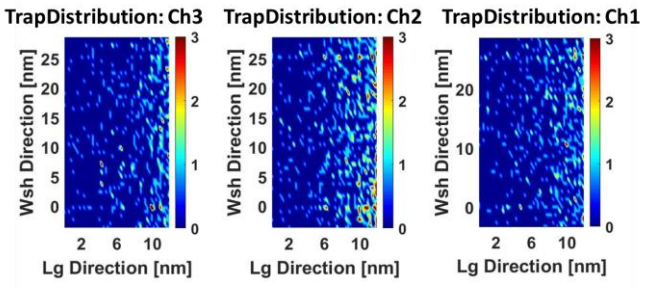

Fig. 10. Cross section along the channel direction of trapped charge distributions for different channels (200 samples).

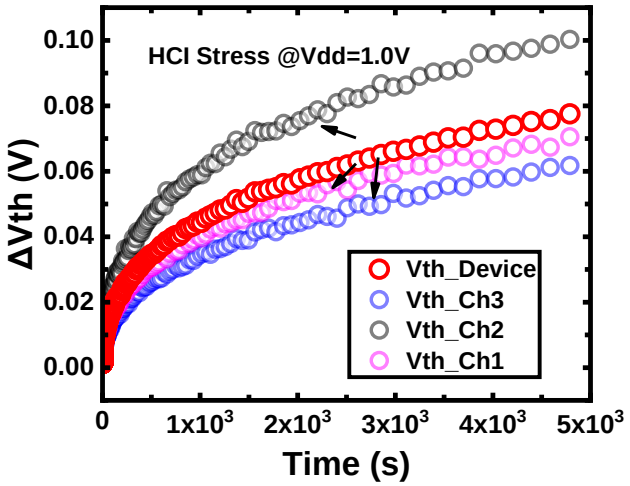

Fig. 11. The threshold voltage degradation between different channels separated from multi-stacked nanosheets.

III. Conclusion

In this paper, the KMC method is used to systematically study the acceleration of SHE on hot carriers, indicating that HCD is strongly dependent on thermal coupling, and channel temperature gradient should be used as the temperature driving force in the evaluation process to avoid errors. In addition, the threshold voltage separation of multi-stacked devices shows that the intermediate channel sheet contributes most significantly to the threshold voltage degradation of the whole device, and severe self-heating is the trigger.

IV. References

[1] P. Paliwoda et al., "Self-Heating Effects on Hot Carrier Degradation and Its Impact on Logic Circuit Reliability," in IEEE Transactions on Device and Materials Reliability, vol. 19, no. 2, pp. 249-254, June 2019.

[2] V. M. van Santen, P. R. Genssler, O. Prakash, S. Thomann, J. Henkel and H. Amrouch, "Impact of Self-Heating on Performance, Power and Reliability in FinFET Technology," 2020 25th Asia and South Pacific Design Automation Conference (ASP-DAC), Beijing, China, 2020, pp. 68-73, doi: 10.1109/ASP-DAC47756.2020.9045582.

[3] C. Prasad, "A Review of Self-Heating Effects in Advanced CMOS Technologies," in IEEE Transactions on Electron Devices, vol. 66, no. 11, pp. 4546-4555, Nov. 2019, doi: 10.1109/TED.2019.2943744.

[4] E. Bury et al., "Self-heating in FinFET and GAA-NW using Si, Ge and III/V channels," 2016 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 2016, pp. 15.6.1-15.6.4. doi: 10.1109/IEDM.2016.7838425.

[5] S. J. Kang, J. H. Kim, Y. S. Song, S. Go and S. Kim, "Investigation of Self-Heating Effects in Vertically Stacked GAA MOSFET With Wrap-Around Contact," in IEEE Transactions on Electron Devices, vol. 69, no. 3, pp. 910-914, March 2022. doi: 10.1109/TED.2022.3140283.

[6] S. J. Kang, J. H. Kim, Y. S. Song, S. Go and S. Kim, "Investigation of Self-Heating Effects in Vertically Stacked GAA MOSFET With Wrap-Around Contact," in IEEE Transactions on Electron Devices, vol. 69, no. 3, pp. 910-914, March 2022. doi: 10.1109/TED.2022.3140283.

[7] W. Ahn et al., "A Predictive Model for IC Self-Heating Based on Effective Medium and Image Charge Theories and Its Implications for Interconnect and Transistor Reliability," in IEEE Transactions on Electron Devices, vol. 64, no. 9, pp. 3555-3562, Sept. 2017, doi: 10.1109/TED.2017.2725742.
[8] C. -C. Chung, H. H. Lin, W. K. Wan, M. . -T. Yang and C. W. Liu, "Thermal SPICE Modeling of FinFET and BEOL Considering Frequency-Dependent Transient Response, 3-D Heat Flow, Boundary/Alloy Scattering, and Interfacial Thermal Resistance," in IEEE Transactions on Electron Devices, vol. 66, no. 6, pp. 2710-2714, June 2019, doi: 10.1109/TED.2019.2912426.
[9] S. Tyaginov et al., "Understanding and Modeling Opposite Impacts of Self-Heating on Hot-Carrier Degradation in n- and p-Channel Transistors," 2022 IEEE International Reliability Physics Symposium (IRPS), Dallas, TX, USA, 2022, pp. 6A.3-1-6A.3-8, doi: 10.1109/IRPS48227.2022.9764515.
[10] C. Gupta, A. Gupta, R. A. Vega, T. B. Hook and A. Dixit, "Impact of Hot-Carrier Degradation on Drain-Induced Barrier Lowering in Multifin SOI n-Channel FinFETs With Self-Heating," in IEEE Transactions on Electron Devices, vol. 67, no. 5, pp. 2208-2212, May 2020. doi: 10.1109/TED.2020.2977734.
[11] D. Son, K. Hong, H. Shim, S. Pae and H. Shin, "New Insight Into Negative Bias Temperature Instability Degradation During Self-Heating in Nanoscale Bulk FinFETs," in IEEE Electron Device Letters, vol. 40, no. 9, pp. 1354-1357, Sept. 2019. doi: 10.1109/LED.2019.2930077
[12] Z. Chbili and A. Kerber, "Self-heating impact on TDDB in bulk FinFET devices: Uniform vs Non-uniform Stress," 2016 IEEE International Integrated Reliability Workshop (IIRW), South Lake Tahoe, CA, USA, 2016, pp. 45-48. doi: 10.1109/IIRW.2016.7904898.
[13] O. Prakash, C. K. Dabhi, Y. S. Chauhan and H. Amrouch, "Transistor Self-Heating: The Rising Challenge for Semiconductor Testing," 2021 IEEE 39th VLSI Test Symposium (VTS), San Diego, CA, USA, 2021, pp. 1-7, doi: 10.1109/VTS50974.2021.9441002.
[14] C. Yan, Y. Ding, Y. Qu, L. Zhao and Y. Zhao, "Universal Hot Carrier Degradation Model under DC and AC Stresses," 2022 IEEE International Reliability Physics Symposium (IRPS), Dallas, TX, USA, 2022, pp. 7A.1-1-7A.1-6.
[15] W. Chen, Y. Li, L. Cai, P. Chang, G. Du and X. Liu, "Entire Bias Space Statistical Reliability Simulation By 3D-KMC Method and Its Application to the Reliability Assessment of Nanosheet FETs based Circuits," 2018 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 2018, pp. 33.5.1-33