Understanding the impact of polysilicon percolative conduction on 3D NAND variability

Salvatore Maria Amoroso
Synopsys Northern Europe, Ltd
Glasgow, G3 8HB UK
salvatore.amoroso@synopsys.com

Gerardo Malavena
Politecnico di Milano
Dipartimento Elettronica, Informazione e Bioingegneria,
Milan 20133, Italy
gerardo.malavena@polimi.it

Andrew R. Brown
Synopsys Northern Europe, Ltd
Glasgow, G3 8HB UK
andrew.brown@synopsys.com

Plamen Asenov
Synopsys Northern Europe, Ltd
Glasgow, G3 8HB UK
plamen.asenov@synopsys.com

Xi-Wei Lin
Synopsys, Inc
Sunnyvale, CA, USA
xiwei@synopsys.com

Victor Moroz
Synopsys, Inc
Sunnyvale, CA, USA
victor.moroz@synopsys.com

Mattia Giulianini
Politecnico di Milano
Dipartimento Elettronica, Informazione e Bioingegneria,
Milan 20133, Italy
mattia.giulianini@polimi.it

David Gianluigi Refaldi
Politecnico di Milano
Dipartimento Elettronica, Informazione e Bioingegneria,
Milan 20133, Italy
davidgianluigi.refaldi@polimi.it

Christian Monzio Compagnoni
Politecnico di Milano
Dipartimento Elettronica, Informazione e Bioingegneria,
Milan 20133, Italy
christian.monzio@polimi.it

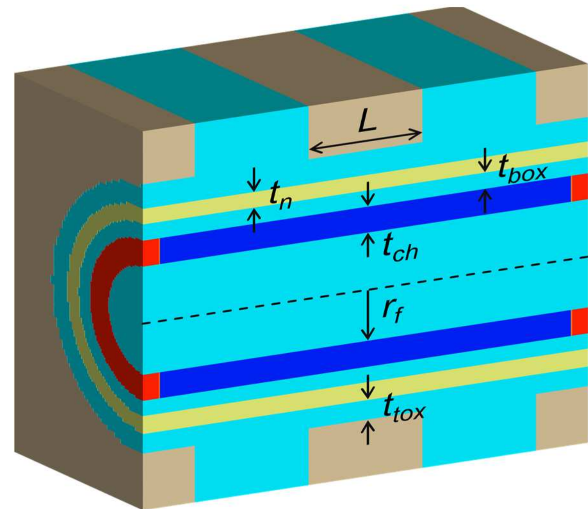
Alessandro Sottocornola Spinelli
Politecnico di Milano
Dipartimento Elettronica, Informazione e Bioingegneria,
Milan 20133, Italy
alessandro.spinelli@polimi.it

***Abstract*—In this work, by means of 3D TCAD simulations, we analyze the effects of the trap-induced percolative conduction in the polysilicon channels of 3D NAND memory cells. We demonstrate that the discrete nature of traps at polysilicon grain boundaries affects the memory cell threshold voltage and its fluctuation, as well as the random telegraph noise, with larger impact than is predicted by a continuous-trap approach. Our results highlight the importance of discrete-trap modeling for accurate variability prediction.**

Keywords—3D NAND, Memories, TCAD, Variability, Reliability, Random Telegraph Noise

I. Introduction

NAND memory technology has reached an unprecedented level of performance and scaling thanks to 3D stacking of cells, which is currently featuring more than 200 layers in a four-bit-per-cell technology [1-2]. This extraordinary increase in memory density brings with it stringent requirements to accurately control the variability and reliability affecting the electrical characteristics of billions of transistors. The statistical spread in device parameters comes from both geometric variations [3] and intrinsic fluctuations due to the polycrystalline nature of the vertical silicon channel [4]. In particular, numerical simulation has been used to investigate the spread of the threshold voltage (V_T) and random telegraph noise (RTN). However, simulations are usually carried out by adopting a continuous distribution of traps at the polysilicon grain boundaries, whereas the true discrete nature of the traps is expected to play a non-negligible role in the assessment of V_T and its fluctuations. Only a few works have, so far, adopted a discrete-trap approach [5-7], and a thorough comparison between continuous and discrete-trap methodologies is still missing. In this paper, we aim to present such a comparison and to highlight the importance of properly capturing the strong percolative nature of conduction induced by discrete random traps in 3D NANDs. In the next sections we will summarize our simulation methodology and assumptions and then will present our main simulation results and analysis in section III.



L	35 nm	r_f	20 nm
t_{ch}	10 nm	t_{box}	6 nm
t_n	6 nm	t_{tox}	8 nm

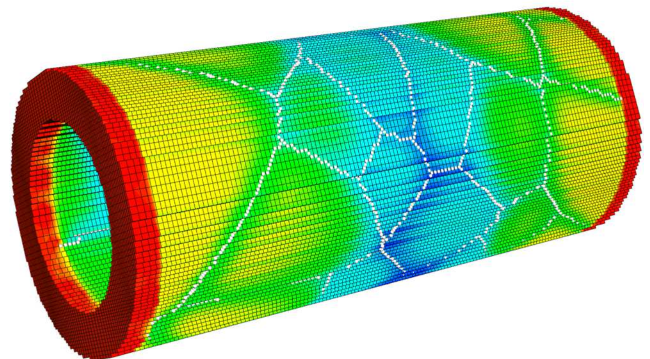


Figure 1: (Top) Schematic of the Macaroni device structure (red = highly-doped silicon; blue = polysilicon, light-blue = oxide, yellow = nitride, *brown* = WLs). (Middle) Relevant device parameters and values are listed in the table; (Bottom) Example of polysilicon channel grain structure generated with Garand VE.

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II. Simulation Methodology

We focus our analysis on a 3D NAND architecture, restricting our attention to a single cell. To correctly capture the fringing effects in the intercell regions, we also include one half-cell per side as illustrated in Figure 1. These neighbouring word lines are kept at V_{pass}=6V. The Macaroni-like cell [8] dimensions are listed in the table. To enable the statistical TCAD simulation of these NAND cells, we performed 3-D Monte Carlo simulations by using Sentaurus tools [9], [10] for processing the typical cell structure and Garand VE [11] for studying the statistical behaviour of the cell.

The stochastic nature of polycrystalline silicon is accounted for by means of random grains having average diameter Dg = 30 nm and with traps located at their grain boundaries (GB). An example of a polysilicon channel grain structure generated with Garand VE is also shown in Figure 1. This polysilicon channel granularity (PCG) is introduced in Garand VE through generation of random 3D grain patterns based on a 3D Laguerre-Voronoi pattern, where the specified average grain diameter determines the average number of grains. The actual number of grains generated in the structure will be taken randomly from a Poisson distribution whose expected value is the average number of grains.

A constant polysilicon/oxide acceptor-like interface state sheet density of 10^{11} cm^{-2} eV^{-1} has been here adopted. In the case of discrete traps, given this specified average trap sheet density and the total area of grain boundaries, the expected number of GB traps can be calculated, and likewise for the oxide interfaces. The actual number of traps on the grain boundaries and oxide interfaces are stochastically drawn from Poisson distributions given their calculated expected number.

The average GB trap energy distribution is taken from [12] and follows a double-exponential distribution. It has been demonstrated that such a distribution allows reproduction of experimental data [4]. The exact values of the parameters are, however, not significant for the scope of this work, where the comparison is carried out between a continuous-trap (CT) approach [4] and a discrete-trap (DT) approach [13] with the same assumed energy distribution. In the continuous case, the amount of trapped charge on a grain boundary is calculated by integrating the full energy distribution, with trap occupancy following a Fermi-Dirac distribution based on the local Fermi level. In the discrete trap case, each trap is assigned an energy level within the band gap taken randomly from the energy distribution, and the occupancy of each trap is calculated and updated during the simulation. The localized charge from each occupied discrete trap will then be captured by the simulation.

Carrier transport in the polysilicon channel is solved by means of the drift-diffusion equations with density-gradient corrections to account for quantum effects at the interfaces and in the Coulomb wells associated with the discrete charges. To focus on percolation and electrostatic effects, a low bitline bias of 50 mV and a constant mobility μ_n = 100 cm^2 V^{-1} s^{-1} are also adopted.

III. TCAD Simulation Results

We started our study by firstly comparing the impact of continuous traps (CT) and discrete traps (DT) on V_T variations. Further analysis of the impact of CT and DT on the random telegraph noise (RTN) variability was subsequently performed. The results of these analyses are presented in this section.

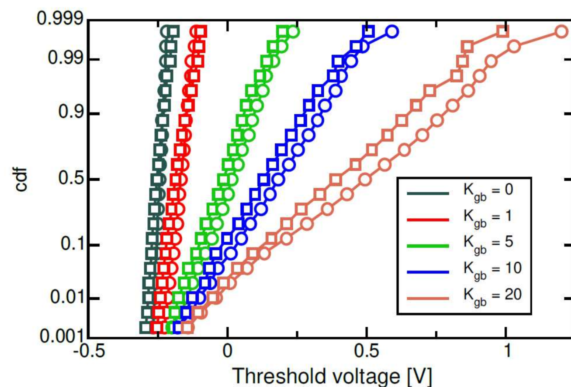

Figure 2: V_T CDF for different values of the GB trap density. Circles = CTs, squares = DTs.

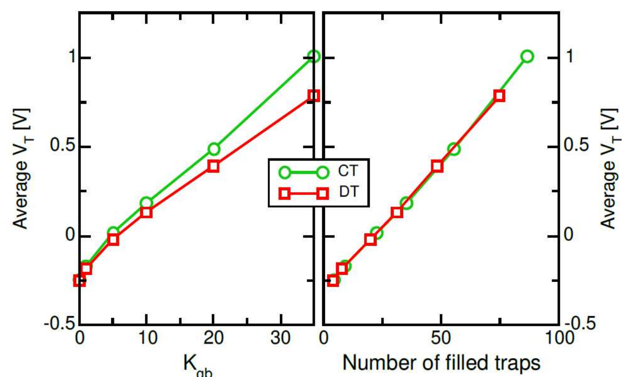

Figure 3: Average VT values as a function of the GB trap density (left) and average number of filled traps (right). Circles = CTs, squares = DTs.

A. *Threshold Voltage*

In all simulations, V_T is extracted at a constant current of 10 nA. Results for the V_T cumulative distribution function (CDF) are shown in Figure 2 for different grain boundary trap densities. Here we are scaling the nominal GB trap density by a factor K_{gb} and it is worth noting that, even if a very high trap density would result in the highest K_{gb} = 20 case, most states are close to the conduction band and remain empty, meaning that their actual density is not physically relevant. Figure 2 shows that CT and DT distributions have a similar trend with K_{gb}, increasing their average value and variance as the density increases. It should also be noted that the low probability part of the CDFs is barely affected by K_{gb}, because of the random grain generation: indeed, cells featuring zero GBs in the channel region, will exhibit a low V_T that is practically independent of K_{gb}. Note also that the DT approach consistently gives a lower V_T value, as one would expect from percolation theory. Figure 3 shows the average V_T as a function of K_{gb} (left) and the average number of occupied traps in the channel region N_T^{full} (right), for CT and DT cases. V_T trends overlap when plotted as a function of N_T^{full}, confirming that it is the smaller number of filled traps in the DT case that are responsible for the lower V_T. To understand the mechanism leading to this difference, we simulated an ideal cell with one GB placed completely across the macaroni structure at the mid-channel position.

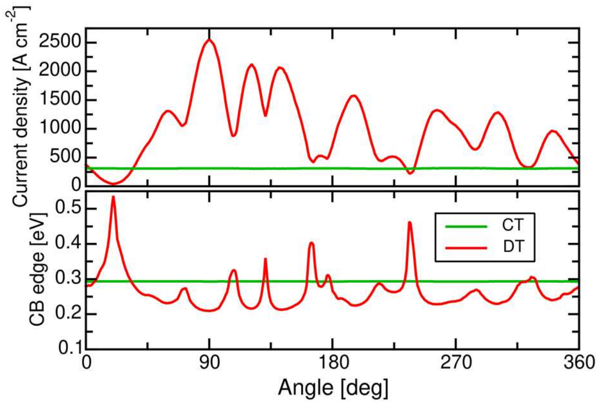

Figure 4: (Top) EC and current density at the middle of the polysilicon film as a function of the radial angle, for the CT and DT cases. (Bottom) 2D cutplanes from 3D simulation of the current densities at the GB for the CT (left) and DT (right) cases showing current percolation. The dashed line here illustrates the cutline along which the top graph is plotted.

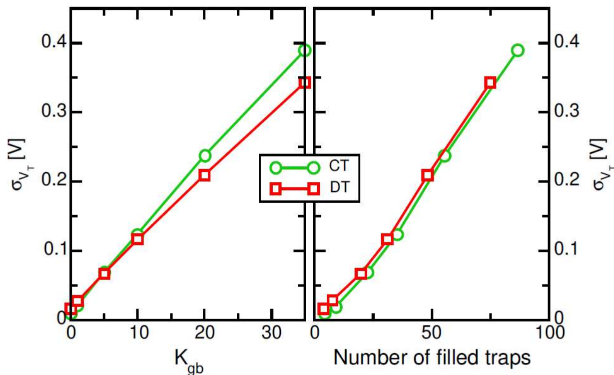

Figure 5: V_T statistical dispersion values as a function of the GB trap density (left) and average number of filled traps in the channel (right). Circles = CTs, squares = DTs.

Figure 4 shows results for conduction band edge (E_C) and current density at the GB position at the same WL bias, as a function of the rotation angle around the centre of the cylindrical structure. The cutline position and rotation is shown in the cross-sections below the graph. These cross-sections show the uniformity of the current density in the case of CT, and the non-uniformity of the current density in the case of DT.

While a uniform profile is obtained in the CT case, discrete filled traps give rise to 3D Coulomb peaks close to the negatively charged traps, leading to a non-uniform E_C profile. The current can more easily flow in the low-energy channels formed around the trap-induced peaks, which means more percolative conduction and more current, as shown by the

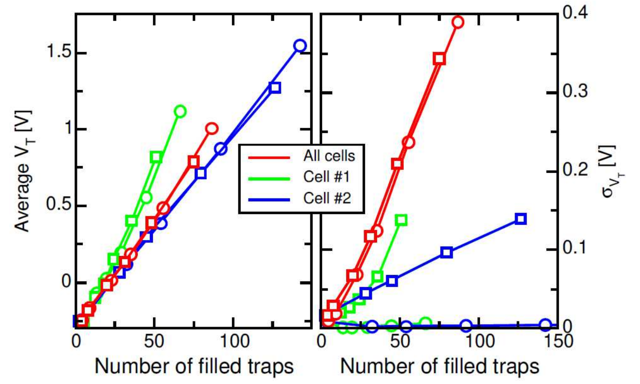

Figure 6: Average V_T (left) and σ_{VT} (right) as a function of N_T^{full}, considering also two cells with fixed GB configuration. Circles = CTs, squares = DTs.

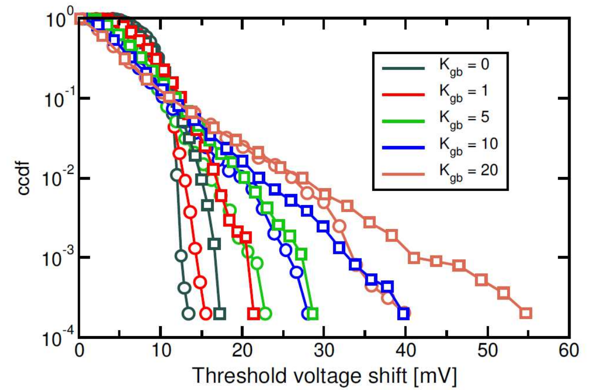

Figure 7: The CCDF of ΔV_T due to a single RTN trap being filled, for different values of the GB trap density. Circles = CTs, squares=DTs.

higher current density in those regions. This triggers a feedback mechanism, because a lower WL bias is needed to meet the constant-current V_T criterion in presence of a percolative conduction; lower gate bias translates in fewer occupied traps, N_T^{full}, and in turn less variability. We can, indeed, better understand the impact of trap discretization by looking at the V_T dispersion, σ_{VT} in Figure 5. Here we can see that σ_{VT} vs. K_{gb} is smaller in the DT case (left) but becomes slightly higher when reported as a function of N_T^{full} (right). This confirms that σ_{VT} is also related to the number of traps, as previously anticipated, and the higher DT value (at constant N_T^{full}) is due to the contribution of the randomness in the individual trap position.

To gain further insight on the impact of different sources of statistical variability, we have also run simulations for a few cells, each having fixed GB configuration, and only changing number and positions of the traps. The results are reported in Figure 6 showing that individual cells can have higher or lower V_T than the average. Also, their statistical spread is negligible in the CT case and it is interesting to highlight that even for the DT case we observe smaller than average dispersion. This result suggests that, for a given number of traps, σ_{VT} is mainly controlled by the stochastic dispersion of GB number and position.

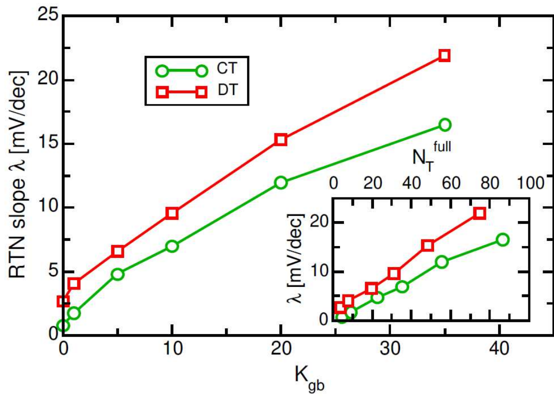

Figure 8: RTN slope λ as a function of the GB trap density and N_T^{full} (inset). Circles = CTs, squares = DTs.

B. Random Telegraph Noise

To evaluate the random telegraph noise (RTN) fluctuations, we have followed a similar approach as in [4]. We simulated the threshold voltage shift, ΔV_T, following the capture of an electron by a random trap. The trap can be located either at a GB or at one polysilicon/oxide interface. Results for the complementary CDF (CCDF) of ΔV_T for different K_{gb} values are reported in Figure 7. The exponential tail that is typically observed in the experimental data (see e.g. [14]) is clear in the simulation results. As expected, the (inverse) slope λ of this tail increases with K_{gb}. It is worth noting that larger ΔV_T values are reached in the DT case, highlighting again the importance of this approach. The trend of this slope vs K_{gb} is plotted in Figure 8, where we can fit a power-law with exponent ~0.62 for both CT and DT cases. The stronger impact of DT RTN is even more relevant considering the smaller number of filled traps in this case. In fact, when data is plotted as a function of N_T^{full} (see inset in Figure 8), a linear behaviour can be seen, with two different slopes (0.19 and 0.27 mV/dec for CTs and DTs, respectively). This result follows from the E_C and current density profiles depicted in Figure 4 where the DT approach results in a strongly non-uniform E_C and current density profile, leading to more percolation, i.e. smaller V_T but larger RTN fluctuations, as a strategic trap is more likely to shut off a region of the GB where the current is localized. In the CT case, instead, the RTN is mainly due to the randomness in the GB configuration. These results make clear that a DT approach is required for accurately assessing 3D NAND variability.

IV. Conclusions

In this paper we have studied the impact of discrete traps on 3-D NAND variability and compared it to the predictions obtained from a continuous-trap modelling approach. We have shown that the strong percolative conduction induced by random discrete polysilicon traps leads to lower average threshold voltage and its stochastic dispersion, but larger RTN fluctuations, when compared to a continuous-trap approach. This phenomenon has been analysed by extensive 3D TCAD statistical simulations and we have shown that the different electrostatics and fraction of occupied traps, as well as the stronger impact of a discrete charge on the NAND string percolative conduction are ruling the difference in prediction between continuous and discrete trap modelling. These findings highlight the importance of adopting a discrete-trap modelling approach for accurately assessing variability in modern NANDs.

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