Modeling Degradation and Breakdown in SiO_2 and High-k Gate Dielectrics

Andrea Padovani
Engineering Department "Enzo Ferrari" (DIEF)
University of Modena and Reggio Emilia
Reggio Emilia, Italy
andrea.padovani@unimore.it
ORCID: 0000-0003-1145-5257

Paolo La Torraca
Department of Sciences and Methods for Engineering (DISMI)
University of Modena and Reggio Emilia
Reggio Emilia, Italy
ORCID: 0000-0003-4852-4623

Luca Larcher
MDLx Italy
Applied Materials
Reggio Emilia, Italy
ORCID: 0000-0002-9139-349X

Jack Strand
Department of Physics and Astronomy
University of College London
London, UK
ORCID: 0000-0002-4603-6151

Alexander Shluger
Department of Physics and Astronomy
University of College London
London, UK
ORCID: 0000-0002-2488-0896

***Abstract*— We present a multiscale device simulation framework for modeling degradation and breakdown (BD) of gate dielectric stacks. It relies on an accurate, material-dependent description of the most relevant defect-related phenomena in dielectrics (charge trapping and transport, atomic species generation), and self-consistently models all degradation phases within the same physics-based description: stress-induced leakage current (SILC), soft (SBD), progressive (PBD) and hard breakdown (HBD). This methodology is applied to understand several key aspects related to the reliability of SiO_2 and high-k (HK) gate dielectrics: i) characterization and role of defects responsible for the charge transport in fresh and stressed devices (SILC); ii) the differences observed in the SILC behavior of nMOS and pMOS transistors; iii) the degradation of bilayer SiO_x/HfO_2 stacks; and iv) the voltage dependence of the time-dependent dielectric breakdown (TDDB) distribution.**

Keywords*— *Dielectric degradation, dielectric breakdown, TDDB, Ginestra®, stress-induced leakage currents (SILC).

I. Introduction

Dielectric degradation and breakdown (BD) are strongly affecting the reliability of logic devices. Despite the vast research efforts made so far, many experimental trends and observations have still not been fully understood and explained. The adoption of 3D geometries (FinFET, GAA, Nanosheet) [1] and new materials [2] further complicated the scenario. Nonetheless, achieving a comprehensive and self-consistent description of many different aspects concerning dielectric degradation (nMOS vs. pMOS BD dynamics, bilayer dielectric stacks, voltage/field dependence, etc.) is mandatory for reliable interpretation of experiments and correct assessment and prediction of device lifetime. Achieving this requires accurate models of defect processes.

In this paper, we present a physics-based simulation framework, implemented in the Ginestra® software [3], that provides a comprehensive and self-consistent solution for the modeling of degradation and breakdown in gate dielectric stacks. This methodology is applied to investigate stress-induced leakage currents (SILC) in both nMOS and pMOS devices, model the dielectric degradation – from SILC to hard BD (HBD) in SiO_2 and SiO_x/HfO_2 dielectrics, and to understand the different voltage dependencies (power law, E-model, etc.) exhibited by experimental time-dependent dielectric breakdown (TDDB) distributions.

This work has been partially supported by the FAR 2022-2023 project of the "Enzo Ferrari" Engineering Department of the University of Modena and Reggio Emilia, Italy.

II. The Multi-Scale Modeling Framework

Simulations of dielectric degradation and BD in SiO_2 and high-k (HK) gate oxides are performed using the Ginestra® commercial software [3], a multi-scale simulation platform that self-consistently describes all the main physical mechanisms occurring in dielectric layers subjected to electrical stress: charge trapping and transport, increase of the local power dissipation, temperature, and field, breaking of interatomic bonds promoted by field, temperature, and carrier injection. This enables the simulation of stress-induced degradation and BD in single and multi-layer stacks [4]-[8]. TDDB simulations are performed considering statistically different time-zero devices (in terms of energy, location and character of distribution of pre-existing defects) and accounting for the randomness of the defect generation process through the kinetic Monte Carlo method [9].

Transport of carriers through the dielectric(s) includes both *intrinsic* (direct/Fowler-Nordheim tunneling, thermionic emission, drift) and *defect-assisted* mechanisms. The latter are implemented in the framework of the multi-phonon trap-assisted tunneling (TAT) theory [10], [11], that has been found to dominate electrical conduction in a wide variety of materials [10], [12]-[16]. It provides a defect-centric description relying on two key parameters connected to the atomic structure of the trap, the thermal ionization, E_T, and relaxation, E_{REL}, energies [10], [17], [18]. In highly degraded oxides, the model accounts for a change in the dominant conduction mechanism from TAT to drift [5], associated with the presence of high defect density (~10^{21} cm^{-3}). The total current is computed including all of the discussed transport mechanisms simultaneously, while considering the local potential (defined by the applied bias, defect charge states and occupations and the internal redistribution due to the presence of breakdown spots with a quasi-metallic or semiconducting nature) and the local temperature (accounting for the power dissipation associated with the charge transport).

The stress-induced creation of new defects is described using an effective-energy description formalism [19]-[21] where the temperature (T) and field (F) dependent defect generation rate G is written as:

$$G = R\exp\left(-\frac{E_A - p_0\frac{2+k}{3}F}{k_B T}\right), \quad (1)$$

where R is the specific frequency of the generation process, E_A is the zero-field bond-breaking activation energy, p_0 the effective process dipole moment, k is the relative dielectric

XXX-X-XXXX-XXXX-X/XX/$XX.00 ©20XX IEEE

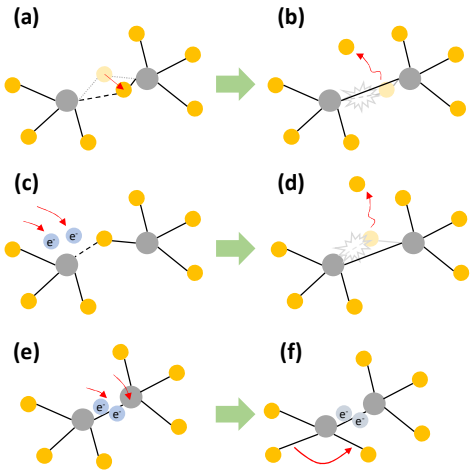

Figure 1. Schematic representation of different mechanisms involved in dielectric degradation: i) field-driven (a) bond stretching and (b) breaking (thermochemical model [McPherson2003]); ii) (c) double electron trapping at precursor site with subsequent weakening and (d) breaking of the adjacent bond (carrier injection model [Padovani2023]); iii) (e) double electron trapping at an existing trap and (f) subsequent formation of a new precursor (for example, due to local lattice distortion).

constant, and k_B is the Boltzmann's constant. Equation (1) allows to model different degradation mechanisms, from the simpler thermochemical bond-breaking process [19], Fig. 1(a)-(b), to the more complex microscopic processes involving bond weakening induced by an injection and trapping of carriers by pre-existing defects (precursors) [5], [7], [8]), Fig. 1(c)-(d). Equation (1) is also used to model the formation of new precursor defects [7], [8], Fig. 1(e)-(f). We should note that a comprehensive understanding and explanation of dielectric degradation and BD (including experimental trends and observations [22]) cannot be achieved without the adoption of an advanced microscopic model based on defect creation assisted by carrier injection and trapping (the Carrier Injection (CI) model, see Fig. 1(c)-(f) [8]). The simplified approach relying on the thermochemical formalism, in which E_A and b in eq. (1) are considered as phenomenological parameters can be (and have been) used to understand degradation dynamics and explain important BD behaviors [6], [15], but lack the mechanistic insight. The proposed multi-scale simulation framework is therefore tightly connected to ab-initio modeling that provides physically sound values of the various material-related parameters of trap-assisted transport (E_T, E_{REL}) and degradation (E_A, p_0) [5], [7], [23]-[25]. These parameters can also be extracted from experimental data [10], [26], [27].

III. Stress-Induced Leakage Currents

Using the proposed framework to reproduce experimental gate leakage currents is a very effective way to identify and characterize the traps responsible for the charge transport through the gate dielectric stack [10] in both fresh and stressed devices. Figure 2 shows the excellent agreement between the gate leakage currents measured and simulated as a function of the temperature on unstressed nMOSFET capacitors having a high-k gate dielectric stack comprised of a 1.1nm-thick SiO_x interfacial layer (IL) and either a 3nm-thick or a 5nm-thick HfO_2. The simulation results indicate that neutral oxygen vacancies (V^0) in the IL (E_T=2.2-3.1eV; E_{REL}=0.36eV) and positively charged oxygen vacancies (V^+) in HK (E_T=1.7-2.7eV; E_{REL}=1.19eV) are responsible for the gate current, respectively, in thin and thick stacks [10]. The different nature

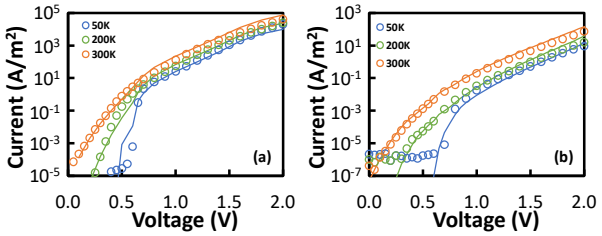

Figure 2. Gate leakage currents (symbols) measured and (lines) simulated as a function of the temperature on nMOSFET capacitors with (a) a 1.1nm/3nm and (b) a 1.1nm/5nm SiO_x/HfO_2 gate dielectric stack.

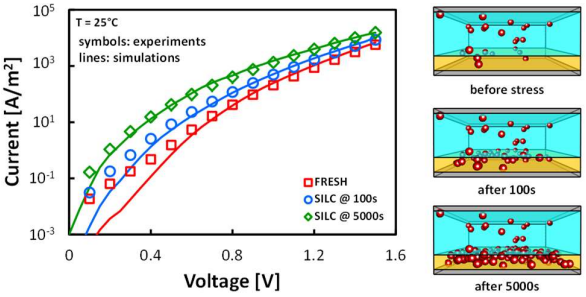

Figure 3. Stress-induced leakage currents (symbols) measured and (lines) simulated during CVS experiments at 3V and different stress times on a nMOSCAP device with a 1.1nm/3nm SiO_x/HfO_2 gate dielectric stack. Cartoons on the right show the evolution of the oxygen vacancies distribution (red spheres) as obtained from the simulation of the CVS.

of the traps assisting the charge transport in the two devices is in agreement with the different dependence of the gate current on temperature, which is controlled by the multi-phonon transitions [10]. It is also worth noting that the density of IL traps is significantly higher (of the order of 10^{19} cm^{-3}) than in a high-quality SiO_2 film, as a consequence of its interaction with the overlying HfO_2 layer [28], [29].

The results just discussed identified SiO_x V^0 traps as the major contributor to the gate leakage current for the thinner 1.1nm/3nm SiO_x/HfO_2 high-k dielectric stack. We now use these important results, together with the modeling of stress-induced trap generation, to investigate the degradation of this dielectric stack. Figure 3 shows the evolution of the gate current measured and simulated at different stress times during a constant voltage stress (CVS) experiment performed at V_G=3V and room temperature on the same 1.1nm/3nm SiO_x/HfO_2 nMOS capacitor as in Fig. 2(a). Simulations of the degradation process show that the electrical stress leads to the generation of traps in the SiO_x IL (cartoons in Fig. 3). Such an increase of IL traps with stress time allows to nicely reproduce the significant increase in the current (SILC) [30], [31].

Simulations also allow us to understand and to explain the different SILC behavior exhibited by high-k/metal gate nMOS and pMOS transistors under CVS. Different groups have reported that, while the breakdown of a nMOS device is preceded by a significant SILC increase [similar to the one in Fig. 2(a)], no (or very limited) SILC is typically observed in a pMOS device before BD [32], [33]. Figure 4 shows the results of CVS simulations performed on nMOS and pMOS devices having the same 0.7nm/1.5nm SiO_x/HfO_2 high-k dielectric stack. As can be seen, the gate current of the nMOS as a function of the stress time shows a clear increase (SILC) before breakdown, Fig. 4(a), which is not present in the case of pMOS, Fig. 4(b). This behavior, which is fully consistent with the reported experiments [32], [33], also correlates with the degradation dynamics and with the nature of the traps

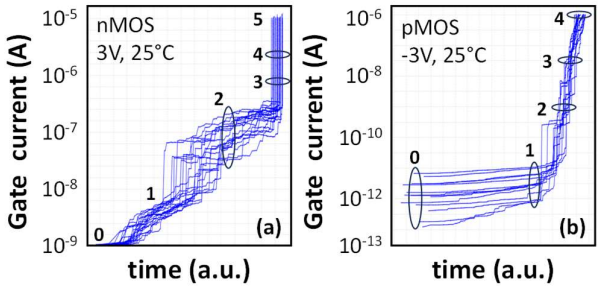

Figure 4. Evolution of the gate leakage currents as obtained from the statistical simulation of CVS experiments on (a) nMOS and (b) pMOS capacitors with a 0.7nm/1.5nm SiO_x/HfO_2 gate dielectric stack. The numbers identify subsequent instant of the degradation, whose IV characteristics and oxygen vacancies distributions are shown in Fig. 6 (for a single device).

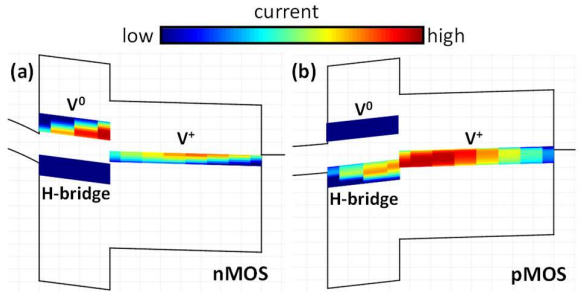

Figure 5. Band diagram of the 0.7nm/1.5nm SiO_x/HfO_2 gate dielectric stack (a) nMOS and (b) pMOS devices respectively at positive and negative voltages. The distribution of V^0, V^+ and Hydrogen-bridge traps extracted by reproducing experimental data (not shown) are also reported and colored depending on the amount of the driven current.

assisting the conduction through the stack. In this respect, Fig. 5 shows that the current flowing through the high-k stack is controlled mainly by IL V^0 in the nMOS under positive voltages, Fig. 5(a), and by HfO_2 V^+ in the pMOS under negative voltages, Fig. 5(b) (note that these conditions are the same as for the CVS in Fig. 4). This, together with the fact that the electrical stress induces the formation of oxygen vacancies in the IL (see Fig. 3), well explains the different SILC behavior exhibited by nMOS and pMOS devices under CVS. This can be better understood by looking at the simulation results in Fig. 6. In the case of the nMOS device, Fig. 6(a), the gate current increases as soon as oxygen vacancies start to be generated in the IL due to the applied electrical stress [see IV characteristics 1, 2 and the corresponding VO distributions in Fig. 6(a)]. Such rapid SILC increase, observable also in Fig. 4(a), is a direct consequence of the dominant current contribution provided by the oxygen vacancies in the IL, see Fig. 5(a). On the other hand, the same defects do not assist the charge transport in the case of a pMOS device under a negative V_G, whose current is mostly controlled by HfO_2 oxygen vacancies and, to a much lesser extent, by H-related defects (e.g. H-bridges), Fig. 5(b). As a consequence, no significant current increase is observed when new VOs are generated in the IL, see IV characteristic 1 and the corresponding VO distributions in Fig. 6(b), and Fig. 4(b). As shown in Figs. 4(b) and 6(b), the current starts to increase (abruptly) only when the IL is broken and traps start to be generated in the overlying high-k (IV characteristics 2, 3, 4 and the corresponding VO distributions in Fig. 6(b)). Note that at this stage the device is already in the runaway phase leading to HBD, Fig. 4(b). Finally, it must be mentioned that a minor SILC increase could be observed even in pMOS under negative CVS if some of the generated IL vacancies are converted into H-related traps [34]-[36], since these defects provide a (minor) contribution to the current, see Fig. 5(b).

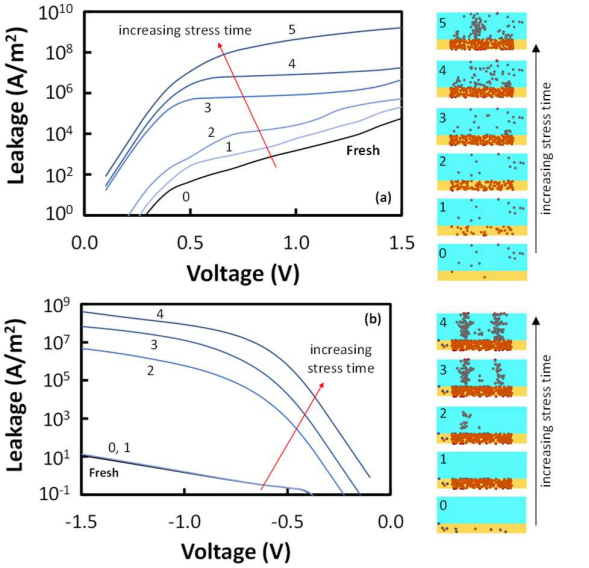

Figure 6. Evolution of the gate currents during the simulated CVS in Fig. 4 for one of the considered (a) nMOS and (b) pMOS devices. 2D visualizations of the IL/HK stack representing subsequent snapshots of the simulated evolution of the oxygen vacancies distribution (red spheres) are shown on the right. Each snapshot is numbered according to the corresponding I-V characteristic for increasing stress times as in Fig. 4 (0: fresh; 4/5: HBD).

The simulation results consistently explain also the differences observed between the SILC measured in both nMOS and pMOS devices under inversion and accumulation conditions (not shown) [33].

IV. Towards a Universal BD Model

The key parameter used to assess gate oxide reliability is the time-dependent dielectric breakdown [37], whose characterization is typically done under field-accelerated and/or temperature-accelerated conditions. The collected experimental data are then used to extrapolate the device lifetime under operating conditions, a critical step that strongly depends on the adopted model [8], [37]-[39] (among the many proposed in the literature, such as the E-model [19], [20], the power-law model [40], [41], the 1/E model [42], [43], etc.). Here, we briefly describe a new microscopic degradation model that has demonstrated the potential to reconcile the earlier BD theories/models within a unique physics-based framework. It is based on the CI model, Fig. 1, and stems from recent findings highlighting the role of structural precursors in facilitating the bond-breaking process leading to the dielectric breakdown [5], [7], [8], [23], [44]. It has been implemented in the Ginestra® platform through the effective-energy description formalism discussed in Section II.

The CI model relies on four key material-dependent processes shown in Fig. 1(c)-(f): the two-electron trapping into a precursor defect, Fig. 1(c); ii) the breaking of the adjacent weakened bond and the formation of O vacancy and interstitial $O^=$ ion, Fig. 1(d), iii) an additional process leading to the formation of new precursors, Figs. 1(e)-(f), and iv) multi-phonon electron tunneling through the formed neutral O vacancies. Within this model, the term R in eq. (1) includes the probability for the precursor site to be occupied by two electrons, which is calculated using the multi-phonon theory while considering all possible electron trapping/de-trapping transitions (trap-trap, trap-band, trap-electrode) [8]. Here we focus on the specific case of SiO_2, but the model has already been adopted to HfO_2 [7] and Al_2O_3 [45].

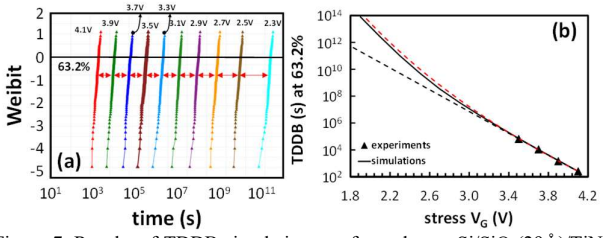

Figure 7. Results of TDDB simulations performed on a Si/SiO_2(29Å)/TiN stack with stress voltages between 2.3V and 4.1V. (a) TDDB Weibull plots. (b) 63.2% TDDB versus the stress voltage as extracted from (b). Black and red dashed lines respectively represent results obtained with classical thermochemical equation and power law extrapolation (for comparison purposes). 100 randomly generated devices are considered for every stress condition. Experimental data (symbols) are taken from [46].

Figure 7 shows the results of the statistical TDDB simulations performed using the proposed model on a MOS capacitor with a 29 Å-thick SiO_2 dielectric for stress voltages from 2.3V to 4.1V [8]. The simulated TDDB distributions are characterized by the same Weibull slope, but an increasing spacing in time between them is observed at the lower stress voltages (red arrows in Fig. 7(a)). When the 63.2% TDDB is extracted and plotted versus the stress voltage, Fig. 7(b), this translates into a deviation from the trend of the pure thermochemical (TC) model (dashed black line) towards a power-law (PL) dependence (dashed red line). This is a direct consequence of the electron injection contribution captured by the prefactor R in eq. (1), that determines a voltage-dependent modulation of the oxygen vacancy generation rate associated with the voltage-dependent probability of precursors to capture two electrons [8]. These findings have important implications for the explanation and interpretation of many – sometimes contradicting – experimental TDDB vs. V_G trends reported in the literature. In fact, the proposed CI BD model not only reconciles TC and PL theories, but also provides a theoretical description that can explain why the BD, even for the same material, can exhibit different voltage dependencies. It is the type of precursor defect (tightly connected to material properties and process conditions) that determines, through its E_T and E_{REL} properties, the shape of the TDDB vs. V_G plot, as well as whether, how and at what voltage deviation from the E-dependence occurs (not shown) [8].

Figure 8 shows the 2D maps of the evolution of the distributions of precursors and oxygen vacancies and of the current they drive, as obtained from the simulation of one of the 2.9nm-thick SiO_2 devices in Fig. 7 at 300K for a stress voltage of 4.1V. The generation of the initial oxygen vacancies brings the device in the SILC stage, characterized by uniform oxygen vacancies and current distributions, Fig. 8(a),(d), the latter driven primarily by oxygen vacancies. As more vacancies are generated, the device enters the soft/progressive BD stage (SBD/PBD), characterized by the formation of one or more spots with a higher local concentration of vacancies that sustain a larger current with respect to the rest of the device, dashed circles in Fig. 8(e). One of these local vacancy clusters is the seed of the final BD spot [dashed circle in Fig. 8(f)]: its higher current increases locally the power dissipation and temperature (not shown), which triggers, together with local field variations, a thermally driven positive feedback that eventually leads to the hard breakdown. This condition is characterized by the presence of a dominant BD spot that drives almost all the current, Figs. 8(c), (f). The degradation process is sustained by the generation of additional precursors through the mechanism in Fig. 1(e)-(f).

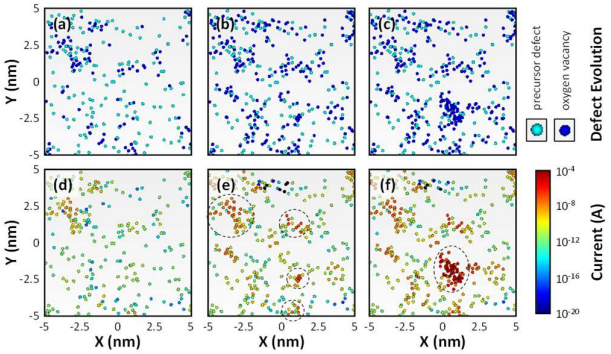

Figure 8. 2D map (X, Y plane) of the evolution of (a)-(c) distribution of precursors and oxygen vacancies (cyan and blue spheres, respectively) and (d)-(f) current driven by precursors and VO traps. All maps are shown for subsequent phases of the degradation process: SILC, SBD/PBD, and HBD (from left to right – the initial fresh state is not shown) as simulated at 300K with a stress voltage of 4.1V on the 29Å-thick SiO_2 film of Fig. 7.

V. Conclusions

We presented a multiscale device simulation framework for the modeling of the degradation and breakdown (BD) of gate dielectric stacks. The framework is applied to the investigation of stress-induced leakage currents (SILC) in nMOS and pMOS devices and can easily extend to 3D gate all-around transistors as well, to the modeling of dielectric degradation in SiO_2 and SiO_x/HfO_2 dielectrics, and to the understanding of the different voltage dependencies (power law, E-model, etc.) exhibited by experimental TDDB data.

References

[1] H.-J. Lee *et al.*, DOI: https://doi.org/10.1109/IEDM.2018.8614490.
[2] R. Chau *et al.*, DOI: https://doi.org/10.1109/LED.2004.828570.
[3] Applied Materials Ginestra®. https://www.appliedmaterials.com/eu/en/semiconductor/ginestra-software.html
[4] L. Larcher *et al.*, DOI: https://doi.org/10.1007/s10825-013-0526-z.
[5] A. Padovani *et al.*, DOI: https://doi.org/10.1063/1.4979915.
[6] A. Padovani and L. Larcher, DOI: https://doi.org/10.1109/IRPS.2018.8353552.
[7] J. Strand, *et al.*, DOI: https://doi.org/10.1063/5.0083189.
[8] A. Padovani *et al.*, DOI: https://doi.org/10.1109/IRPS48203.2023.10117846.
[9] L. Vandelli *et al.*, DOI: https://doi.org/10.1109/TED.2013.2255104.
[10] L. Vandelli *et al.*, DOI: https://doi.org/10.1109/TED.2011.2158825.
[11] M. Zhang *et al.*, DOI: https://doi.org/10.1063/1.3662195.
[12] G. Jegert *et al.*, DOI: https://doi.org/10.1109/TED.2010.2090158.
[13] K. A. Nasyrov and V. A. Gritsenko. DOI: https://doi.org/10.1063/1.3587452.
[14] A. Padovani *et al.*, DOI: https://doi.org/10.1109/TED.2019.2900030.
[15] P. La Torraca *et al.*, DOI: https://doi.org/10.1109/TED.2022.3172928.
[16] A. Slassi *et al.*, DOI: https://doi.org/10.1002/aelm.202201224.
[17] K. Huang *et al.*, DOI: https://doi.org/10.1098/rspa.1950.0184.
[18] C. H. Henry, D. V. Lang, DOI: https://doi.org/10.1103/PhysRevB.15.989.
[19] J. W. McPherson *et al.*, DOI: https://doi.org/10.1063/1.1565180.
[20] J. W. McPherson *et al.*, DOI: https://doi.org/10.1063/1.368217.
[21] G. Bersuker *et al.*, DOI: https://doi.org/10.1016/S0026-2714(01)00120-2.
[22] E. Wu, DOI: https://doi.org/10.1109/TED.2019.2933612.
[23] D. Z. Gao *et al.*, DOI: https://doi.org/10.1109/IRPS.2018.8353602.
[24] D. Z. Gao *et al.*, DOI: https://doi.org/10.3389/fphy.2019.00043.
[25] J. W. Strand *et al.*, DOI: https://doi.org/10.1103/PhysRevB.102.014106.
[26] A. Padovani *et al.*, DOI: https://doi.org/10.1109/LED.2013.2251602.
[27] M. Alayan *et al.*, DOI: https://doi.org/10.1109/MDAT.2017.2682246.
[28] G. Bersuker *et al.*, DOI: https://doi.org/10.1063/1.2362905.
[29] D. Heh *et al.*, DOI: https://doi.org/10.1109/TED.2007.896371.
[30] A. Padovani *et al.*, DOI: https://doi.org/10.1109/LED.2013.2275182.
[31] G. Bersuker *et al.*, DOI: https://doi.org/10.1109/IEDM.2008.4796816.
[32] A. Kerber *et al.*, DOI: https://doi.org/10.1109/IRPS.2009.5173304.
[33] C. Prasad *et al.*, DOI: https://doi.org/10.1109/RELPHY.2008.4558979.
[34] P. E. Blochl and J. H. Stathis, DOI: https://doi.org/10.1103/PhysRevLett.83.372.
[35] W. Goes *et al.*, DOI: https://doi.org/10.1109/TDMR.2008.2005247.
[36] Y. Wimmer *et al.*, DOI: https://doi.org/10.1098/rspa.2016.0009.
[37] Ghetti, A. (2004). DOI: https://doi.org/10.1007/978-3-662-09432-7_6.
[38] R. Degraeve *et al.*, DOI: https://doi.org/10.1016/S0026-2714(99)00051-7.
[39] J. W. McPherson *et al.*, DOI: http://dx.doi.org/10.1016/j.microrel.2012.06.007.
[40] E. Miranda *et al.*, DOI: https://doi.org/10.1109/55.767093.
[41] E. Wu *et al.*, DOI: https://doi.org/10.1109/IEDM.2000.904375.
[42] I.-C. Chen *et al.*, DOI: https://doi.org/10.1109/T-ED.1985.21957.
[43] I.-C. Chen *et al.*, DOI: https://doi.org/10.1109/EDL.1986.26332.
[44] A.-M. El-Sayed *et al.*, DOI: https://doi.org/10.1016/j.mee.2013.03.027.
[45] in preparation
[46] E. Wu *et al.*, DOI: https://doi.org/10.1109/TED.2002.805606