Doped Channel SOI pMOS TCAD Description Including Floating Body Effects

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***Abstract*— In this work, we propose to investigate Silicon-on-Insulator (SOI) pMOS behavior modulation due to channel doping and its TCAD description. We first demonstrate channel doping variation due to the diffusion through the BOX and consumption during gate oxide formation. As the channel thickness is not so thin (T_{SI}=22nm), channel doping variation leads to different device operation from Fully Depleted (FD) to Partially Depleted (PD), going through an "in between" regime where Floating Body (FB) effects occurs. We finally propose TCAD methodology to account for channel doping variation in SOI pMOS.**

Keywords*— *SOI; TCAD; Floating Body Effects

I. Introduction

SOI devices are studied since decades for many applications: Partially-Depleted SOI devices with thick silicon film (>60nm) are used for RF-SOI applications [1] while Fully-Depleted-SOI devices with thin SOI film (<10nm) are used for RF, digital and more Moore applications [2-4]. Floating Body (FB) effects are known to occur in PD-SOI devices [5-6] and can be canceled by body contact [7-8] while FD-SOI device are immune to FB effects thanks to the thin SOI film. Recently, SOI device on thin BOX with relatively thin film (22nm) have been proposed to fulfill imager application requirements with 3D sequential integration [9], where SOI film doping can be used for Vt centering. The objective of this paper is to determine the operation of such a SOI device and to propose the corresponding TCAD description, accounting for the SOI film doping.

II. Device & TCAD Description

SOI pMOS is defined to fulfill imager applications requirements (V_{DD}=2.5V) [9]: SiO2-polysilicon gate, 22 nm silicon film thickness (T_{SI}), 25 nm buried oxide thickness (T_{BOX}), 5 nm SiO2 gate oxide grown by Rapid Thermal Oxidation (RTO) and a highly in-situ doped N-type Ground Plane (GP, Phosphorus, $2.10^{20}cm^{-3}$). To build high V_T devices, channel doping is performed with BF2 implantation for large dose variation (0 to $6.10^{13}cm^{-2}$) and gate length L varies from 0.15 to 1µm. TCAD is performed through process and device simulations. The complete process is simulated (Fig.1): channel implantation, gate formation (RTO and P-type polysilicon), LDD implantation, spacer formation and HDD implantation. Device simulations are then performed with Poisson equation, drift-diffusion, SRH recombination and ThinLayer(IALmob) model including HighFieldSaturation.

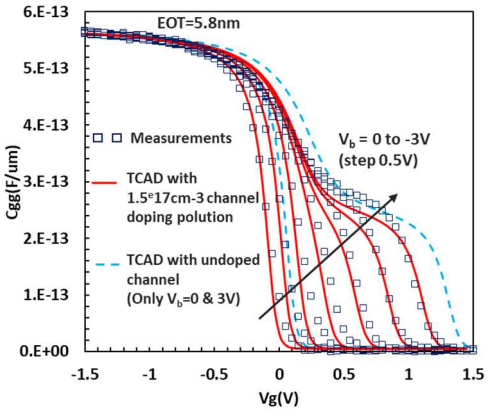

Fig. 1 : (C_{GG}-V_G) for V_b =0 to -3V from measurement and TCAD before and after tuning.

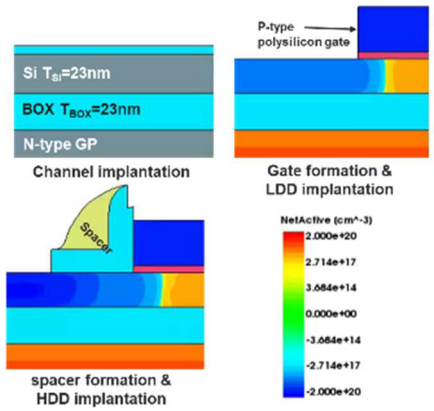

Fig. 2 : pMOS structure snapshots taken during TCAD process simulation

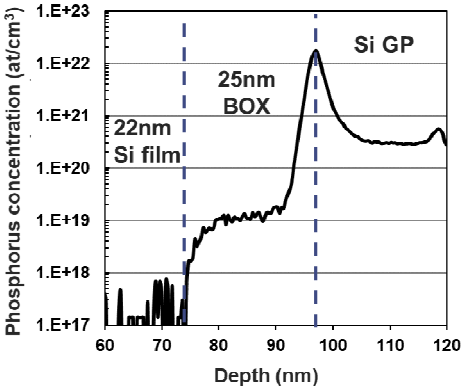

Fig. 3 : SIMS characteristic in the SOI substrate highlighting the phosphorus diffusion from the GP to the Si film.

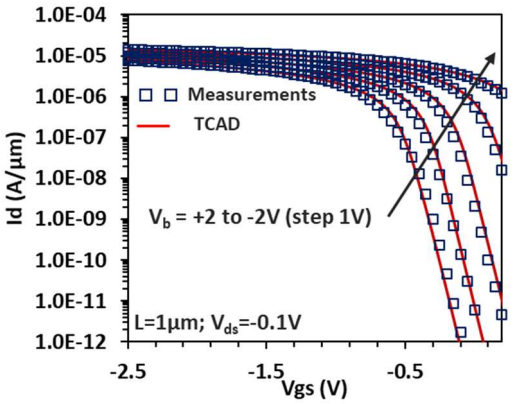

Fig. 4 : L=1µm pMOS I_d-V_g for V_b variation at V_d=-0.1V from TCAD and measurement.

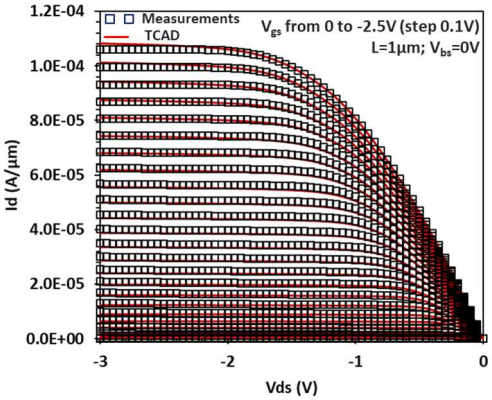

Fig. 5 : L=1µm pMOS I_d-V_d for V_g variation from 0 to -2.5V at V_b=0V from TCAD and measurement

III. Undoped Channel SOI pMOS TCAD validation

We first focus on long channel (L=1µm) undoped channel SOI pMOS. Gate capacitance with gate voltage characteristic (C_{gg}-V_g, Fig.2) highlight that strong inversion regime is well described but there is lower TCAD threshold voltage V_T at V_b=0 & 3V than measurement (dashed blue line). To increase TCAD V_T, higher N-type channel doping is necessary and cannot come from the implantation steps, which are all P-type. From Secondary Ion Mass Spectrometry (SIMS) measurement performed on SOI substrate (Fig.3), we

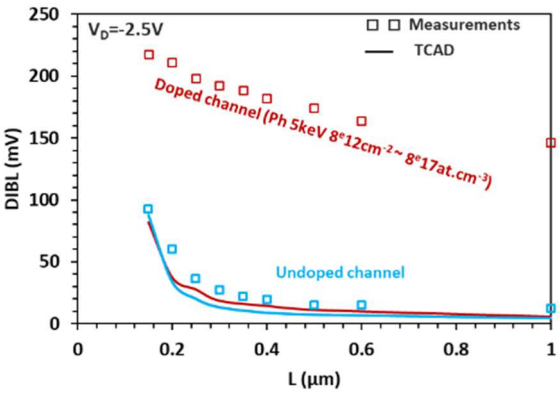

Fig. 7 : DIBL variation with gate length L for doped and undoped channel from TCAD and measurement

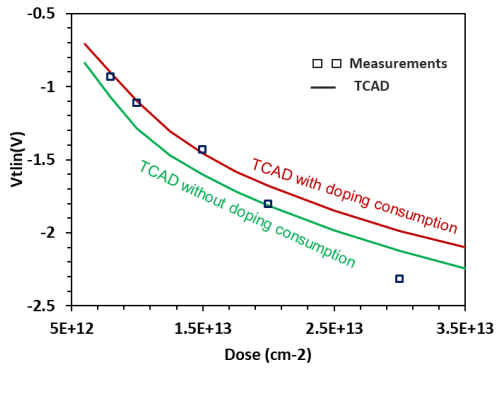

Fig. 8 : L=1µm V_{tlin} variation with Phosphorus implantation dose from measurement and TCAD

demonstrate that 1~4e17cm^{-3} Phosphorus diffused from the GP to the channel through the 25nm thick BOX. It is included in TCAD and C_{gg}-V_g for V_b variation is reproduced (red line on Fig.2), as well as long channel I_d-V_g at V_d=-0.1V for V_b variation & I_d-V_d at V_b=0V (Fig 4,5). The short channel TCAD description is then validated with DIBL variation versus gate length (Fig.6). An important DIBL degradation appears for doped channel, even for long gate and is not observed in TCAD.

IV. Doped Channel SOI pMOS TCAD Description

Linear regime threshold voltage V_{tlin} variation with channel implantation dose is overestimated by TCAD (green curve on Fig.7). SIMS (Fig.8) characterization reveals that as-implanted phosphorus profile in the 22nm silicon film is well predicted by TCAD (blue curves). However, it also highlights that the mean doping in the silicon film is significantly reduced after the gate oxide formation (Fig.8 dashed lines:~3.10^{18}cm^{-3} doping loss during the gate oxide formation). We attribute it to doping consumption in the surface during the oxidation and include it as a 3nm silicon etching in the process simulation. The phosphorus profile agreement between TCAD and SIMS is improved (Fig.8, red curves) as well as the V_{tlin} variation (red curve on Fig.7) up to phosphorus dose 1.5.10^{13}cm^{-2} and V_{tlin}=-1.5V. As the channel doping increases, the silicon depletion layer decreases and can be lower than the silicon film: the device

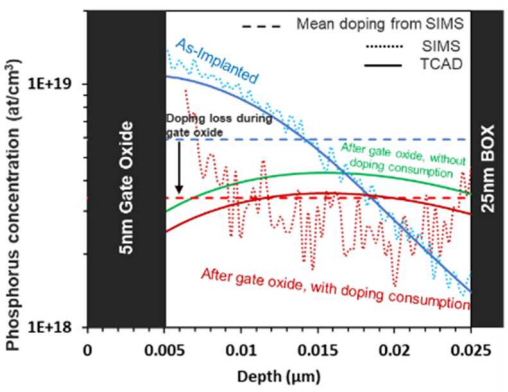

Fig. 6: as-implanted and after gate oxide phosphorus profile in the Si film comparison between SIMS and TCAD

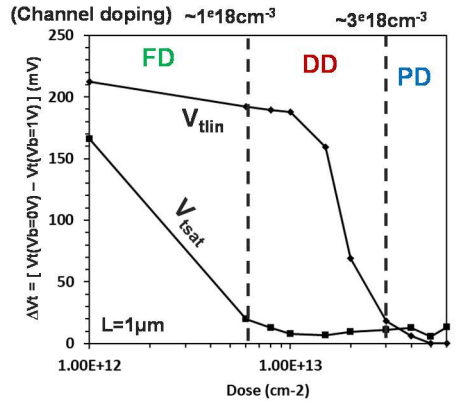

Fig. 9 : L=1µm pMOS V_{tlin} and V_{tsat} variation from V_B=0 to 1V_b as a function of the channel implantation dose. Channel doping from TCAD are provided.

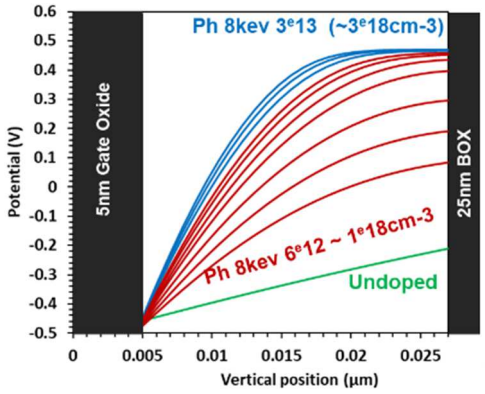

Fig. 10 : Potential variation in the Si film from the gate oxide to the BOX at V_G=V_{tlin} and V_D=-0.1V for several channel implantation dose.

operation can move from Fully Depleted (FD) to Partially Depleted (PD) operation. Because of the undepleted portion of the silicon film in PD operation, the ground plane bias (V_B) has no impact on V_T contrary to FD [2]. Fig.9 shows the measurement of the V_{tlin} dependency to V_B as a function of channel doping and demonstrates that PD operation starts around $3.10^{18}cm^{-3}$ channel doping. Same plot is performed with V_{tsat} (saturated regime V_T at V_D=-2.5V) shows that V_B impact is canceled for doping $>1.10^{18}cm^{-3}$. The channel doping range where V_{tlin} depends on the V_B and V_{tsat} doesn't depends on V_B defines the Dynamic Depleted (DD) operation where the device is FD in linear regime, and PD in saturated regime [10,11]. The potential variation at V_G=V_T and V_D=-0.1V in the Si film is shown on Fig.10 and highlights the difference between the 3 operating regimes: linear for FD, curved for
DD and curved with a constant portion close to the BOX for PD. With channel doping increase, the depleted layer controlled by the gate decreases, so the floating area is thicker. We then focused on TCAD description of device with V_T lower than -1.5V (FD and DD regimes).

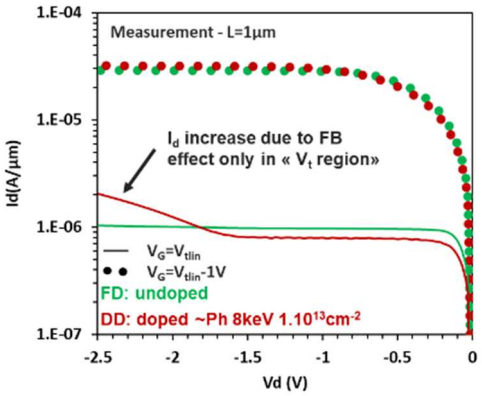

Fig. 11 : Measured I_d-V_d for L=1µm doped and undoped pMOS at V_G=V_{tlin} & V_G= V_{tlin}-1V

V. Floating Body Effects TCAD Description

In DD operation, Floating Body effects (FB) occur. As shown by I_d-V_d measurements (Fig.11), they produce a drain current increase at $|V_D|>1.5V$ only for V_G around V_T. This is due to the silicon floating area charged by Impact Ionization (II) at the drain [5]. For pMOS, it is charged with electrons: this negative charge reduces V_{tsat} and cancels the V_B impact on V_{tsat}: the long channel DIBL increases with channel doping because FB effects are worsened (Fig.12). To account for it in TCAD, II needs to be activated. DriftDiffusion simulations with default parameters leads to too high DIBL (blue on Fig.12). II is usually lower with hydrodynamic simulation [12] but DIBL is still too high. To reduce DIBL for long and doped channel, FB effect needs to be reduced. Two options are possible: reducing the II rate by a factor (II_{FACTOR}) or increase the recombination rate in the floating area with carrier lifetime reduction by a factor (τ_{FACTOR}). Note that is was demonstrated that carrier lifetime are shorter in thin film SOI than in bulk device (~10ns is 7nm Si film, [13]). Fig.13 shows the TCAD long channel DIBL variation for II_{FACTOR} and τ_{FACTOR} variations: in the following, we use (II_{FACTOR}= 0.01 and τ_{FACTOR}=0.2 (same value as [14]). With this TCAD improvement, DIBL variation with channel doping is reproduced (Fig.12). To

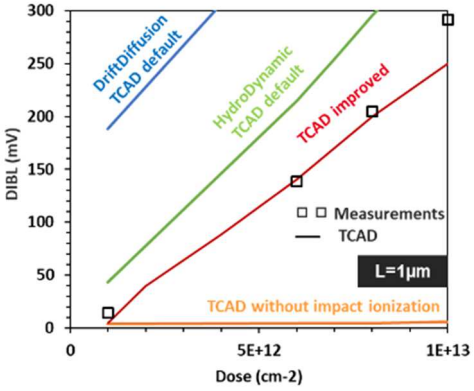

Fig. 12 : DIBL variation with the channel implantation dose from measurement and different TCAD settings.

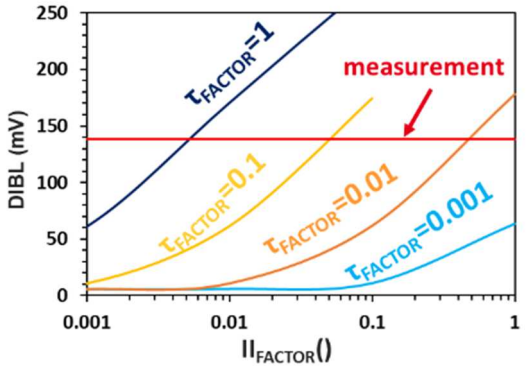

Fig. 13 : L=1µm DIBL variation with II_{FACTOR} for several τ_{FACTOR} at constant channel doping (Phosphorus dose $6.10^{12}cm^{-2}$) compare to measurement (red line)

observe FB effects, we need $|V_D|$>1.5V and channel doping needs to be $>1.10^{18}cm^{-3}$(Fig.14). It also shows floating area thickness increases with channel doping: the electrons stored increases,so the charge increases and the DIBL increases. Finally, Fig.15 shows the FB effects TCAD description improvement for various channel doping on I_d-V_d at V_g=V_{tlin}.

To highlight FB effects impact on the characteristic, drain current is normalized by its value at V_d=-1V, where there is

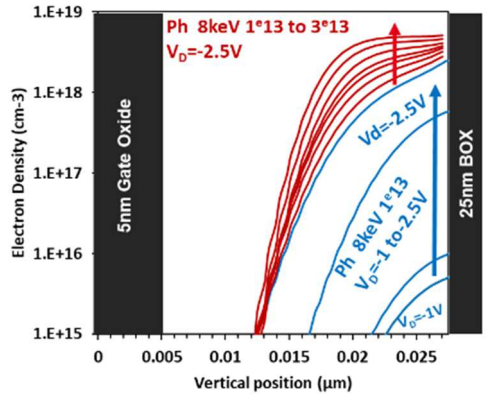

Fig. 14 : Electron density in the Si film at V_G=V_{tlin} from tuned TCAD for V_D and channel doping variation.

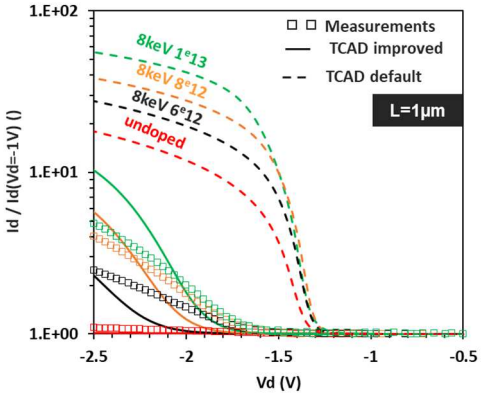

Fig. 15 : I_D-V_D normalized by $I_D(V_D$=-1V) at V_G=V_T at V_G=V_{tlin}, from measurement, defaut hydrodynamic TCAD and tuned TCAD for channel doping variation.

no FB effect. Our description can still be improved, but the channel doping impact is well captured.

VI. Conclusion

In this paper, we propose a TCAD description of 22nm thick SOI device including the floating body effect variation with channel doping. We highlight that large parameter variation is required to match the experimental long channel DIBL, but the modeling still needs to be improved to reproduce experimental I_DV_D characteristics.

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