SOI pMOS drain leakage understanding based on TCAD and measurements

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***Abstract*— This work investigates Silicon-on-Insulator (SOI) pMOS drain leakage current. 2D TCAD simulations with Schenk band-to-band tunneling and Field-Enhanced SRH generation recombination models reproduce experimental leakage for various biases and temperatures (25 to 125°C). Furthermore, we demonstrate that leakage variation with channel thickness is due to carrier lifetime variation. Experimentally, working on the lightly doped drain (LDD) to channel junction (position, steepness and dopants level) results in a leakage modulation for high electric field only. This behavior is perfectly reproduced by TCAD, enabling predictive work about leakage current optimization.**

***Keywords*— SOI; Leakage; TCAD simulation; Schenk Band-to-Band tunneling; SRH; GIDL;**

I. INTRODUCTION

Transistor leakage understanding is primordial for futures SOI technologies such as analog, SRAM [1] or CMOS image sensor [2]. For instance in [3], pixel false event generation is directly linked to transistor Gate Induced Drain Leakage (GIDL) current. It is widely acknowledged that the GIDL is attributed to band-to-band tunneling (BTBT) in the gate-to-drain overlap region due to strong electric field (>~$8x10^5$V/cm) [4,5]. However, Shockley-Read-Hall (SRH) generation and recombination mechanism is rarely considered, but in fact, dominates drain leakage for low electric field [6]. The dissociation between the two leakage mechanisms is primordial to enable GIDL optimization for a given device at a given operation point.

This work takes place in the continuity of ultra-low leakage measurements presented in [6] and exploits the developed measurement methodology. Thanks to temperature measurements, a V_{DS}-V_{GS} mapping of BTBT/SRH leakage mechanism predominance have been established taking the activation energy criteria $_{EA-25=>125°C}$=0.06eV. Experimentally, back biasing (V_B), silicon thickness (t_{si}) and channel doping modulates each leakage mechanism differently [6].

This paper proposes in depth understanding of SOI transistor leakage, combining TCAD and experimental measurements for various biases and temperatures ((V_{DS};V_{GS}); 25°C to 125°C).

II. LEAKAGE MECHANISM EXPERIMENTALLY IDENTIFIED ON SOI PMOS DEVICES

Fig. 1-a shows a TEM cross-section of the measured pMOS SOI devices. They feature a nominal silicon channel thickness (t_{Si}) of 23nm, 25nm buried oxide thickness (t_{BOX}), a 5.6nm Equivalent Oxide Thickness (EOT) and a SiO_2 polysilicon gate. The 5.6nm EOT ensures a low gate current explaining our focus on drain leakage.

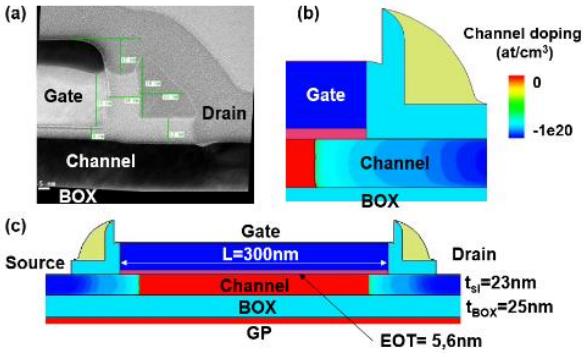

Fig. 1 : (a) TEM cross-section focalized on drain region. (b) TCAD structure reproducing TEM morphology (c) TCAD whole transistor.

All these characteristics are reproduced by Synopsys® process simulation (Fig. 1-b and 1-c). In particular, spacer morphology has been carefully reproduced to position LDD junction realistically.

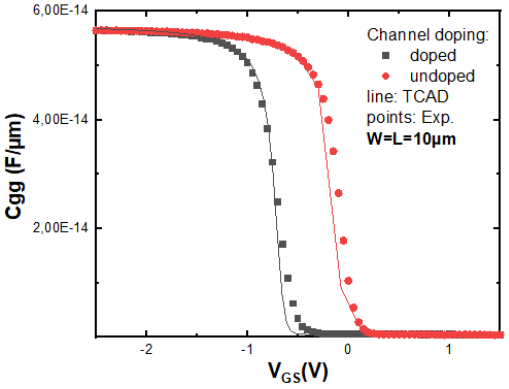

Fig. 2 : TCAD vs. Exp C_{GG} (F/µm) as a function of V_{GS} for both doped and undoped channel.

It has been shown that the parasitic transistor caused by mesa isolation [7] has no influence on drain leakage [6], supporting the choice of 2D TCAD simulations.

Classic 2D TCAD simulations were performed with Poisson equation, drift-diffusion and SRH recombination. CV measurements (Fig. 2) are well reproduced by TCAD for both undoped and doped channel, validating gate stack characteristics as well as channel doping. I_D-V_{DS} experimental behavior for undoped channel is correctly captured (Fig. 3), but TCAD leakage description need to be improved (green curve in Fig. 4).

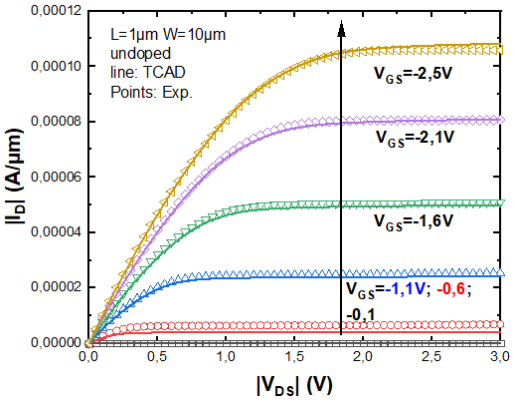

Fig. 3 : TCAD vs. Exp. I_D-V_{DS} for various V_G for undoped channel. TCAD reproduce well Exp. behavior.

III. TCAD DRAIN LEAKAGE MODEL SELECTION

To capture drain leakage behavior, several TCAD carriers generation models are investigated in this part. Firstly, we will focus on V_{DS}/V_{GS} variations and secondly on temperature behavior.

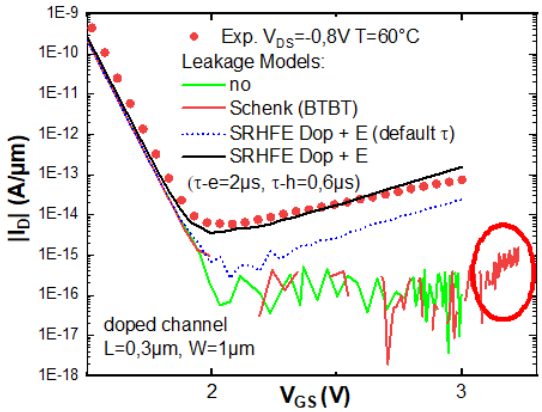

Fig. 4 : TCAD vs. Exp. I_D-V_{GS} at V_{DS}=-0.8V and 60°C for various TCAD model selection. Schenk BTBT tunneling model triggers for V_{GS}>3V.

A. *Drain leakage models selection*

We compare SOI pMOS drain leakage variation with V_{GS} (Fig. 4) and V_{DS} (Fig. 5) for both measurements (red symbols) and TCAD. For each TCAD curve color, only one generation mechanism is activated to dissociate the effects.

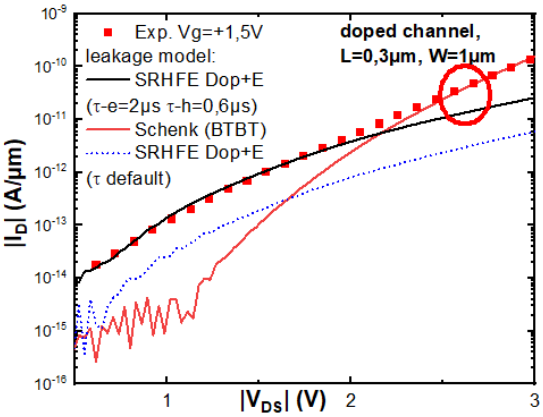

Fig. 5 : TCAD vs. Exp. I_D-V_{DS} at V_{GS}=+1.5V for various TCAD models. Schenk BTBT model is selected as well as Electric and Doping dependence for SRH.

If only BTBT Schenk model is activated (red curves), leakage triggers only for high V_{DS}-V_{GS} values, omitting a whole part of the curve. A screening between non-local path, Schenk and Hurkx BTBT models has been realized (not shown here) and Schenk model with default parameters (+local density correction) reproduced perfectly measurement in the BTBT predominance region. However, for low V_{DS}-V_{GS} values, BTBT Schenk model only underestimate leakage by two decades (see Fig. 4, red curve).

On the contrary, if SRH model with Field-Enhanced option (due to steep P-N junction at LDD-channel interface), Schenk lifetime and doping dependence is activated, TCAD drain leakage reproduces measurement behavior only for lower V_{DS} (dot blue curve). However, in this region, the total leakage current is still underestimated. Indeed, bulk carrier lifetime is considered (τe= 10µs and τh= 3µs) and not SOI value.

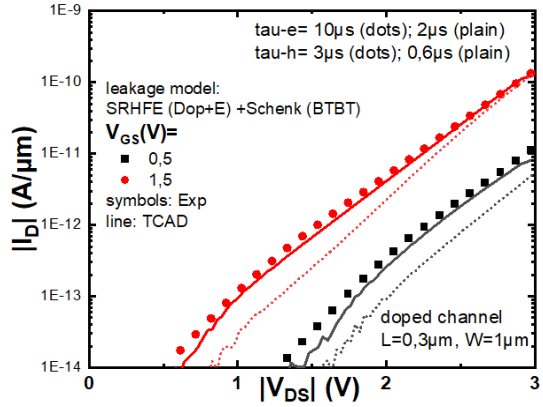

Fig. 6 : TCAD vs. Exp. I_D-V_{DS} for various V_{GS}: experimental data (symbols) vs. TCAD (line). Carrier lifetimes have been lowered down to match exp. data.

In literature, it is seen that carrier lifetime is reduced for SOI devices, being limited by silicon/insulator interfaces proximity (τ=0.01µs for t_{si}=7nm [8]), but we lack data for our Si film thickness. To reproduce drain leakage characteristics (Fig. 6), carriers lifetimes need to be reduced to τe= 2µs and τh= 0.6µs which is consistent with literature. Experimental data are perfectly reproduced for whole V_{DS}-V_{GS} range by the sum of BTBT and SRH contributions (red + black curve in Fig. 5 and Fig. 4 or plain curves in Fig. 6).

B. *Temperature measurements*

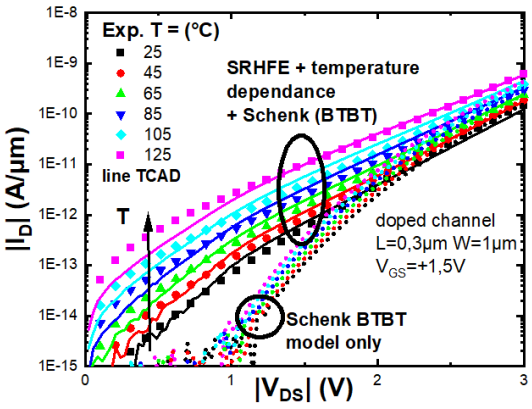

Fig. 7 : TCAD vs. Exp. I_D-V_{DS} at V_{GS}=+1.5V for various temperatures. A power law has been selected for SRH temperature dependence.

I_D-V_{DS} for V_{GS}=+1.5V and temperature varying from 25°C to 125°C are plotted in Fig. 7. From experimental data, one can observe that GIDL depends highly on temperature for lower $|V_{DS}|$ values. In fact, leakage temperature behavior results mainly from carrier lifetime temperature dependency, which can be modelled by a power law [9]. In addition to, there is a negligible component arising from BTBT mechanism (dots in Fig. 7, translation to the left for higher temperature). Indeed, tunneling processes are temperature insensitive but bandgap energy is decreased with temperature [9], increasing slightly leakage. When both contributions are summed up (line in Fig. 7), temperature behavior is well captured for the whole $|V_{DS}|$ range.

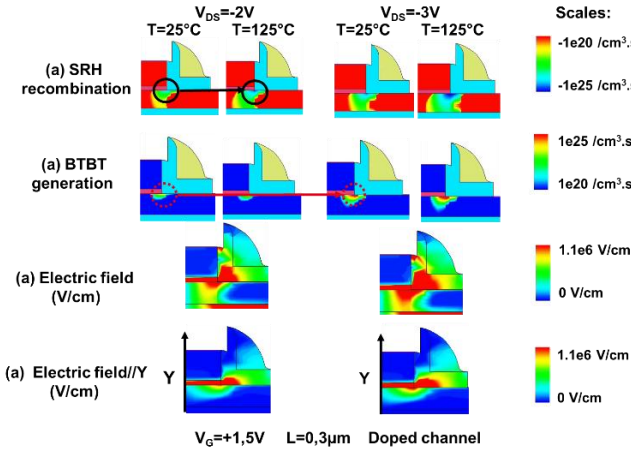

Fig. 8 : TCAD crossection of (a) SRH recombination, (b) BTBT generation, (c) Electric field, (d) Electric field projected on X axe for V_G=+1.5V, V_{DS}=-2V and -3V, doped channel and L=0.3µm.

This temperature (and electric field) dependence is illustrated in Fig. 8 by TCAD crossections. In fact, BTBT generation is mainly V_{DS} dependent and SRH recombination is both V_{DS} and temperature dependent. A noticeable difference concerns the location of generation/recombination processes: BTBT occurs just below gate/spacer interface when the vertical component of the electric field is larger than~$8x10^5$V/cm [5], whereas SRH is a diffused phenomenon following the electric field pattern around the junction. Thus, when SRH is the predominant leakage mechanism, both electric field component plays a role for leakage and not only the vertical one. Besides, $E_{A\ 25=>125°c}$ =0.057eV is extracted by TCAD, which is close to 0.07-0.06eV criteria used to discriminate between BTBT and SRH predominance in [6], which results from experimental observations.

IV. TCAD DRAIN LEAKAGE MODEL: VALIDATION WITH EXPERIMENTAL DATA

This part will set aside the proposed TCAD settings with experimental data to understand better back bias, silicon channel thickness and junction morphology impact on leakage.

A. *Back-bias polarization (V_{BS}):*

Fig. 9 presents the impact of back-biasing (V_{BS}) on I_D-V_{GS} curves for V_{DS}=-1.5V (SRH dominated region). It is worth noticing that applying a back bias shifts the threshold voltage value. Thus, it can modulate the "OFF current", when taken at a fixed V_{GS} value. This modulation can be significant if the current at V_{GS}=0V is limited by subthreshold slope. However, if we consider the minimum of drain leakage current, the modulation by back biasing is much lower.

To understand experimental data, TCAD cross-sections have been realized for various V_{BS} around the minimum of drain current. A leakage optimum is seen for 0V<V_{BS}<1V. In fact, for negative values (V_{BS}=-3V), a conductive back channel is formed at the BOX interface (see current density plot) explaining the large leakage increase. At the opposite, for large positive V_{BS} values (see SRH re-combination plot for V_{BS}=+6V), an additional SRH recombination generation occurs near the BOX interface compared to V_{BS}=0V, leading thus to a slight leakage increase.

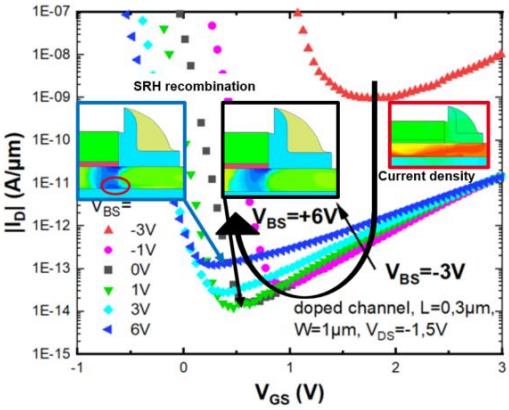

Fig. 9 : Exp. I_D-V_{GS} at V_{DS}=-1.5V and various V_B with TCAD cuts. A leakage optimum is seen for 0<V_{BS}<1V.

B. *Silicon channel thickness (t_{si}):*

Experimentally [6], drain leakage increases for lower silicon channel thickness in SRH region but remains the same in BTBT one. As seen previously, carrier lifetimes have been lowered down to correspond to a 23nm thick silicon film. In Fig. 10, we reduce simultaneously carrier lifetime and silicon thickness to reproduce experimental data behavior (t_{si}=16nm or 20nm).

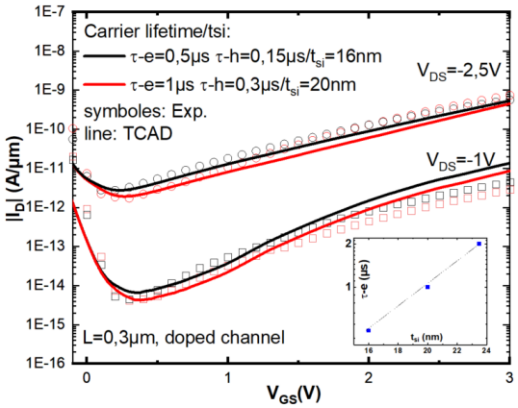

Fig. 10 : TCAD vs. EXP. I_D-V_{GS} for V_{DS}=-2.5V and V_{DS}=-1V. Inset: electron lifetime as a function of silicon channel thickness. Carrier lifetime is reduced to correspond to a silicon thickness reduction.

As an example, electron lifetime is reduced from 2µs down to 0.5µs to capture the leakage increase caused by a 23nm to 16nm channel thickness reduction. Carrier lifetime adjustments done to match the experimental channel thickness are displayed as a function of t_{si} (Fig.10-inset).

Note that, TCAD captures the SRH/BTBT behavior difference (black/red curves dissociated for low V_{DS}-V_{DS} and gather for large V_{GS} value at V_{DS}=-2.5V).

C. *Junction morphology:*

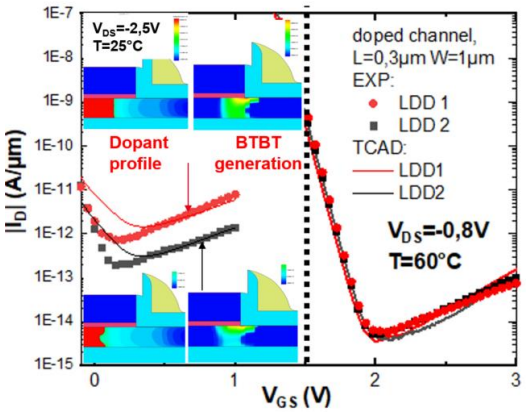

Fig. 11 : TCAD vs. Exp. I_D-V_{GS} for V_{DS}=-2.5V and V_{DS}=-0.8V for two LDD conditions.

Two implantation conditions for Lightly Doped Drain (LDD) are depicted in Fig. 11. LDD2 (black curves) results in a more overlapped and gradual junction with lower doping level compared to LDD1, lowering the electric field at gate corner. Measurements and TCAD show one decade leakage reduction at V_{DS}=-2.5V when BTBT is the identified predominant leakage mechanism [6]. In fact, the LDD2 junction morphology with a reduced electric field at the gate corner has a lower (see TCAD BTBT generation crossection cuts) BTBT generation compared to LDD1.

On the other side, no variation between LDD1 and LDD2 is observed for V_{DS}=-0.8V where SRH is predominant. In this particular case, engineering junction dopants position has no impact on drain leakage at low field. It highlights the importance of knowing the leakage mechanism causing the GIDL in order to optimize the device. Note that the proposed TCAD settings (in particular leakage model + carrier lifetime reduction) reproduce well the junction behavior.

Generally, leakage reduction guidelines in literature targets BTBT reduction by playing on dopants position (underlapped structure [11]) or suppression [1], which is valid only for specific device biases (and device dependent as well).

V. Conclusion

The present work has investigated the SOI pMOS drain leakage current thanks to electrical measurements and 2D-TCAD. The choice of Schenk BTBT model along with SRH model (Field-Enhanced, Schenk lifetime and doping dependence) enable the reproduction of experimental data. Carrier lifetime have been reduced to take into account our SOI device. Finally, the proposed TCAD settings predict well the experimental data for the whole range of operation, allowing future work for device optimization.

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