Next Generation Gate-all-around Device Design for Continued Scaling Beyond 2 nm Logic

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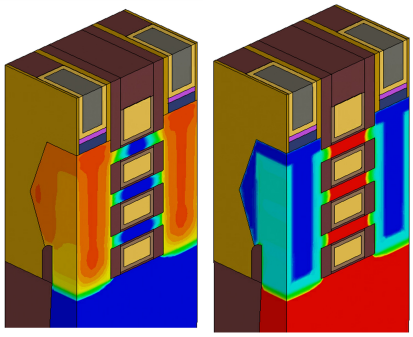
***Abstract*—We explore GAA transistor design elements for performance scaling beyond 2nm technology node. We examine the various resistance components of a 1st generation GAA FEOL transistor with typical 2nm node design rules. We propose different schemes to reduce each resistance component of the GAA transistor to improve its drive-current and circuit performance. Using our calibrated process, device and ring-oscillator modeling platform, we evaluate the device and circuit performance impact of each of these schemes. We show that the drive-current and circuit performance of GAA transistors can be improved by over 50% and 18%, respectively, which aligns with the performance scaling requirements for logic nodes beyond 2nm.**

***Index Terms*—Gate-All-Around, GAA, DTCO, Contact, Resistance, Ring Oscillator, Nanosheet, Device modeling.**

I. Introduction

Fin width scaling limitations and associated process variability challenges [1] in FinFET transistors have prompted logic industry to migrate to the Gate-All-Around (GAA) device architecture to continue area and performance scaling at the 2nm logic technology node and beyond [2]. The nanosheet (NS) channel thickness, in GAA transistors, is tightly controlled by the superlattice epitaxy process and provides all around gate-control that results in better electrostatics and scalability of the transistor.

Gate-All-Around (GAA) Structure and Dimensions

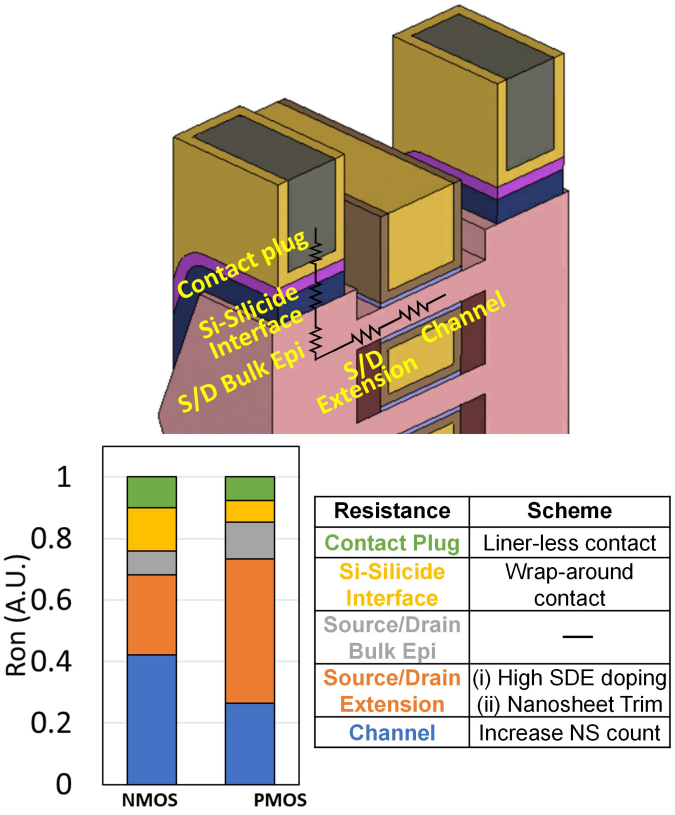


Parameter	Value
L_{Gate}	14 nm
CPP	45 nm
Nanosheet Width	25 nm
Nanosheet Thickness	5 nm
Spacer Width	5 nm

Fig. 1. Device structures of nMOS (left) and pMOS (middle) GAA transistors at the 2 nm technology node, along with key device dimensions (right).

For continuation of logic scaling beyond the 2nm node, it is important to explore the performance scaling knobs of GAA transistors. Typically, a 10% transistor drive-current (I-On) improvement is targeted from node-to-node. For technology nodes beyond 2nm, this cannot be achieved by mere gate-length and CPP (contacted poly pitch) scaling. In this paper, we highlight the different resistance components limiting the

Detailed Breakdown of GAA Resistance Components



Resistance	Scheme
Contact Plug	Liner-less contact
Si-Silicide Interface	Wrap-around contact
Source/Drain Bulk Epi	—
Source/Drain Extension	(i) High SDE doping (ii) Nanosheet Trim
Channel	Increase NS count

Fig. 2. Components of ON-resistance (R-On) of a GAA device, respective values in nMOS and pMOS GAA device, and schemes to reduce each.

GAA performance and investigate various structure optimization schemes targeted to improve these components using our calibrated process, device, and ring-oscillator Materials to Systems Co-Optimization (MSCO^{TM}) modeling platform [3]–[7].

II. 1st Generation Gate-all-Around Transistor Characteristics

Typical 2nm design rules are used for the baseline GAA nMOS and pMOS devices with 3 nanosheets (Fig. 1). Fig. 2 indicate different resistance components of these GAA transistors. In general, we see that the channel resistance (R-channel) and source/drain (S/D) extension resistance (R-SDE) are the major components, followed by significant contribution from the epi/silicide contact interface (R-contact-interface).

Proposed Structure-Optimization Schemes to Improve GAA Drive-Strength

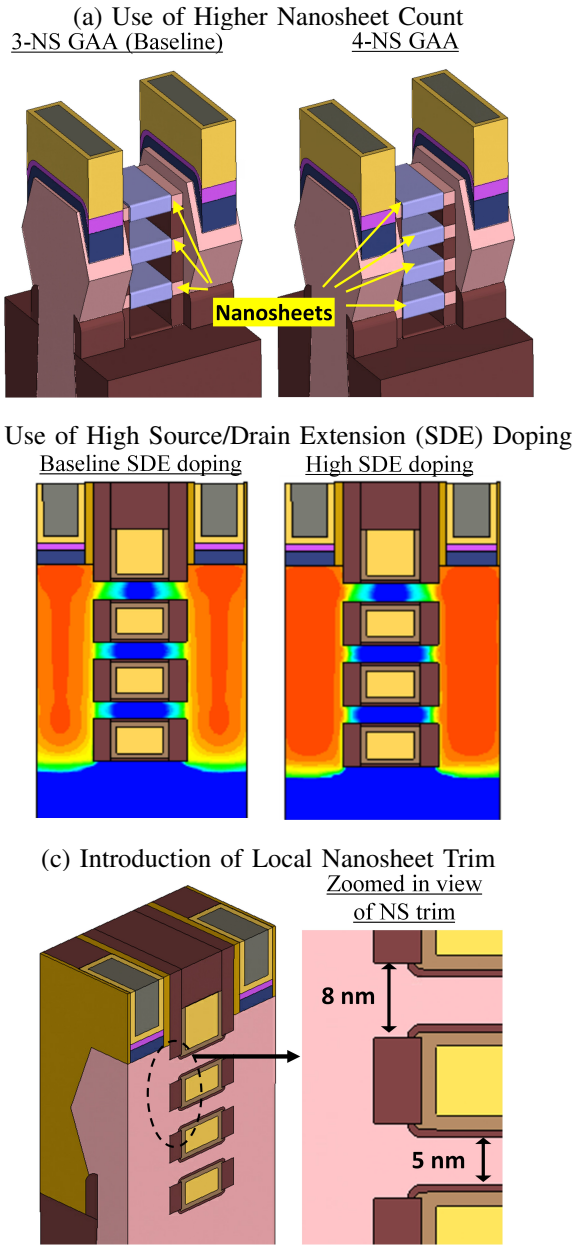


Fig. 3. Proposed structure optimization to reduce overall R-On by (a) increasing nanosheet count per device from 3 to 4 to reduce channel resistance (b) using higher SDE doping to reduce S/D extension resistance, and (c) reducing SDE resistance by introducing local nanosheet trim which results in wider extension region.

We propose separate process schemes to reduce each of these components (Fig. 2) and investigate the impact on device and circuit performance in the remainder of this work.

A. R-channel Improvement with 4 Nanosheets

The channel resistance (R-channel) can be reduced by adding more nanosheets to the GAA transistor (Fig. 3(a)). Our modeling results show that addition of one more nanosheet

R-On and I-On Improvement by Device Optimization

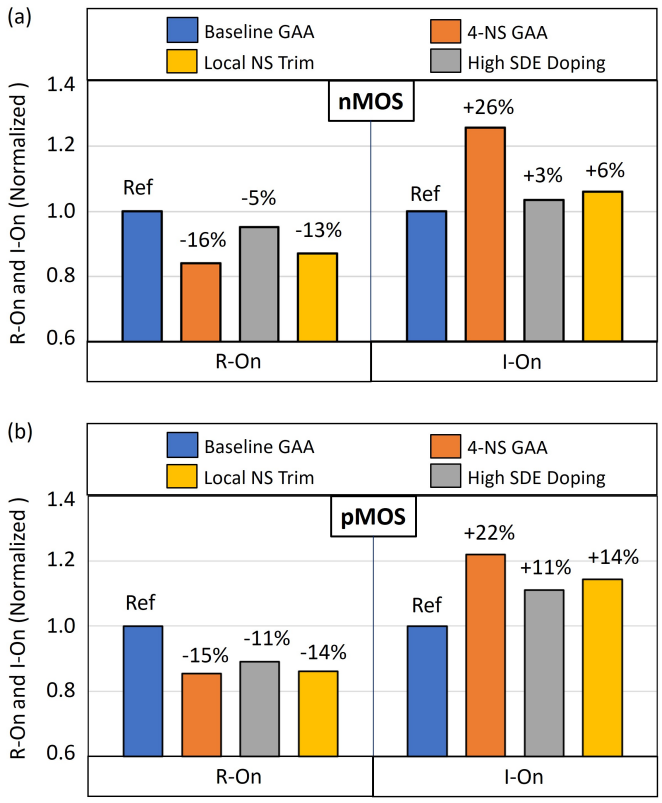


Fig. 4. Percentage improvement of various schemes on R-On and I-On for (a) nMOS and (b) pMOS GAA devices. Among the three, increasing the NS count is the most effective in reducing R-On and improving I-On in nMOS and pMOS, resulting in 26% and 22% I-On improvement, respectively. Local NS trim and higher SDE doping are more effective in pMOS than nMOS because S/D extension resistance makes up a large part of R-On in pMOS.

in nMOS and pMOS GAA device can improve R-On and I-On by 15% and 22-26% respectively, compared to baseline GAA device with 3 NS (Fig. 4). The addition of a nanosheet provides additional current flow path in the GAA device, thus improving R-channel and R-On. In our modeling, the superlattice stack height with 4 nanosheets is assumed to be similar to the 3-NS device, which can be achieved by reducing SiGe-NS thickness.

B. R-SDE Improvement Using Higher S/D Extension Doping

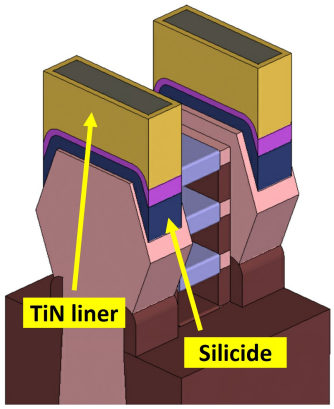
To reduce source/drain extension resistance (R-SDE), higher extension doping can be used (Fig. 3(b)). Using a 3x higher S/D extension doping can result in a 5% and 11% improvement in total R-On for nMOS and pMOS, respectively (Fig. 4). The R-On improvement for GAA pMOS is higher as R-SDE constitutes a larger fraction of the total R-On for GAA pMOS. These R-On improvements lead to a 3% and 11% I-On improvement in the nMOS and pMOS, respectively (Fig. 4).

C. R-SDE Improvement Using Local Nanosheet Trim

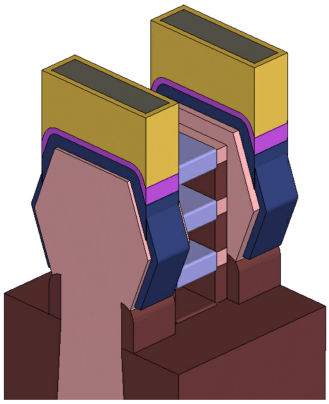
R-SDE can be further improved by using wider extension regions, typically implemented using a local nanosheet trim

Contact-Resistance Reduction Schemes for Improving GAA Performance

(a) Baseline S/D Contact Configuration



(b) Wrap-Around S/D Contact Configuration



(c) Liner-less S/D Contact Configuration

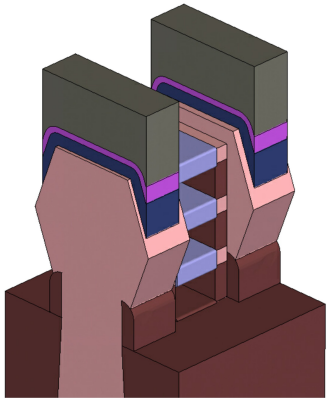


Fig. 5. Comparison of (a) baseline source/drain (S/D) contact configuration with different schemes to reduce contact resistance: (b) wrap around contact (WAC) silicidation scheme, and (c) liner-less contact plug scheme (replacement of TiN liner).

technique [8]. Fig. 3(c) shows the modified GAA device structure with 8nm wider S/D extension region, while keeping the NS thickness at 5nm as in the baseline case. The wider extension region leads to a 13-14% R-On benefit (Fig. 4) for both nMOS and pMOS GAA. Consequently, I-On in nMOS

Contact Optimization: Impact on Device Performance

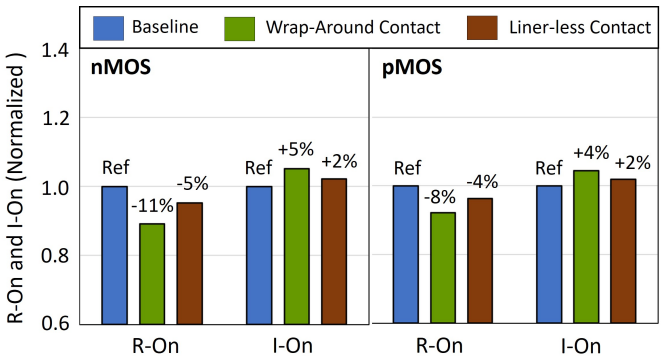


Fig. 6. Percentage improvement of different contact optimization schemes on R-On and I-On. Comparing to linerless contact plug scheme, the WAC results in higher improvement in both nMOS and pMOS.

and pMOS are improved by 6% and 14%, respectively (Fig. 4).

D. R-contact-interface Improvement Using Wrap-Around Contact (WAC)

To reduce S/D-epi/silicide contact interface resistance (R-contact-interface), the contact area needs to be increased. This can be enabled by a wrap-around contact (WAC, Fig. 5(b)) [9], [10], in which the silicide is also placed in the bottom facets of the S/D-epi also. According to our modeling results, WAC can lead to 8-11% R-On improvement in GAA by reducing contact resistance (Fig. 6). This results in a 4-5% I-On improvement (Fig. 6).

E. R-contact-plug Improvement using Liner/Barrier-less Contact Fill

The contact plug resistance (R-contact-plug) can be reduced by using a liner/barrier-less deposition process (such as, selective tungsten [4]), which eliminates the highly resistive liner and barrier layers (TiN, for example) (Fig. 5(c)). This

Net Impact on GAA Performance with All Schemes Combined

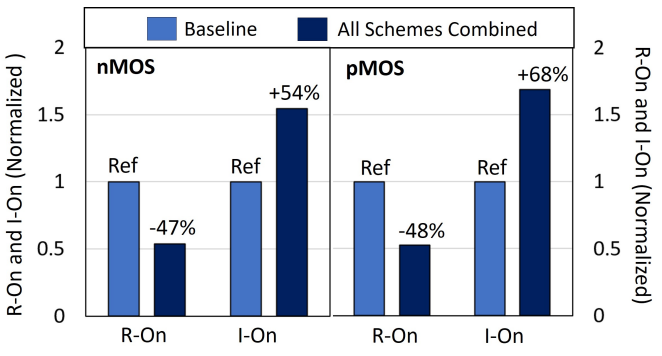


Fig. 7. Net effect of combined optimization schemes: When all improvement schemes are applied, we see a considerable I-On increment of 54% and 68% in nMOS and pMOS, respectively.

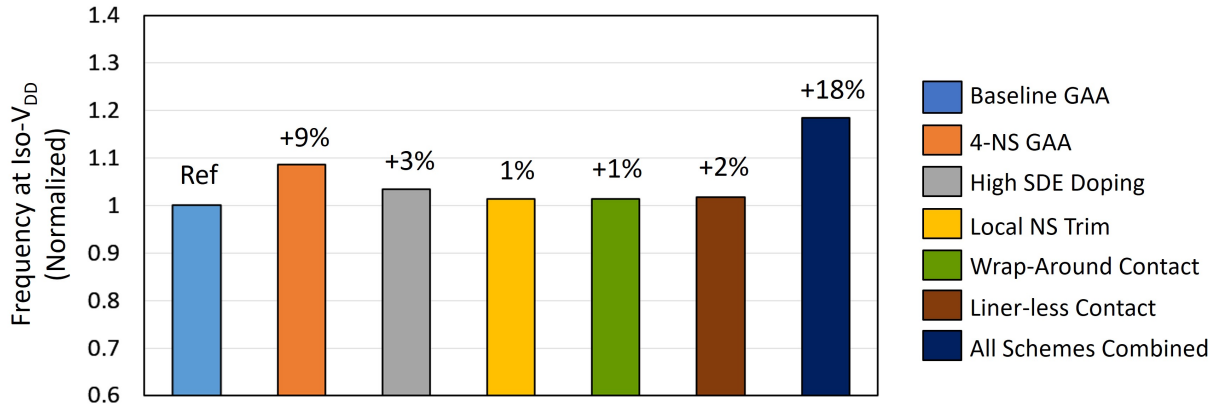


Fig. 8. Comparison of the impact of different optimization schemes on the ring-oscillator (RO) performance (Frequency at iso-VDD). A combined RO performance improvement of 18% over baseline configuration is observed when all optimization schemes are combined.

approach results in 5% and 2% improvement in R-On and I-On, respectively (Fig. 6).

Fig. 7 shows the expected R-On and I-On improvement by integrating all the aforementioned schemes. Such a GAA device (Fig. 7) can show 47% R-On reduction and 54 - 68% drive-current improvement for nMOS and pMOS, compared to a typical 2nm baseline GAA device. Thus, our proposed schemes can significantly improve the overall GAA drive-strength and enable scaling beyond the 2nm technology nodes.

III. Impact on Circuit Performance

To project the impact of the proposed schemes on circuit performance, we utilize our MSCO^{TM} platform and a ring-oscillator (RO) circuit and compare the PPA (power, performance and area) metrics. The RO modeling and PPA metrics extraction also includes any capacitance modification that would result from these proposed schemes. Figure 8 compares the RO performance improvement for different proposed schemes compared to the baseline GAA. The R-channel improvement with 4-NS leads to 9% circuit performance (frequency) improvement. Use of higher SDE doping for R-SDE reduction leads to a 3% circuit performance improvement. The local NS trim scheme, however, exhibits less (1%) improvement for a self-loaded RO scenario due to capacitance increase. The wrap-around contact and liner-less contact schemes for contact resistance reduction result in 1% and 2% circuit performance improvement, respectively. Combining all of these schemes, the circuit performance can be improved by 18%, in line with typical FEOL performance enhancement requirements for one or two nodes.

IV. Conclusion

In summary, we show that our proposed schemes to improve GAA resistance components can result in a combined drive-strength improvement of over 50% at the transistor-level and 18% performance improvement at the RO circuit-level. The significance of the study is highlighted by the fact that the extent of improvement is on par with the targeted node-to-node improvement without any scaling introduced to the gate-length and the contacted gate/poly pitch (CPP).

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